STP3481

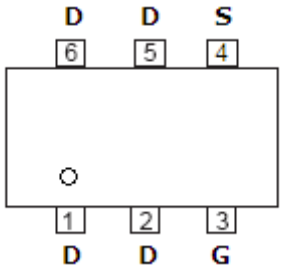
P Channel Enhancement Mode MOSFET

-5.2A

DESCRIPTION

The STP3481 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

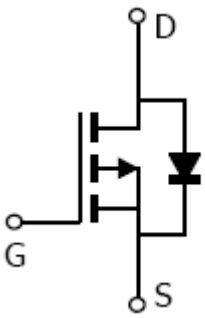
PIN CONFIGURATION
TSOP-6P



1.2.5.6.Drain 3.Gate 4.Source

FEATURE

- -30V/-5.2A, $R_{DS(ON)}$ = 55m-ohm @VGS = -10V
- -30V/-4.2A, $R_{DS(ON)}$ = 75m-ohm @VGS = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TSOP-6P package design



PART MARKING
TSOP-6P



Y: Year Code A: Process Code

ORDERING INFORMATION

Part Number	Package	Part Marking
STP3481S6RG	TSOP-6P	81YA

※ Process Code : A ~ Z ; a ~ z

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※ STP3481S6RG S6 : TSOP-6P ; R : Tape Reel ; G : Pb – Free

ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain CurrentTJ=150℃)	T_A=25℃ T_A=70℃	I_D	-5.2 -4.2	A
Pulsed Drain Current		I_{DM}	-20	A
Continuous Source Current (Diode Conduction)		I_S	-1.7	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	2.0 1.3	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	90	℃/W

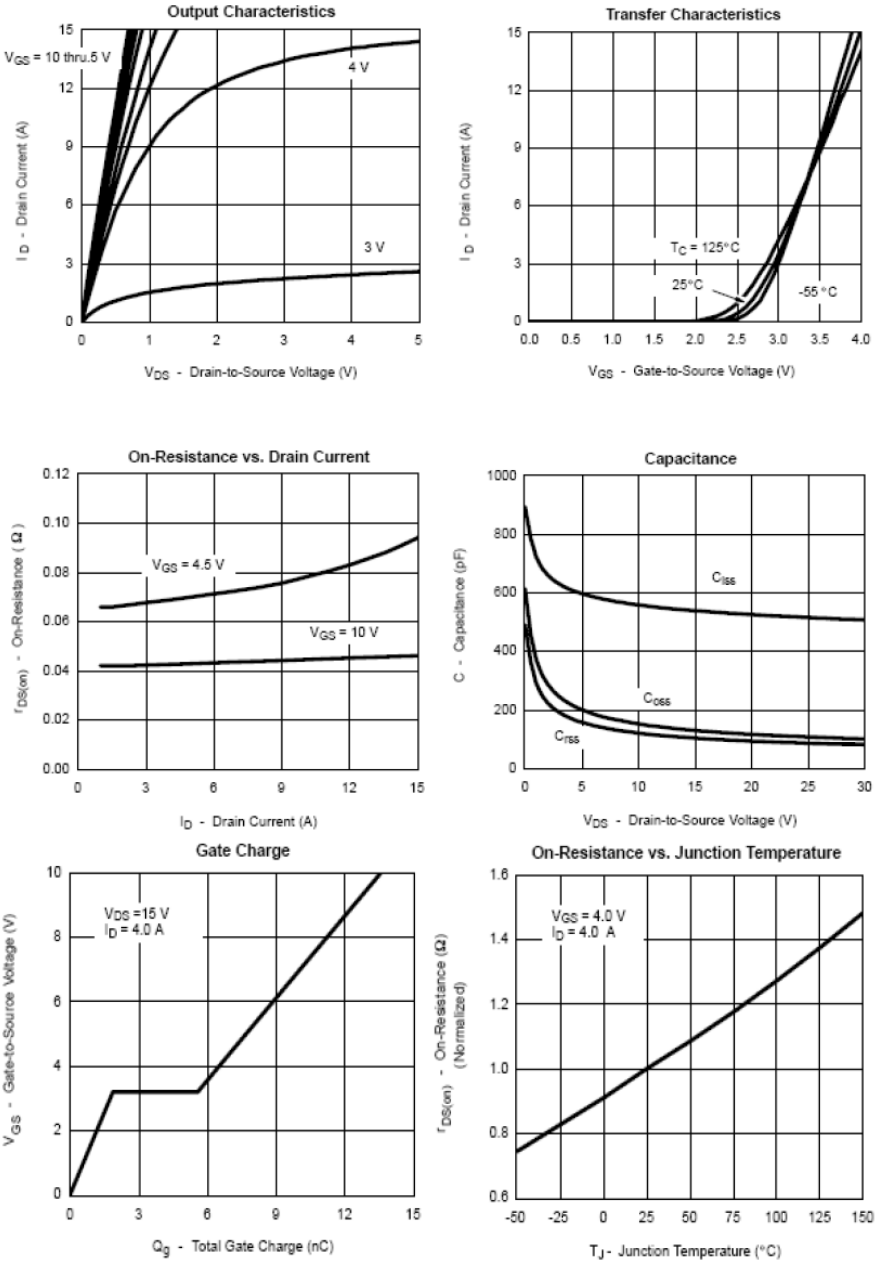
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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250uA	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	Na
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-1	UA
		V_{DS}=-24V, V_{GS}=0V T_J=55℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V, V_{GS}=-10V	-10			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10.0V, I_D=-5.2A V_{GS}=-4.5V, I_D=-4.2A		0.041 0.058	0.055 0.075	Ω
Forward Transconductance	g_{fs}	V_{DS}=-5.0V, I_D=-4.0A		10		S
Diode Forward Voltage	V_{SD}	I_S=-1.0A, V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V V_{GS}=-10V I_D≡-4.0A		14	21	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			3.7		
Input Capacitance	C_{iss}	V_{DS}=-15V V_{GS}=0V F=1MHz		540		pF
Output Capacitance	C_{oss}			131		
Reverse Transfer Capacitance	C_{rss}			105		
Turn-On Time	$t_{d(on)}$ tr	V_{DD}=-15V R_L=15Ω I_D=-1.0A V_{GEN}=-10V R_G=6Ω		10	16	nS
				15	25	
Turn-Off Time	$t_{d(off)}$ tf			32	50	
				21	32	

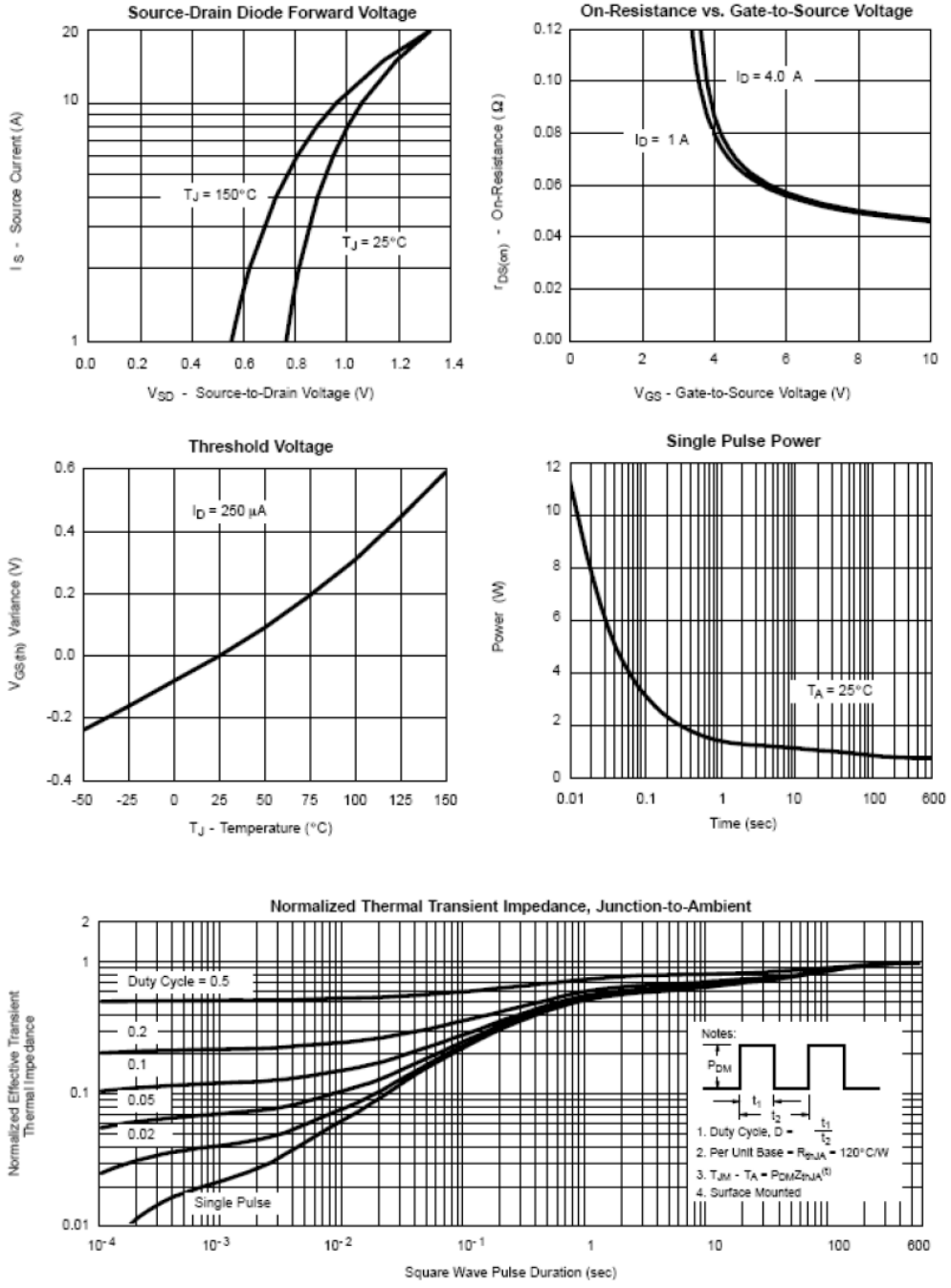
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TYPICAL CHARACTERICTICS (25℃ Unless noted)



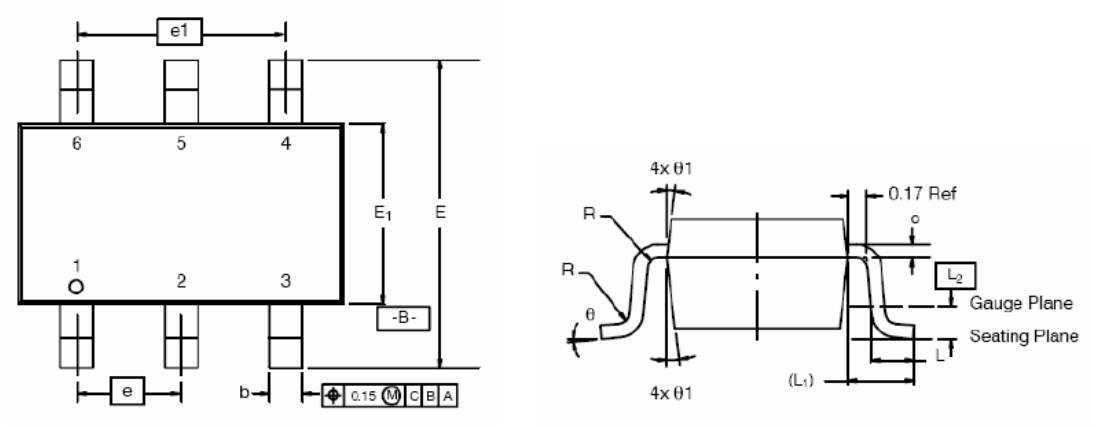
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TYPICAL CHARACTERICTICS (25℃ Unless noted)



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TSOP-6P PACKAGE OUTLINE



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	1.00 BSC			0.0394 BSC		
e_1	1.90	2.00	2.10	0.075	0.080	0.085
L	0.35	-	0.50	0.014	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom			7° Nom		

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