MP86963

High Efficiency, 20A, 27V Intelli-Phase™ Solution (Integrated HS/LS FETs and Driver) in a 5x5mm QFN

The Future of Analog IC Technology

DESCRIPTION

The MP86963 is a monolithic Half Bridge with built-in internal power MOSFETs and gate driver. It achieves 20A continuous output current over a wide input supply range.

Integrating the Driver and MOSFETs results in high efficiency due to optimal dead time control and parasitic inductance reduction.

The MP86963 is a Monolithic IC designed to drive up to 20A per phase. Housed in a very small 5x5mm TQFN Packge, this device can be operated from 100kHz to 1MHz operation.

The IC is intended to work with 3.3V tri-state output controllers.

The MP86963 is ideal for notebook applications where efficiency and small size are a premium.

FEATURES

- Wide 4.5V to 21V Operating Input Range
- 20A Output Current
- Simple Logic Interface (3.3V)
- Operate from 100kHz to 1MHz
- Accepts 3-state PWM Input
- Suitable for single-/multi-phase operation
- Available in a 5mm x 5mm TQFN Package
- ROHS6 Compliant

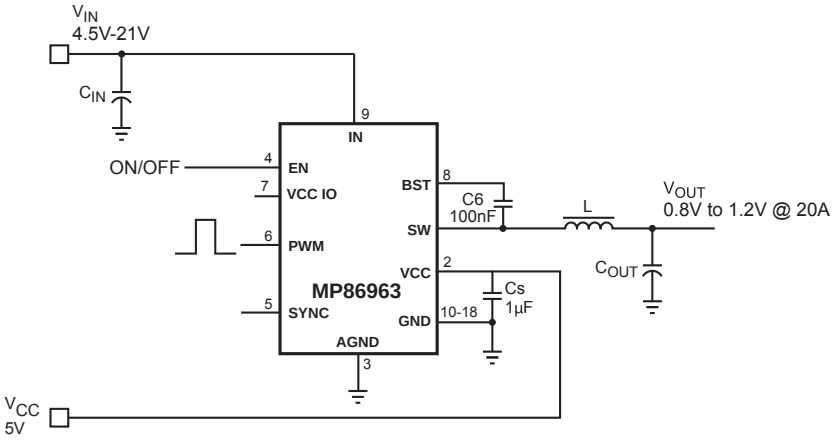
APPLICATIONS

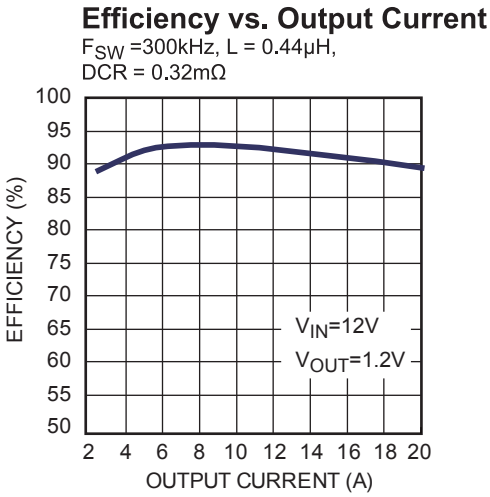
- Power modules
- Notebook, Core Voltage
- Graphic Card Core Regulators

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This Product is Patent Pending.

TYPICAL APPLICATION





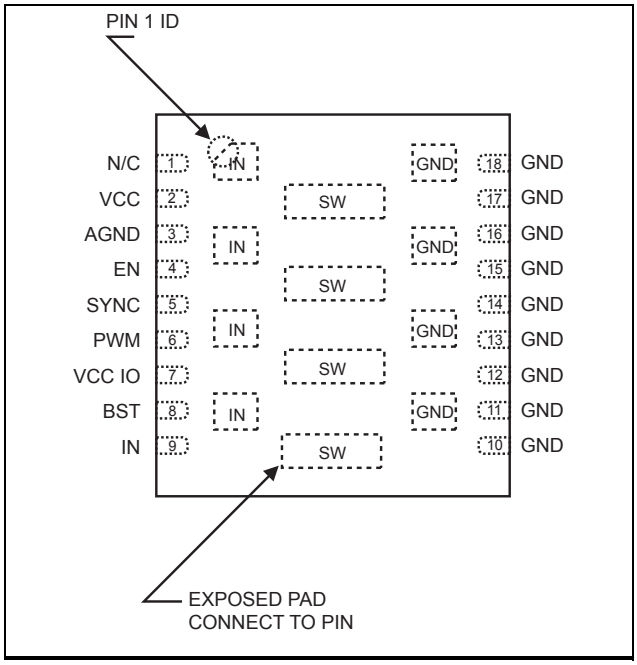
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ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature(T_A)
MP86963DUT	5x5 TQFN	86963UT	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP86963DUT–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP86963DUT–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 27V
V_{SW}(DC) .....-0.3V to V_{IN} +0.3V
V_{SW}(20ns) .....-3V to V_{IN} +3V
V_{BST} ..... V_{SW} + 6V
All Other Pins .....-0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 3.8W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....4.5V to 21V
V_{CC} Driver Voltage…….4.5V to 5.5V
Operating Junct. Temp (T_J)..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
5x5 TQFN	33	8....	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I_{CC} Standby	I_{CC_Stdby}	V_{CC} =5V, PWM=EN=LO		550	610	µA
I_{IN} (Shutdown)	$I_{IN\ (Off)}$	V_{CC} = 0V		1	5	µA
I_{IN} Standby	I_{IN_Stdby}	V_{CC} =5V, PWM=EN=LO		1		µA
Rise Time		I_{OUT} = 20A		5		ns
Fall Time		I_{OUT} = 20A		3		ns
Minimum On-Time				55		ns
Dead-Time Rising				5		ns
Dead-Time Falling				10		ns
V_{CC} Under Voltage Lockout Threshold Rising				3.7	4.2	V
V_{CC} Under Voltage Lockout Threshold Hysteresis				470		mV
SYNC Pull-Up Current	I_{SYNC}	SYNC=0V		-14		µA
SYNC Logic High Voltage			2			V
SYNC Logic Low Voltage					0.4	V
EN Input Low Voltage					0.4	V
En Input High Voltage			2			V
PWM Input						
Input Current	I_{PWM}	V_{PWM}=3.3V		370		µA
		V_{PWM}=0V		-370		µA
V_{CC}IO			2.9	3.3	3.6	V
PWM Low to Tri-State Threshold				1.10		V
PWM Tri-State to High Threshold				2.25		V
PWM High to Tri-State Threshold				2.10		V
PWM Tri-State to Low Threshold				0.75		V
Tri-State Shutdown Holdoff Time	t_{TSSHD}	V_{CC}=5V, Temperature=25°C		100		ns
UG/LG Three-State Propagation Delay	t_{PTS}			20		ns
USW Turn-Off Propagation Delay	t_{PDUL}	V_{CC}=5V		40		ns
LSW Turn-Off Propagation Delay	t_{PDLL}	V_{CC}=5V		25		ns
USW Turn-On Propagation Delay	t_{PDUH}	V_{CC}=5V		30		ns
LSW Turn-On Propagation Delay	t_{PDLH}	V_{CC}=5V		50		ns

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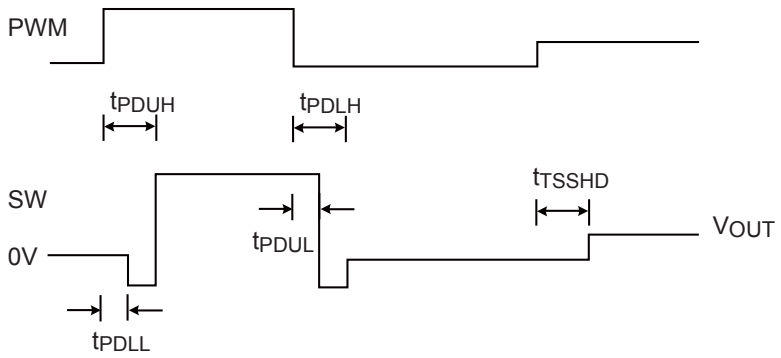


Figure 1—Timing Diagram

PIN FUNCTIONS

Pin #	Name	Description
1	NC	Not Connected.
2	V_{CC}	Low-Side Driver Bias Supply. Decouple with a 1µF ceramic capacitor.
3	AGND	Signal Ground.
4	EN	Active High On/Off Control. Pulling this Pin Low forces the SW Pin to be in a high impedance state.
5	SYNC	Leaving this pin Open enables theLower Synchronous Switch. Pulling it Low forces the Lower Switch into Diode Emulation mode.
6	PWM	Pulse Width Modulation Control. Accepts three-state input. Force PWM to midstate or open to place SW into high impedance state.
7	V_{CC} IO	Reference voltage that connects to PWM driver supply.
8	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BST pins to form a floating supply across the power switch driver.
9 Exposed Pad	IN	Supply Voltage. C_{IN} is needed to prevent large voltage spikes from appearing at the input.
10–18 Exposed Pad	GND	Power Ground.
Exposed Pad	SW	Switch Output. These pins are fused together.

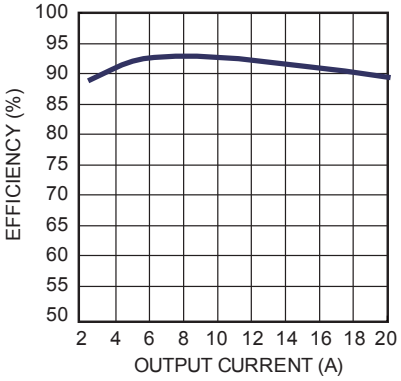
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{CC} = 5V, V_{OUT} = 1.2V, T_A = +25°C, unless otherwise noted.

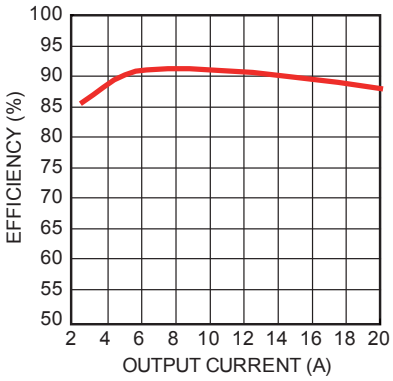
300kHz Efficiency

F_{SW} =300kHz, L = 0.44µH, DCR = 0.32mΩ



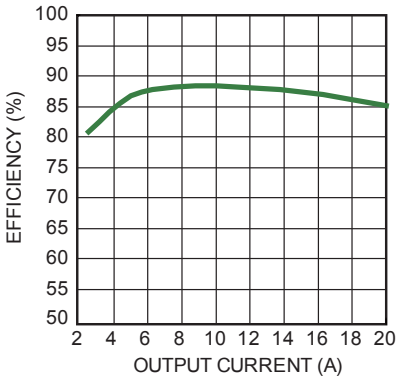
600kHz Efficiency

F_{SW} =600kHz, L = 0.44µH, DCR = 0.32mΩ



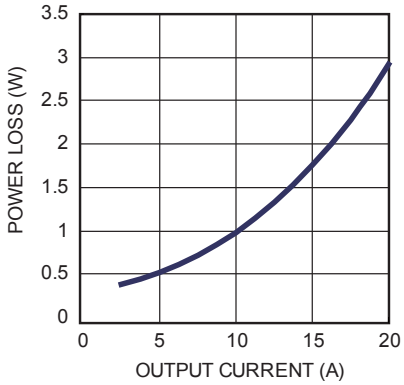
1.0MHz Efficiency

F_{SW} =1.0MHz, L = 0.44µH, DCR = 0.32mΩ



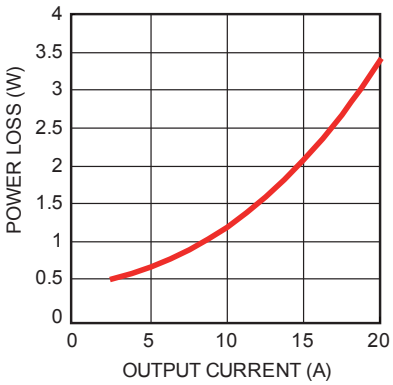
300kHz Power Loss

F_{SW} =300kHz, L = 0.44µH, DCR = 0.32mΩ



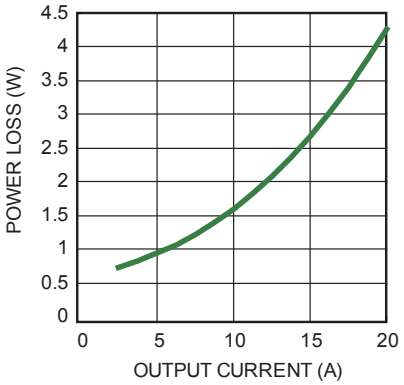
600kHz Power Loss

F_{SW} =600kHz, L = 0.44µH, DCR = 0.32mΩ



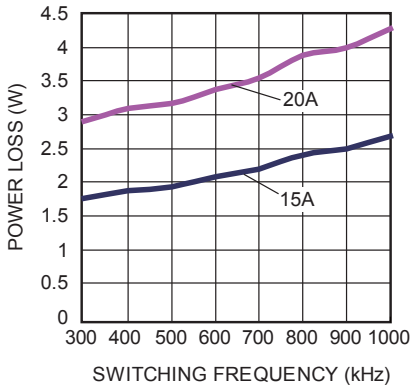
1.0MHz Power Loss

F_{SW} =1.0MHz, L = 0.44µH, DCR = 0.32mΩ



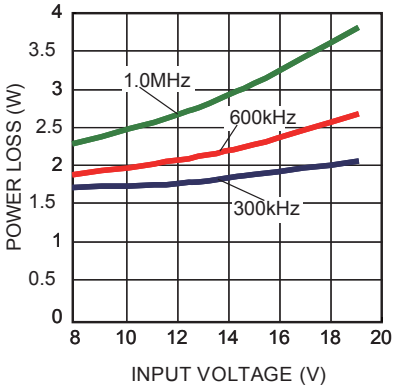
Power Loss vs. Switching Frequency

L = 0.44µH, DCR = 0.32mΩ



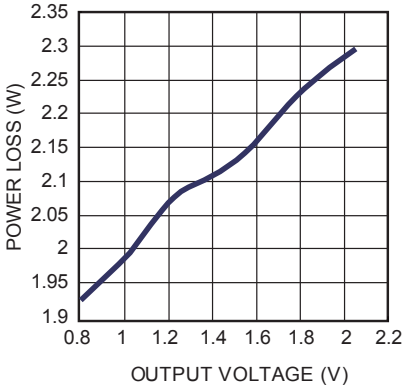
Power Loss vs. Input Voltage

L = 0.44µH, DCR = 0.32mΩ
I_{OUT}=15A



Power Loss vs. Output Voltage

L = 0.44µH, DCR = 0.32mΩ
I_{OUT}=15A, Fsw=600kHz



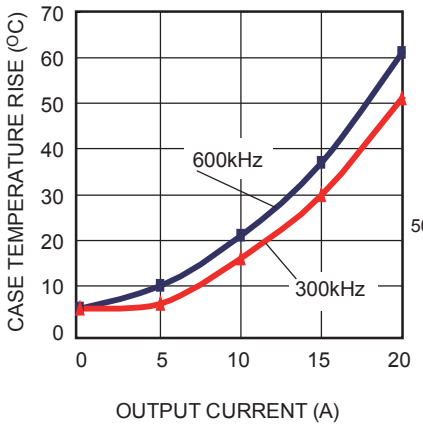
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{CC} = 5V, V_{OUT} = 1.2V, T_A = +25°C, unless otherwise noted.

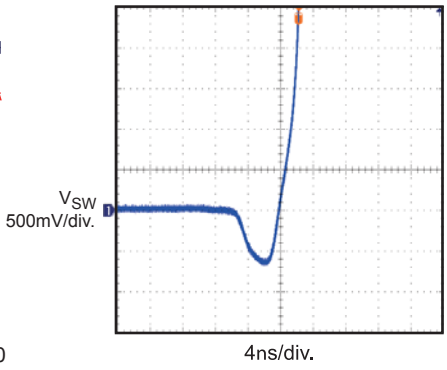
Temperature Rise vs. Output Current

No airflow



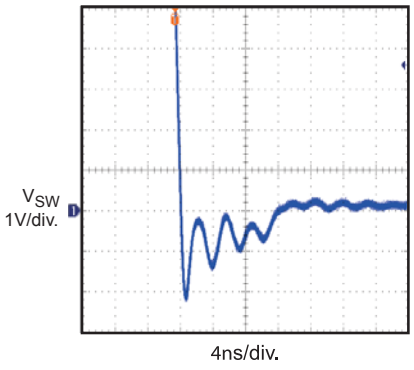
SW Rising Edge Dead Time

I_{OUT} = 15A



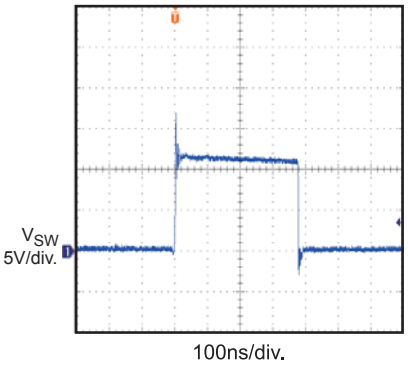
SW Falling Edge Dead Time

I_{OUT} = 15A



Output Waveform

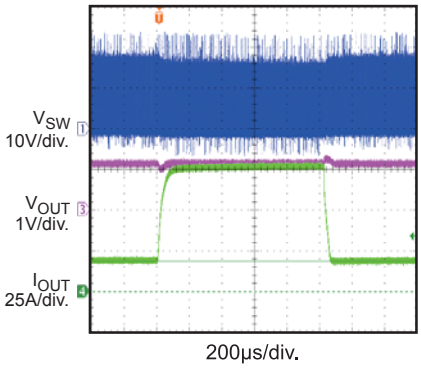
I_{OUT} = 20A



SOA Waveform

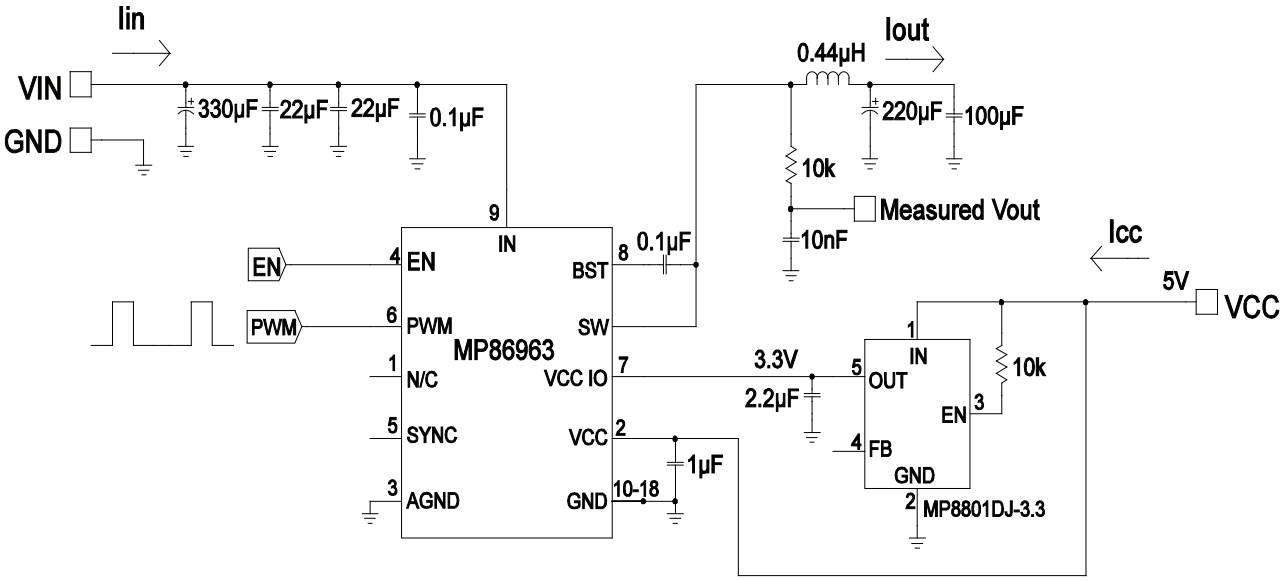
V_{IN} = 19V, V_{OUT} = 1.2V

I_{OUT} = 20A to 80A, F_{SW} = 600kHz



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EFFICIENCY MEASUREMENT SETUP



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BLOCK DIAGRAM

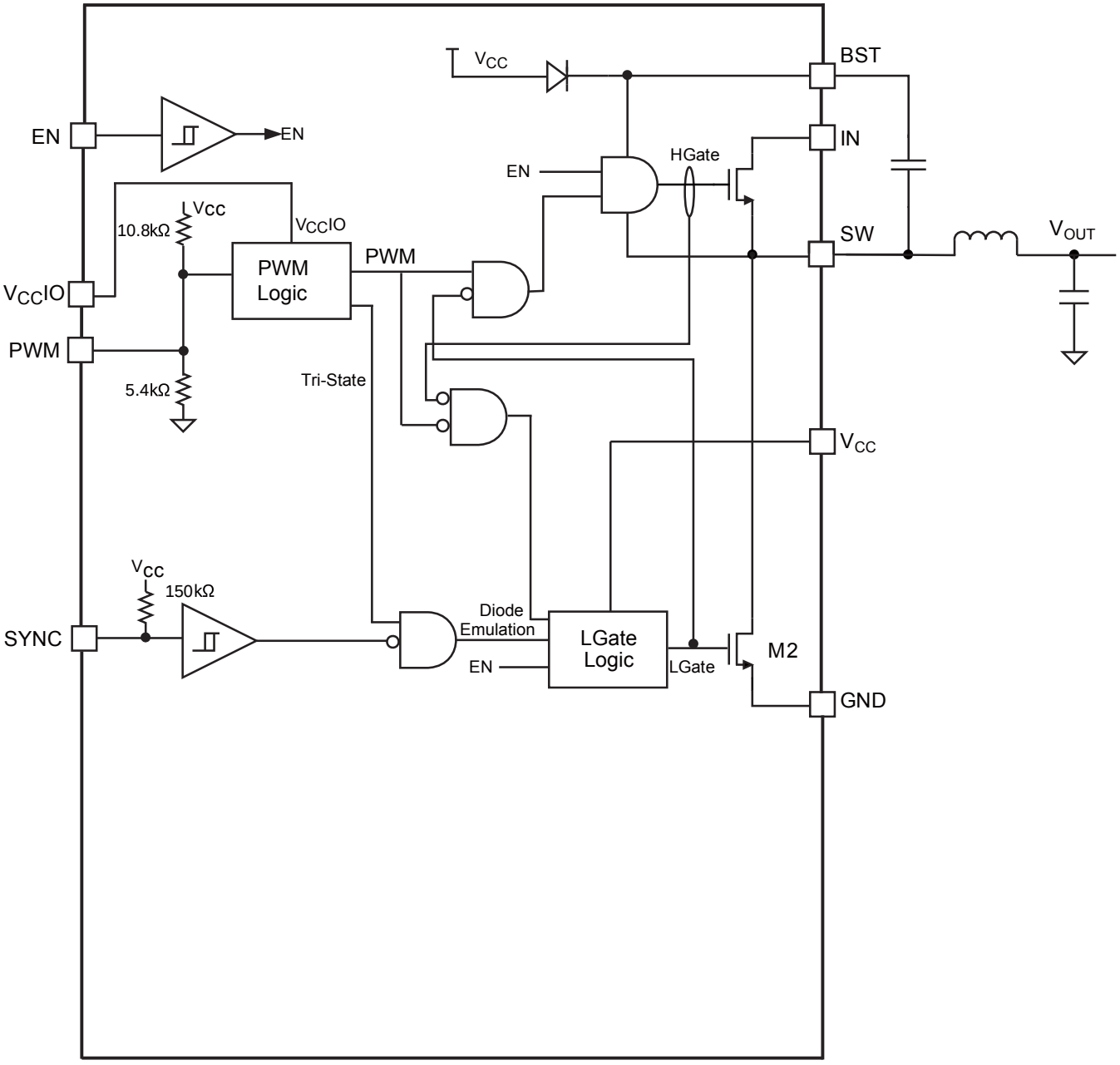


Figure 2—Function Block Diagram

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OPERATION

The MP86963 is a 20A Monolithic Half Bridge driver with MOSFETs ideally suited for single-/multi-phase Buck regulators.

Once the EN, V_{IN}, V_{CC}IO, V_{CC} and V_{BST} signals are sufficiently high, operation begins. BST voltage has a typical rising UVLO of 2.2V and a falling UVLO of 2.0V. When BST is below the UVLO voltage, the device will be off.

MP86963 can work with most PWM controllers. The device accepts PWM signal from 100kHz up to 1MHz. There is an internal resistor divider to put PWM voltage to tri-state region if the PWM pin is open.

Internally, SYNC is tied to V_{CC} through a resistor. By default, the device will operate in synchronous mode. To enter Diode Emulation mode, drive SYNC pin LOW.

Startup and Shutdown Sequence

MP86963 can work with any startup or shutdown sequencing combination of V_{IN}, V_{CC}, V_{CC}IO and EN. If PWM signal is present, the MP86963 will start working whenever V_{IN}, V_{CC}, V_{CC}IO and EN are ready. On the other hand, if any of these signals is not ready, the MP86963 will stop working. However, it is recommended to turn on and turn off the device through the EN pin.

PCB Layout Guideline

PCB layout is very important to achieve stable operation. Please follow these guidelines to achieve optimal performance.

1) Keep the path of switching current short and minimize the loop area formed by input capacitor. Keep the connection between SW pin and input power ground as short and wide as possible.

2) Always place some input bypass ceramic capacitors next to the device and on the same layer as the device. Do not put all of the input bypass capacitors on the back side of the device. Use as many vias and input voltage planes as possible to reduce the switching spike. BST capacitor and V_{CC} capacitor should also be as close to the device as possible.

3) The recommended external BST cap is 100nF. Do not use a capacitance value lower than 100nF. Place a 1.0Ω resistor between the BST capacitor and BST pin for optimized performance.

4) Do not place via on the pad or on the pin footprint. Doing so may cause soldering issue during the assembling process. Use Figure 3 as a via placement reference.

5) Connect IN, SW and GND to large copper area and use vias to cool the chip to improve thermal performance and long-term reliability. See Figure 4 as an example.

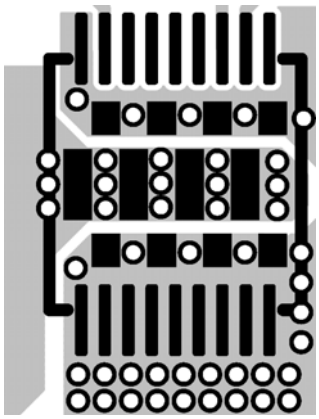


Figure 3—Via Placement Guideline

Do not put via on the device's pad footprint or pin footprint to avoid assembly issue. Use as many vias as possible to cool down the device.

6) Place the V_{CC} decouple capacitor close to the IC. Connect AGND and PGND at the point of V_{CC} capacitor's ground connection.

Recommended SMT Setting

Stencil thickness: 0.12mm

EP Pad Opening: (Stencil opening : Real PCB Size)

Length: 0.85:1
Width: 1:1
Note: The EP pad for Intelli-Phase are IN, SW and GND pad on the bottom.

Solder type: #3

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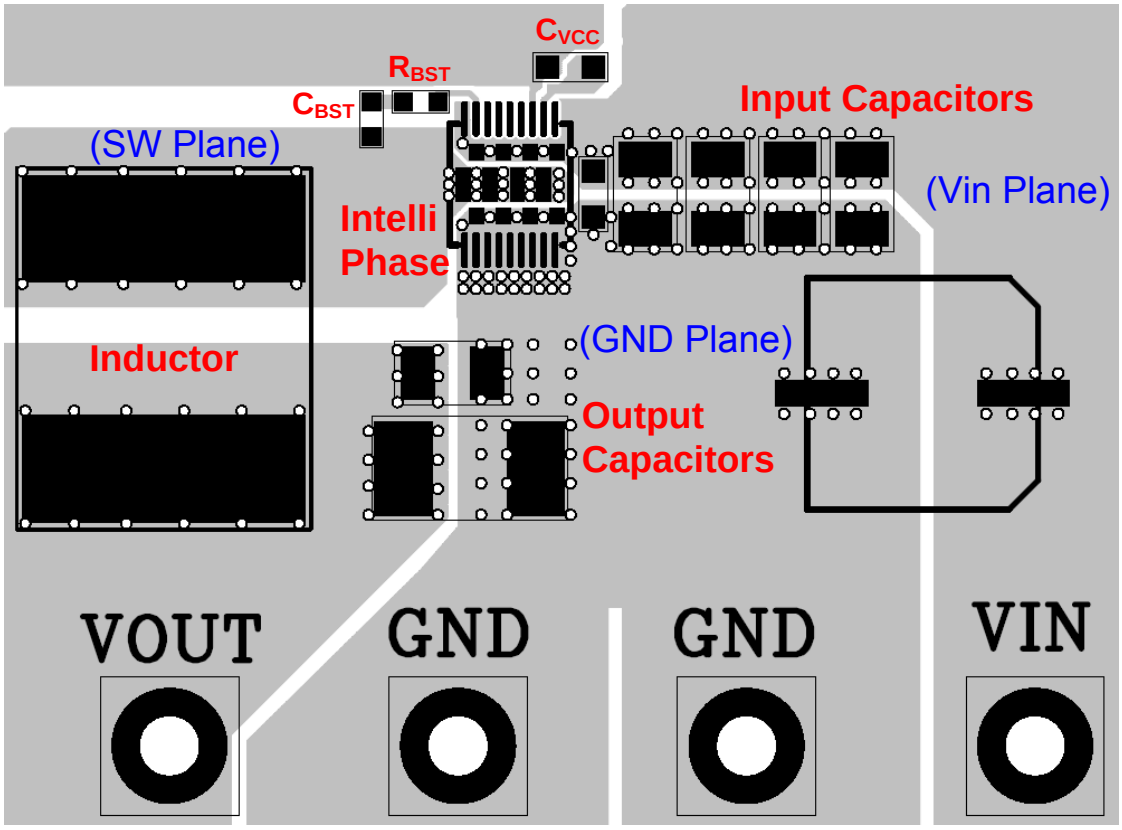


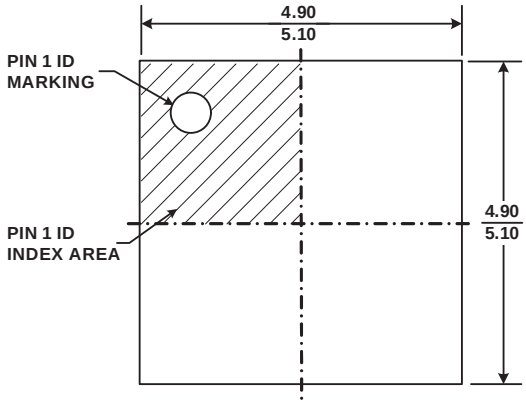
Figure 4—Copper Area Guideline

Use large copper area, many vias and many IN, SW and GND inner layer planes to achieve optimal thermal performance.

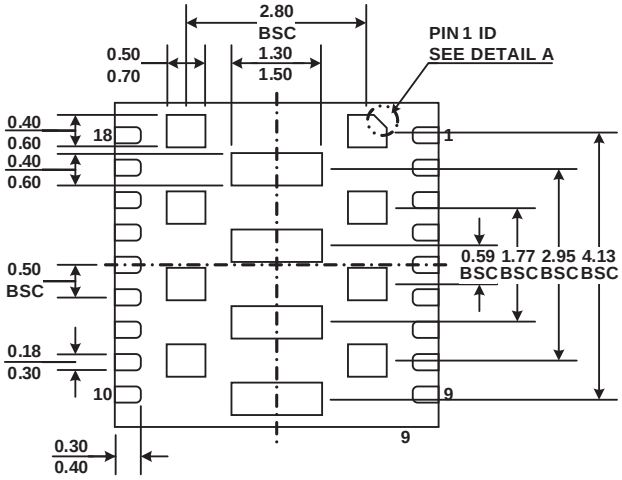
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PACKAGE INFORMATION

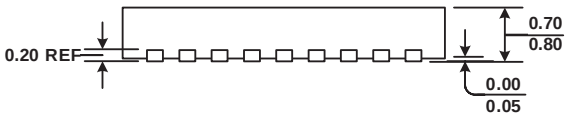
FCTQFN18L (EXPOSED PAD)



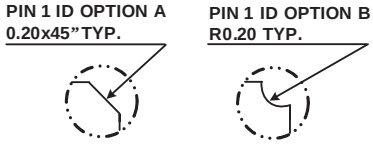
TOP VIEW



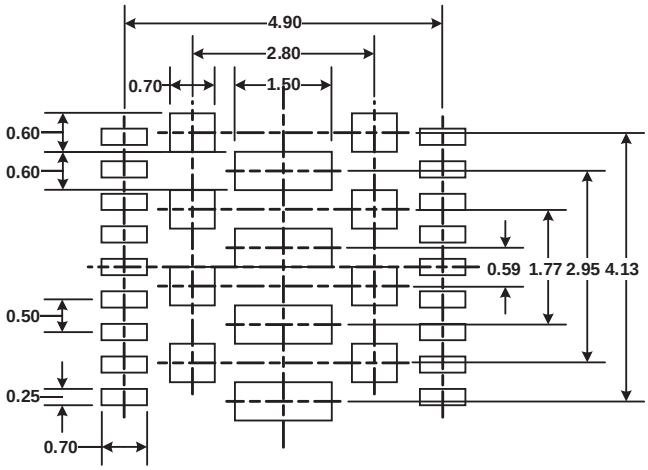
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-229, VARIATION WJJD.
5) DRAWING IS NOT TO SCALE

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