High Efficiency, Main Power Supply Controller for Notebook Computers

General Description

The RT8243A/B/C is a dual step down, Switch Mode Power Supply (SMPS) controller which generates logic supply voltages for battery powered systems. It includes two Pulse Width Modulation (PWM) controllers adjustable from 2V to 5.5V and also two fixed 5V/3.3V linear regulators. One of the controllers (LDO5) provides automatic switch over to the BYP1 input connected to the main SMPS1 output for maximized efficiency. An optional external charge pump can be monitored through SECFB (RT8243B/C). Other features include on board power up sequencing, a power good output, internal soft-start, and a soft discharge output that prevents negative voltage during shutdown.

A constant on-time PWM control scheme operates without sense resistors and assures fast load transient response while maintaining nearly constant switching frequency. To eliminate noise in audio applications, an ultrasonic mode is included, which maintains the switching frequency above 25kHz. Moreover, a diode emulation mode maximizes efficiency for light load applications. The SMPS1/SMPS2 switching frequency can be adjustable from 200kHz/233kHz to 400kHz/466kHz respectively.

The RT8243A/B/C is available in a WQFN-20L 3x3 package, and operates over an extended temperature range from –40°C to 85°C.

Features

- **5.5V to 25V Input Voltage Range**
- **2V to 5.5V Output Voltage Range**
- **No Current Sense Resistor Needed**
- **5V/3.3V Linear Regulators**
- **4700ppm/°C $R_{DS(ON)}$ Current Sensing**
- **Internal Current Limit Soft-Start and Soft Discharge Output**
- **Built In OVP/UVP/OCP**
- **Selectable Operation Mode with Switcher Enable Control (RT8243A)**
- **SECFB Input Maintains Charge Pump Voltage (RT8243B/C)**
- **Power Good Indicator (RT8243B/C includes SECFB)**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook computers
- System Power Supplies
- 3- and 4- Cell Li+ Battery-Powered Device

Ordering Information

RT8243A/B/C□□

- Package Type
  QW : WQFN-20L 3x3 (W-Type)
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free)
- Pin Function With
  A : ENM
  B : SECFB
  C : SECFB, Ultrasonic Mode

Note :

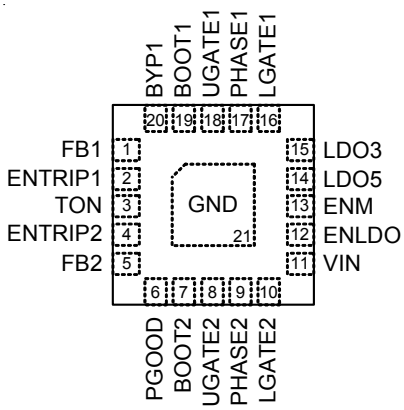
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

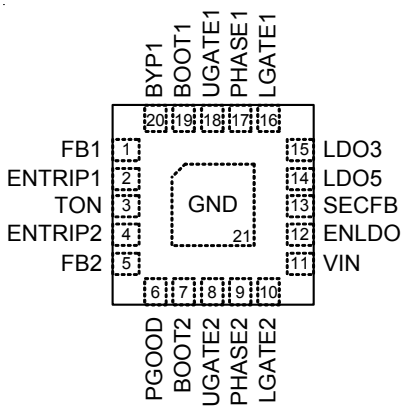
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Pin Configurations

(TOP VIEW)



RT8243A

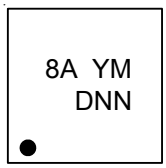


RT8243B/C

WQFN-20L 3x3

Marking Information

RT8243AZQW



8A : Product Code

YMDNN : Date Code

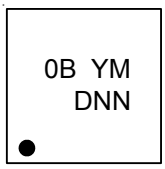
RT8243BZQW



7A : Product Code

YMDNN : Date Code

RT8243CZQW



0B : Product Code

YMDNN : Date Code

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Typical Application Circuit

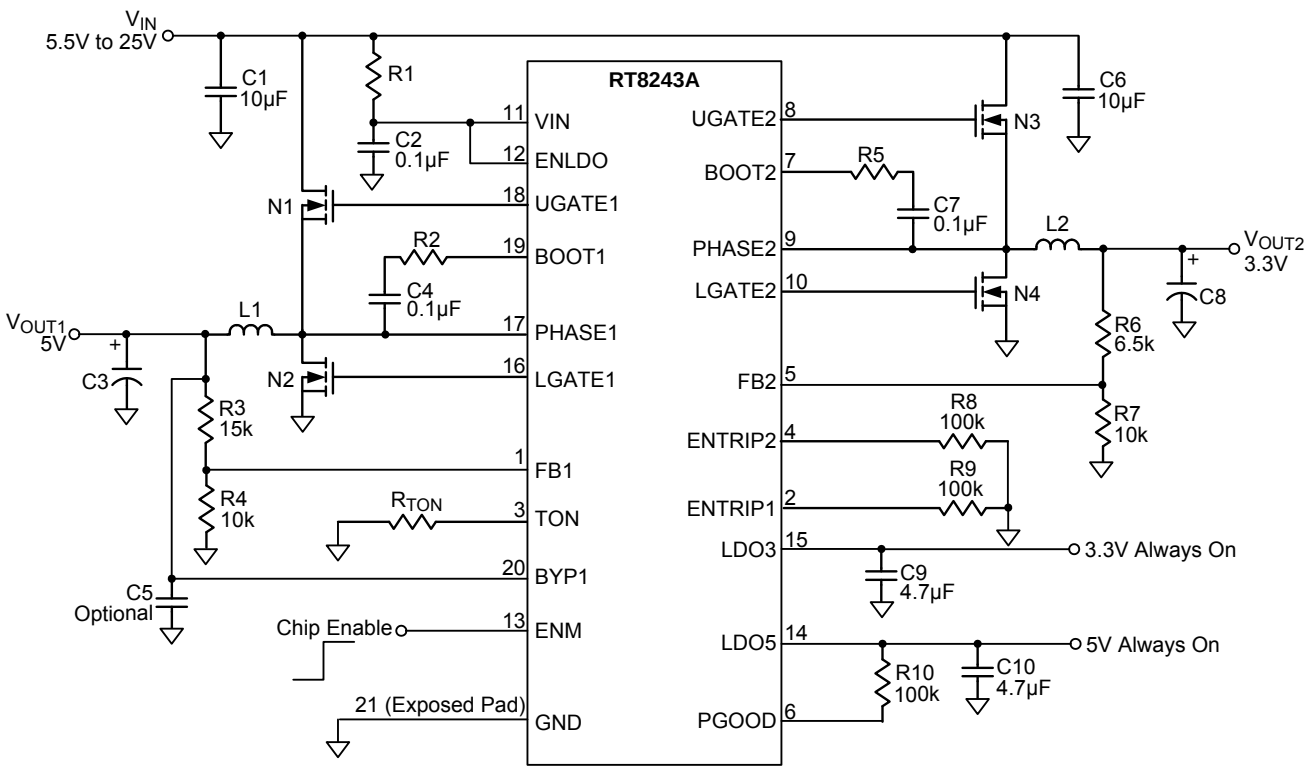


Figure 1. RT8243A NB Main Supply Typical Application Circuit

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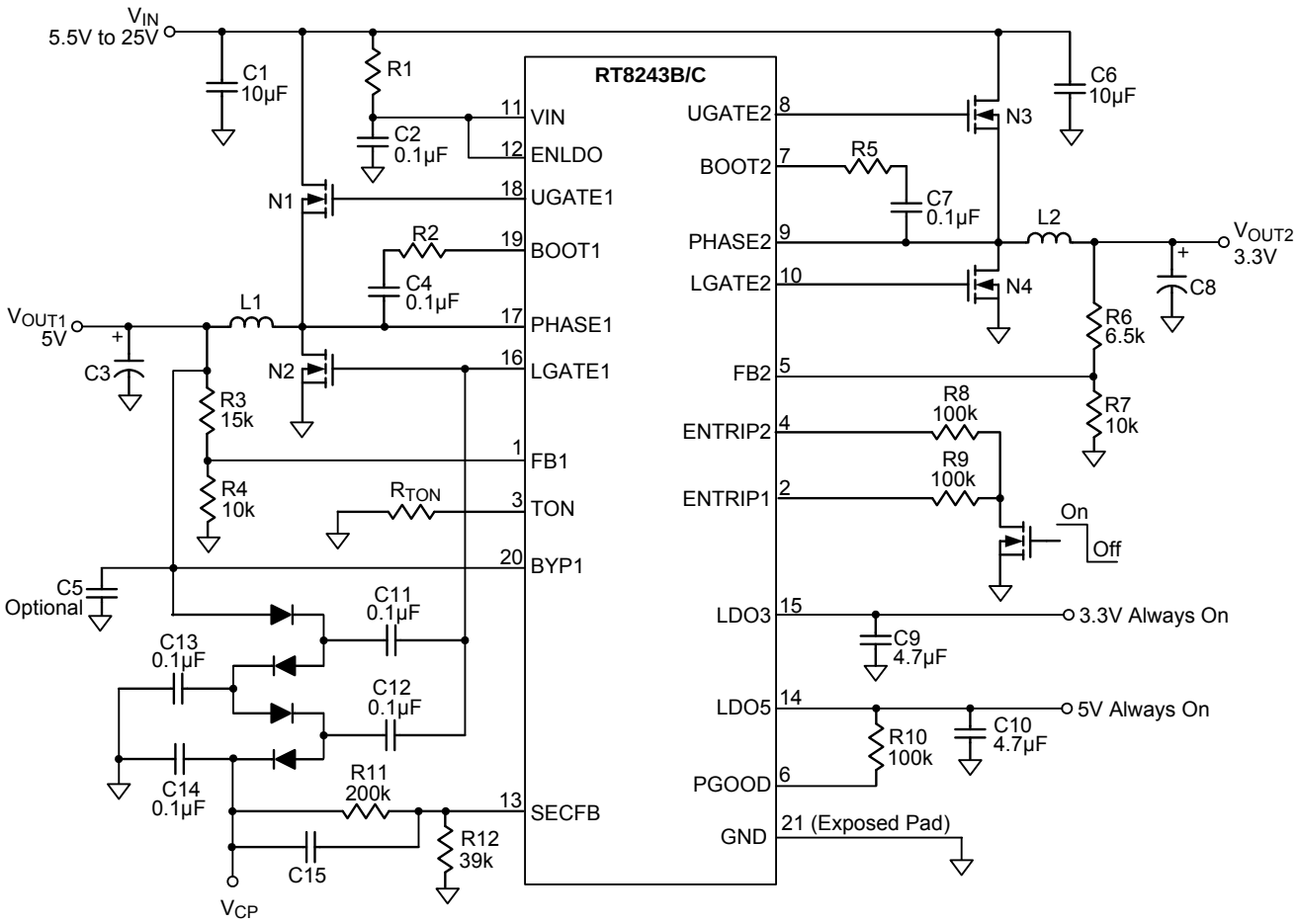


Figure 2. RT8243B/C NB Main Supply Typical Application Circuit

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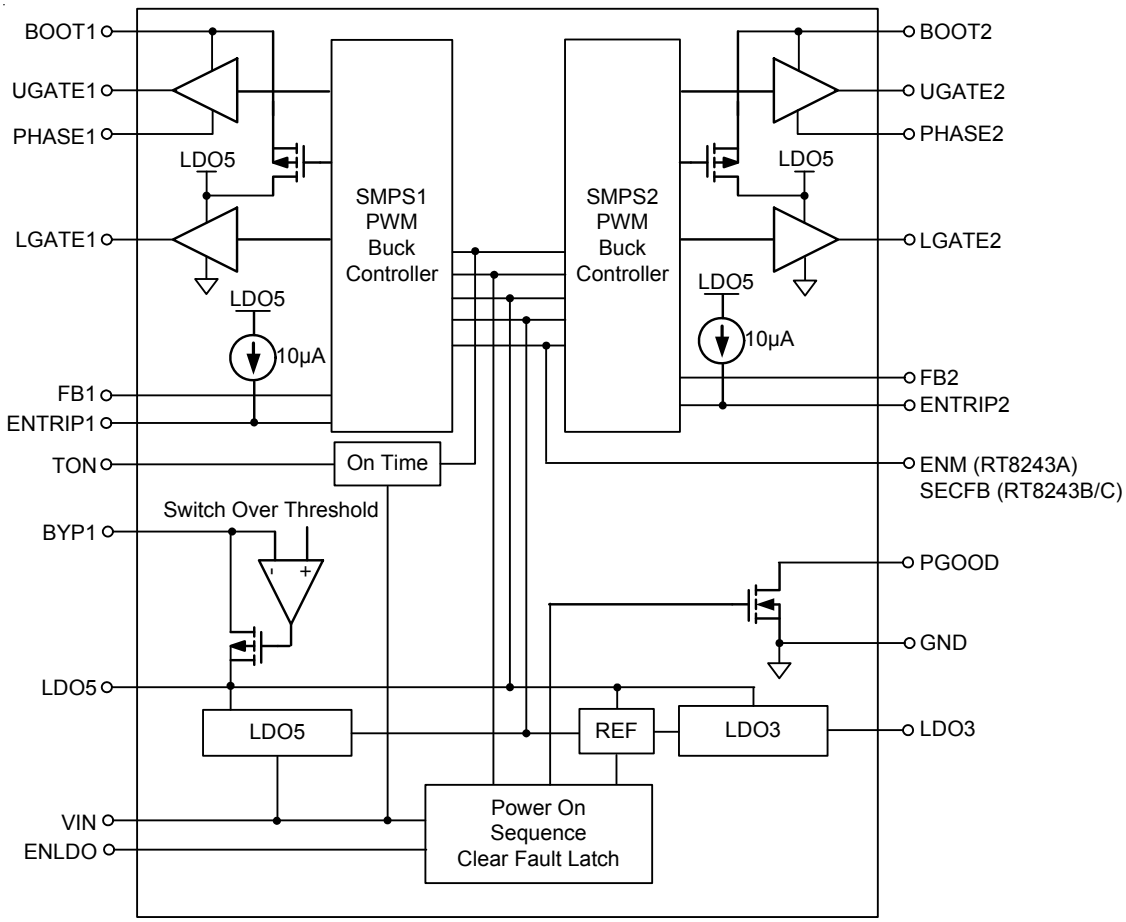
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB1	SMPS1 Feedback Input. Connect FB1 to a resistive voltage divider from SMPS1 output to GND for adjustable output from 2V to 5.5V.
2	ENTRIP1	Channel 1 Enable and Current Limit Setting Input. Connect resistor to GND to set the threshold for Channel 1 synchronous $R_{DS(ON)}$ sense. The GND-PHASE1 current limit threshold is 1/10th the voltage seen at ENTRIP1 over a 0.5V to 3V range. There is an internal 10μA current source from LDO5 to ENTRIP1. Leave ENTRIP1 floating or drive it above 4.5V to shut down channel 1.
3	TON	ON-Time/Frequency Adjustment Input. Connect to GND with 56kΩ to 100kΩ.
4	ENTRIP2	Channel 2 Enable and Current Limit Setting Input. Connect resistor to GND to set the threshold for Channel 2 synchronous $R_{DS(ON)}$ sense. The GND-PHASE2 current limit threshold is 1/10th the voltage seen at ENTRIP2 over a 0.5V to 3V range. There is an internal 10μA current source from LDO5 to ENTRIP2. Leave ENTRIP2 floating or drive it above 4.5V to shut down channel 2.
5	FB2	SMPS2 Feedback Input. Connect FB2 to a resistive voltage divider from SMPS2 output to GND for adjustable output from 2V to 5.5V.
6	PGOOD	Power Good Output for Channel 1 and Channel 2 (RT8243A).
		Power Good Output for Channel 1, Channel 2 and SECFB (RT8243B/C).
7	BOOT2	Boost Flying Capacitor Connection for SMPS2. Connect to an external capacitor according to the typical application circuits.
8	UGATE2	Upper Gate Driver Output for SMPS2. UGATE2 swings between PHASE2 and BOOT2.
9	PHASE2	Switch Node for SMPS2. PHASE2 is the internal lower supply rail for the UGATE2 high side gate driver. PHASE2 is also the current sense input for the SMPS2.
10	LGATE2	Lower Gate Drive Output for SMSP2. LGATE2 swings between GND and LDO5.
11	VIN	Supply Input for LDO5.
12	ENLDO	Master Enable Input. LDO5/LDO3 is enabled if it is within logic high level and disabled if it is less than the logic low level. Leave ENLDO floating to default enable LDO5/LDO3.
13	ENM (RT8243A)	Mode Selection with Enable Input. Pull up to LDO5 (Ultrasonic mode) or LDO3 (DEM) to turn on both switch Channels. Short to GND for shutdown.
	SECFB (RT8243B/C)	Change Pump Feedback Pin. The SECFB is used to monitor the optional external charge pump. Connect a resistive divider from the change pump output to GND to detect the output. If SECFB drops below its feedback threshold, an ultrasonic pulse occurs to refresh the charge pump driven by LGATE1 or LGATE2. If SECFB drops below its UV threshold, the switcher channels stop working and enter into discharge-mode. Pull up to LDO5 or LDO3 to disable SECFB UVP function.
14	LDO5	5V Linear Regulator Output. LDO5 is the supply voltage for the low side MOSFET driver and also the analog supply voltage for the device. Bypass a minimum 4.7μF ceramic capacitor to GND
15	LDO3	3.3V Linear Regulator Output. Bypass a minimum 4.7μF ceramic capacitor to GND.

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Pin No.	Pin Name	Pin Function
16	LGATE1	Lower Gate Driver Output for SMPS1. LGATE1 swings between GND and LDO5.
17	PHASE1	Switch Node SMPS1. PHASE1 is the internal lower supply rail for the UGATE1 high side gate driver. PHASE1 is also the current sense input for the SMPS1.
18	UGATE1	Upper Gate Driver Output for SMPS1. UGATE1 swings between PHASE1 and BOOT1.
19	BOOT1	Boost Flying Capacitor Connection for SMPS1. Connect to an external capacitor according to the typical application circuits.
20	BYP1	Switch Over Source Voltage Input for LDO5.
21 (Exposed Pad)	GND	Analog Ground and Power Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- VIN, ENLDO to GND ---------- –0.3V to 30V
- BOOTx to PHASEx
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –2.5V to 6.3V
- ENTRIPx, FBx, TON, BYP1, PGOOD, LDO5, LDO3, ENM/SECFB to GND ---------- –0.3V to 6V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - < 20ns ---------- –8V to 38V
- UGATEx to PHASEx
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-20L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  - WQFN-20L 3x3, θ_{JA} ---------- 30°C/W
  - WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 5.5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

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Electrical Characteristics

(V_{IN} = 12V, V_{ENLDO} = 5V, $V_{ENTRIPx}$ = 2V, V_{BYP1} = 5V, No Load on LDO5, LDO3, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Supply							
VIN Power On Reset		Rising Threshold		--	5.1	5.5	V
		Falling Threshold		3.5	--	4.5	
VIN Shutdown Current	I_{VIN_SHDN}	V_{ENLDO} = GND		--	20	40	μA
VIN Standby Supply Current	I_{VIN_SBY}	Both SMPS Off		--	250	350	
Quiescent Power Consumption	I_Q	Both SMPSs on, FBx = 2.1V, BYP1 = 5V, ENM = 3.3V (RT8243A)		--	5	7	mW
SMPS Output and FB Voltage							
FBx Regulation Voltage	V_{FBx}	FBx, CCM Operation		--	2	--	V
		FBx, DEM Operation		1.98	2.006	2.03	
Output Voltage Adjustable Range		SMPS1, SMPS2		2	--	5.5	V
SECFB Voltage	V_{SECFB}	RT8243B		1.92	2	2.08	
On Time							
ON-Time Pulse Width	t_{UGATEx}	V_{IN} = 20V, R_{TON} = 56kΩ	V_{PHASE1} = 2V	--	256	--	ns
			V_{PHASE2} = 2V	--	220	--	
Minimum Off-Time	t_{LGATEx}	V_{FBx} = 1.8V		--	--	400	ns
Frequency Range	f_{SMPS1}	SMPS1 Operating Frequency		200	--	400	kHz
	f_{SMPS2}	SMPS2 Operating Frequency		233	--	466	
Ultrasonic Mode Frequency	f_{ASM}	RT8243C, V_{PHASEx} = 50mV		25	--	--	kHz
Soft-Start							
Soft-Start Time	t_{SSx}	Zero to 200mV Current Limit Threshold from ENTRIPx Enable		--	2	--	ms
Current Sense							
Current Limit Current Source	$I_{ENTRIPx}$	$V_{ENTRIPx}$ = 0.9V		9.4	10	10.6	μA
Temperature Coefficient of $I_{ENTRIPx}$		On The Basis of 25°C		--	4700	--	ppm/°C
Current Limit Adjustment Range		$V_{ENTRIPx}$ = $I_{ENTRIPx}$ x $R_{ENTRIPx}$		0.5	--	2.7	V
Current Limit Threshold	$V_{ENTRIPx}$	GND – PHASEx, $V_{ENTRIPx}$ = 2V		180	200	225	mV
Zero-Current Threshold	V_{ZC}	GND – PHASEx, FBx = 2.1V		--	3	--	mV
Internal Regulator and Reference							
LDO5 Output Voltage	V_{LDO5}	V_{BYP1} = 0V, I_{LDO5} < 100mA		4.9	5	5.1	V
		V_{BYP1} = 0V, I_{LDO5} < 100mA , 6.5V < V_{IN} < 25V		4.75	--	5.25	
		V_{BYP1} = 0V, I_{LDO5} < 50mA, 5.5V < V_{IN} < 25V		4.75	--	5.25	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LDO5 Output Current	I_{SHORT5}	V_{BYP1} = 0V, V_{LDO5} = 4.5V	150	225	300	mA
5V Switchover Threshold	V_{BYP1TH}	Falling Edge, Rising Edge with FB1 Regulation Point	4.53	4.66	4.79	V
5V Switch $R_{DS(ON)}$	R_{BYPSW}	V_{BYP1} = 5V, I_{LDO5} = 50mA	--	1.5	3	Ω
LDO3 Output Voltage	V_{LDO3}	V_{BYP1} = 0V, I_{LDO3} < 100mA	3.234	3.3	3.366	V
		V_{BYP1} = 5V, I_{LDO3} < 100mA	3.2	3.3	3.46	
LDO3 Output Current	I_{SHORT3}	V_{BYP1} = 0V, V_{LDO3} = 2.9V	80	150	260	mA
UVLO						
LDO5 UVLO Threshold	V_{UVLO5}	Rising Edge	--	4.35	4.5	V
		Falling Edge	3.9	4.05	4.2	
LDO3 UVLO Threshold	V_{UVLO3}	Both SMPS Off	1.9	2.2	2.5	
Power Good						
PGOOD Threshold	V_{PGOOD}	PGOOD Detect, Rising edge with soft-start delay time. Hysteresis = 2.5%	−14	−10	−6	%
PGOOD Propagation Delay	t_{PD_PGOOD}	Falling Edge	--	5	--	μs
PGOOD Leakage Current	I_{LK_PGOOD}	High State, Forced to 5.5V	--	--	1	μA
PGOOD Output Low Voltage	V_{SINK_PGOOD}	I_{SINK} = 4mA	--	--	0.4	V
SECFB Power Good Threshold	V_{SFB_PGOOD}	SECFB with Respect to 2V (RT8243B/C)	40	50	60	%
Fault Detection						
Over Voltage Protection Trip Threshold	V_{OVP}	OVP Detect, FBx Rising Edge	108	112	116	%
Over Voltage Protection Propagation Delay	t_{DLY_OVP}	Rising Edge	--	5	--	μs
Under Voltage Protection Trip Threshold	V_{UVP}	UVP Detect, FBx Falling Edge.	53	58	63	%
	V_{SFB_UVP}	UVP Detect, SECFB Falling Edge.	0.8	--	1.2	V
Under Voltage Protection Shutdown Blanking Time	t_{SSHx}	From ENTRIPx or ENM Enable	--	5	--	ms
Thermal Shutdown						
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	10	--	°C
Logic Input						
ENTRIPx Input Voltage	$V_{ENTRIPx}$	Clear Fault Level/SMPSx Off Level	4.5	--	--	V
ENLDO Input Voltage	V_{ENLDO}	Rising Edge Threshold	1.2	1.6	2	V
		Falling Edge Threshold	0.9	0.95	1	
		When ENLDO is Floating (Default Enable)	2.1	--	--	
ENM Input Voltage (RT8243A)	V_{ENM}	Clear Fault Level/SMPSs Off Level	--	--	0.8	V
		SMPSs On, DEM Operation	2.3	--	3.6	
		SMPSs On, Ultrasonic Mode Operation	4.5	--	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{FBx}	V_{FBx} = 0V or 5V	–1	--	1	μA
	I_{P13}	ENM/SECFB = 0V or 5V	–1	--	1	
	I_{ENLDO}	ENLDO = 0V or 5V	–1	--	3	
Internal BOOT Switch						
Internal Boost Charging Switch On-Resistance	R_{BOOTx}	LDO5 to BOOTx, 10mA	--	--	90	Ω
Power MOSFET Drivers						
UGATEx On-Resistance	$R_{UGATEsr}$	Source, $V_{BOOTx} - V_{UGATEx}$ = 0.1V	--	5	8	Ω
	$R_{UGATEsk}$	Sink, $V_{UGATEx} - V_{PHASEx}$ = 0.1V	--	2	4	
LGATEx On-Resistance	$R_{LGATEsr}$	Source, $V_{LDO5} - V_{LGATEx}$ = 0.1V	--	5	8	Ω
	$R_{LGATEsk}$	Sink, V_{LGATEx} = 0.1V	--	1.5	3	
Dead Time	$t_{LGATERx}$	UGATEx Off to LGATEx On	--	30	--	ns
	$t_{UGATERx}$	LGATEx Off to UGATEx On	--	40	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

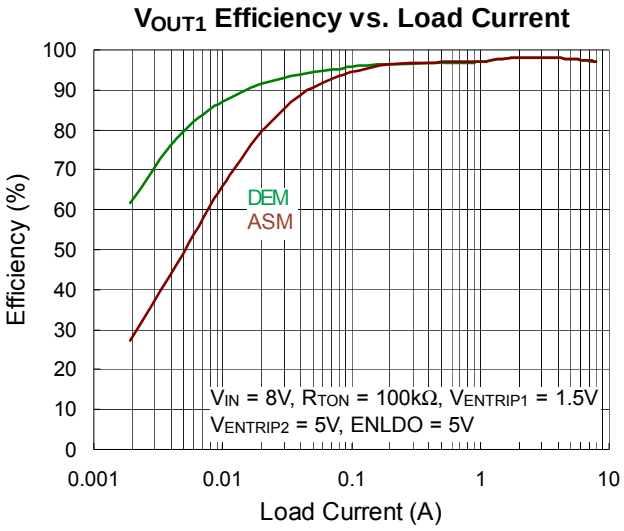
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

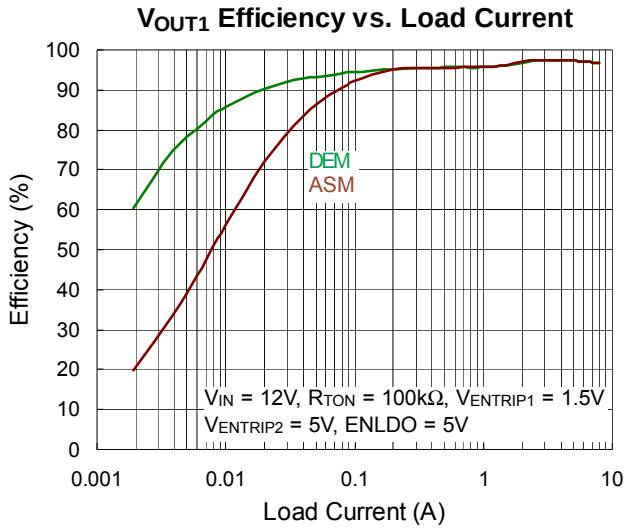
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

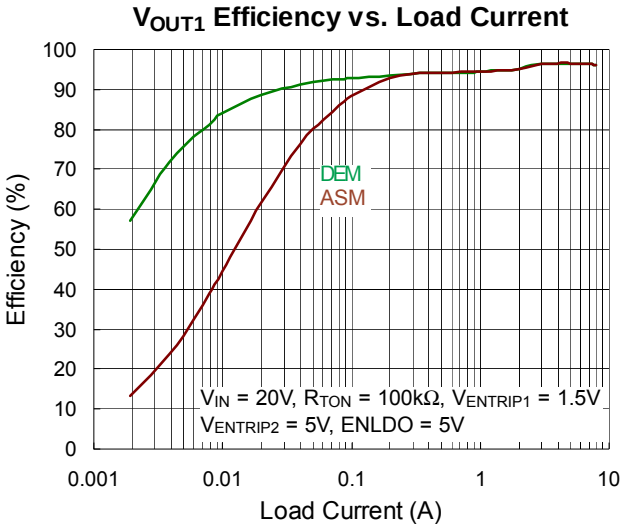
Note 4. The device is not guaranteed to function outside its operating conditions.

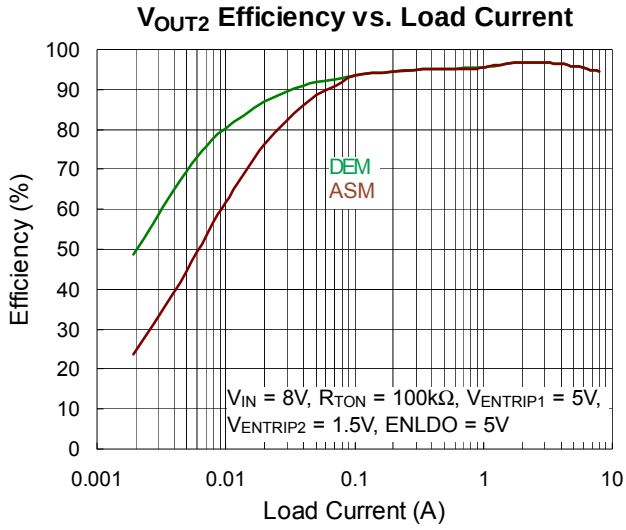
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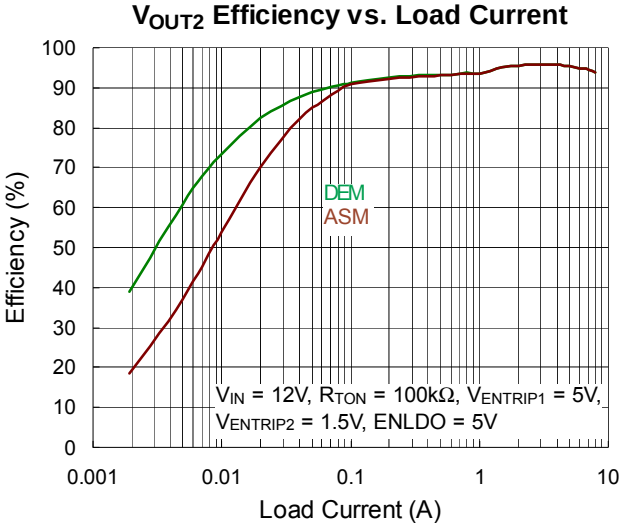
Typical Operating Characteristics

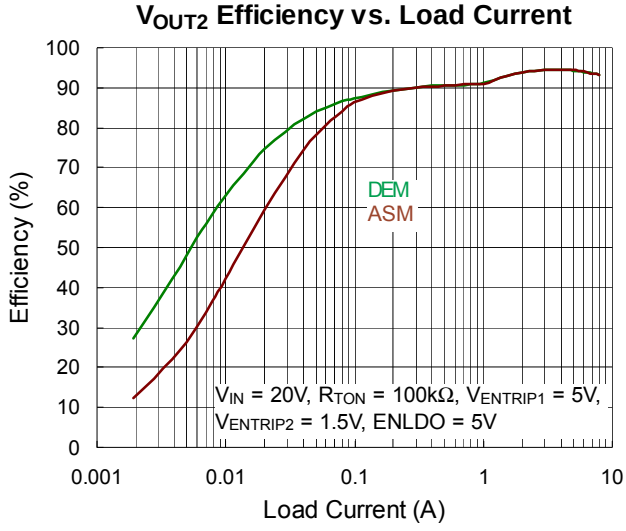






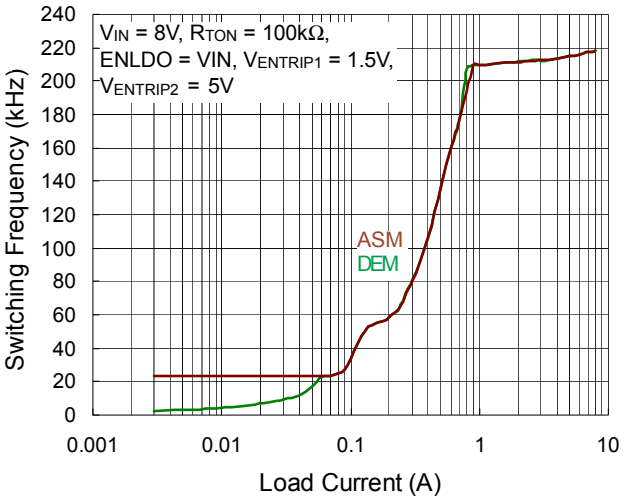




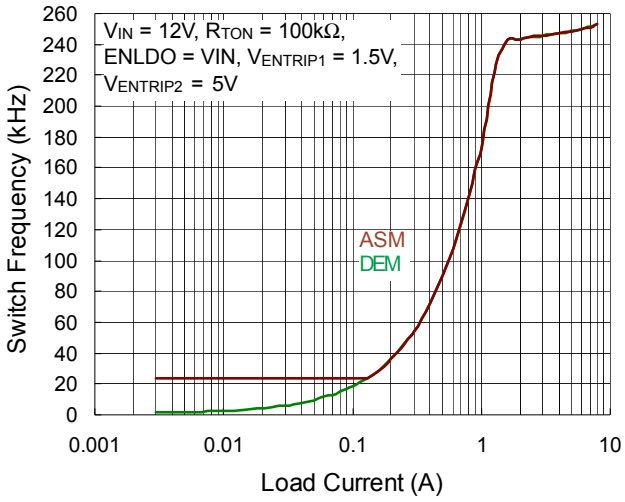


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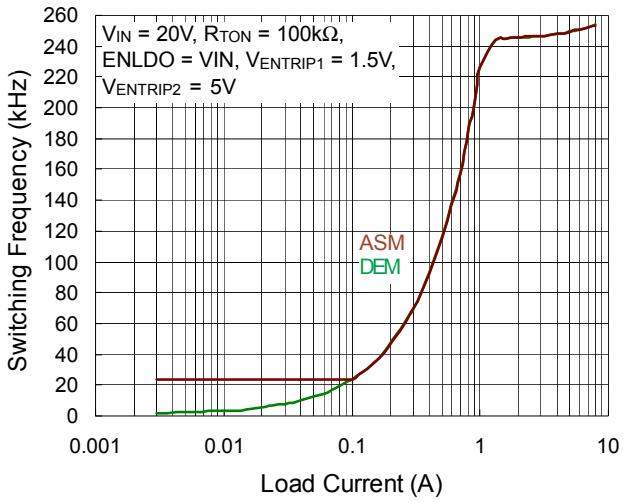
V_{OUT1} Switching Frequency vs. Load Current



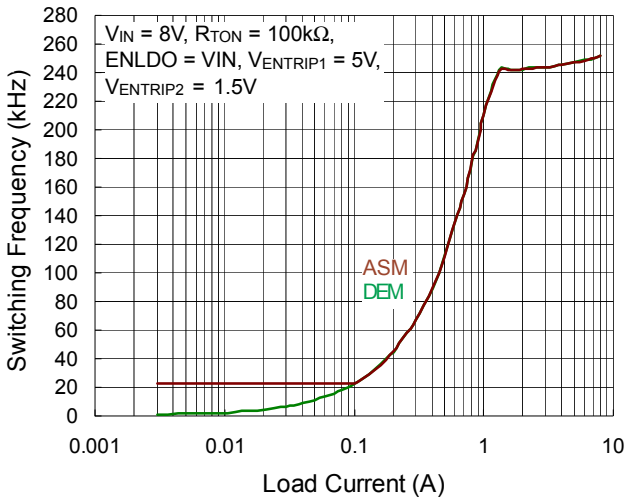
V_{OUT1} Switching Frequency vs. Load Current



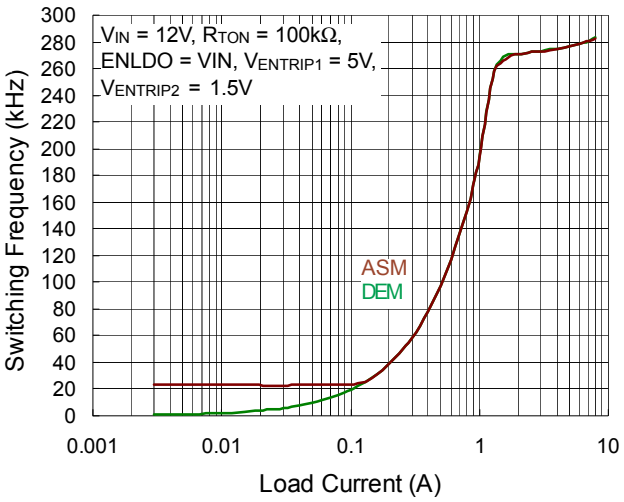
V_{OUT1} Switching Frequency vs. Load Current



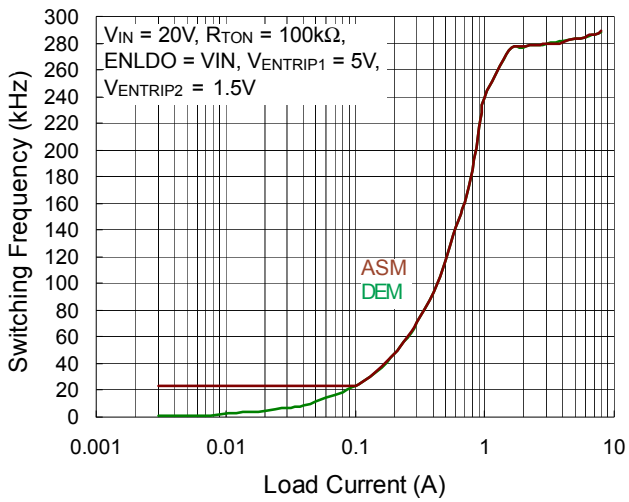
V_{OUT2} Switching Frequency vs. Load Current



V_{OUT2} Switching Frequency vs. Load Current

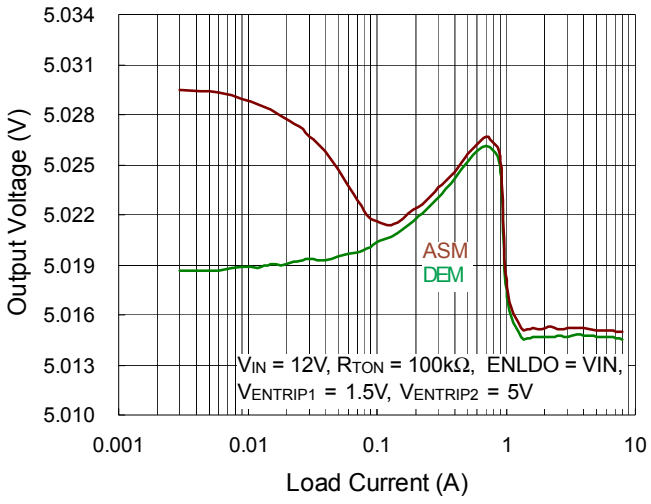


V_{OUT2} Switching Frequency vs. Load Current

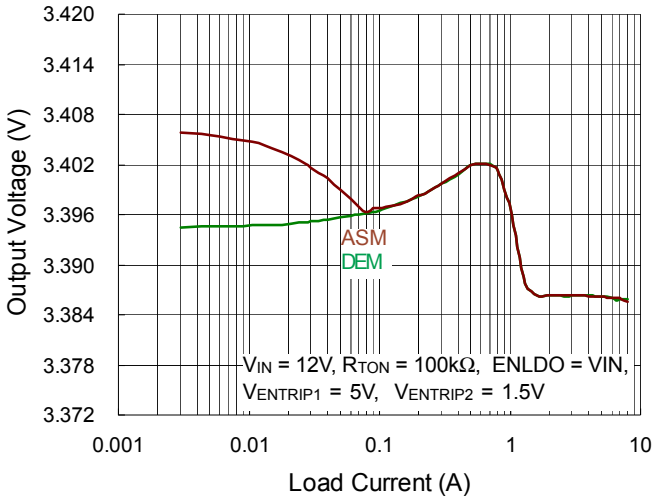


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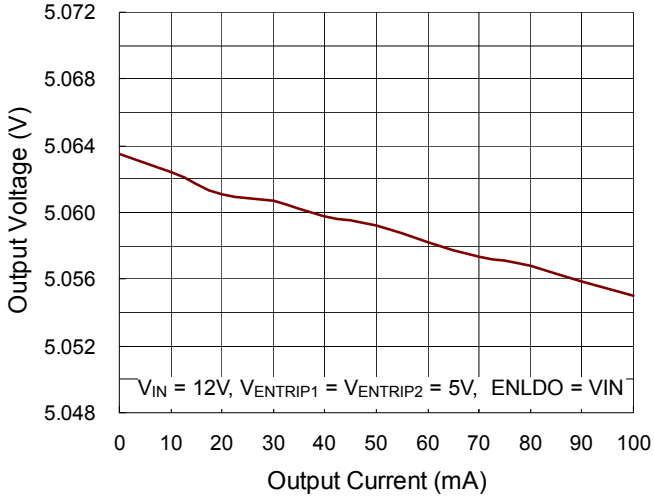
V_{OUT1} Output Voltage vs. Load Current



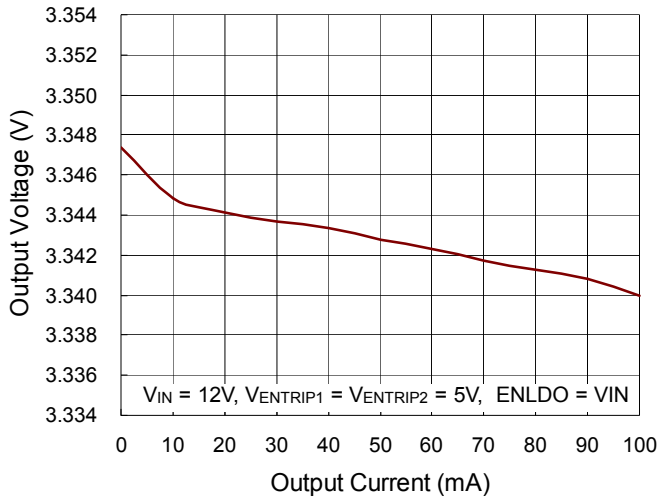
V_{OUT2} Output Voltage vs. Load Current



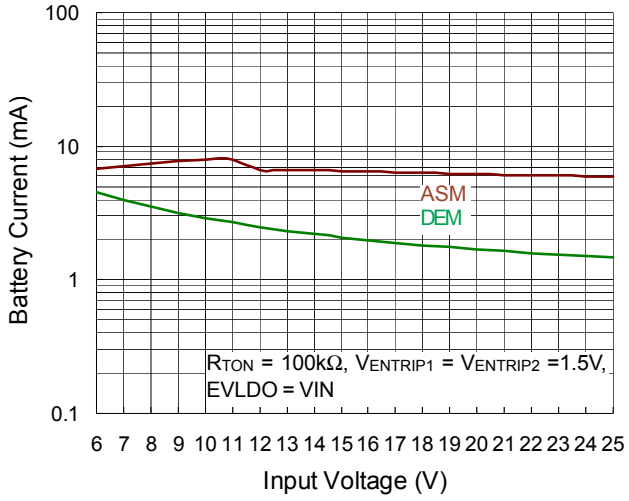
LDO5 Output Voltage vs. Output Current



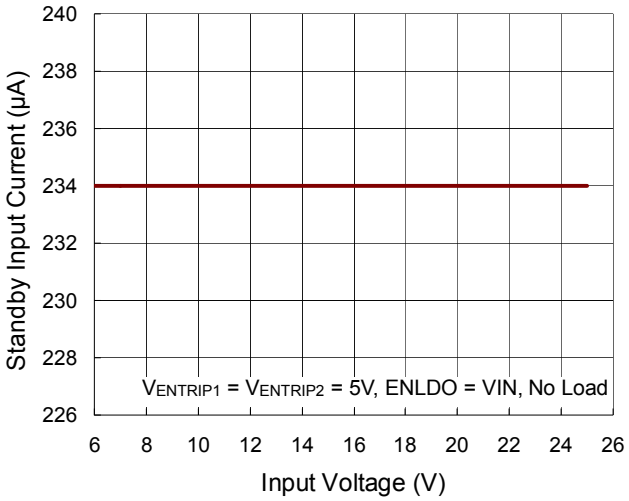
LDO3 Output Voltage vs. Output Current



No Load Battery Current vs. Input Voltage

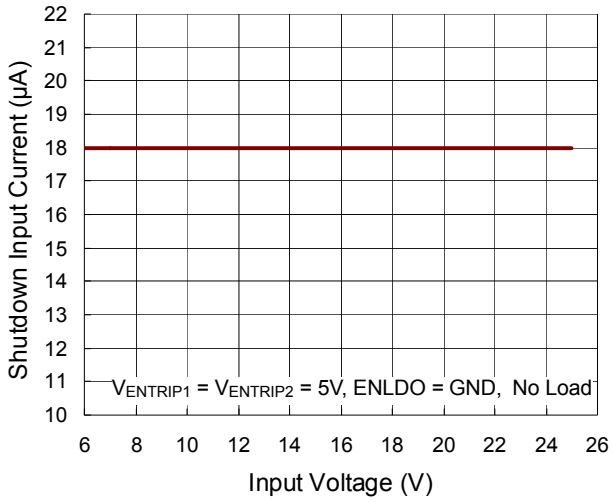


Standby Input Current vs. Input Voltage

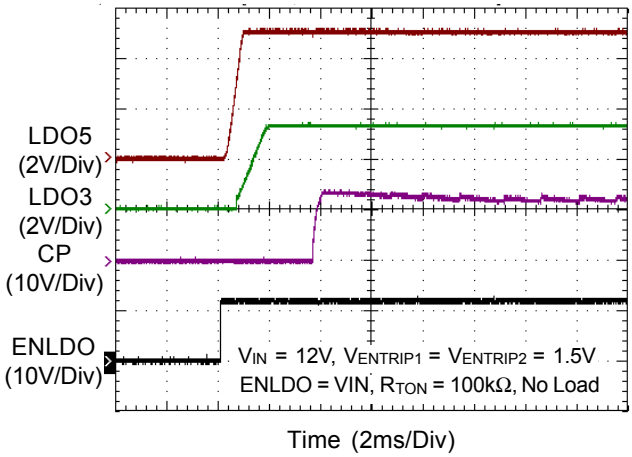


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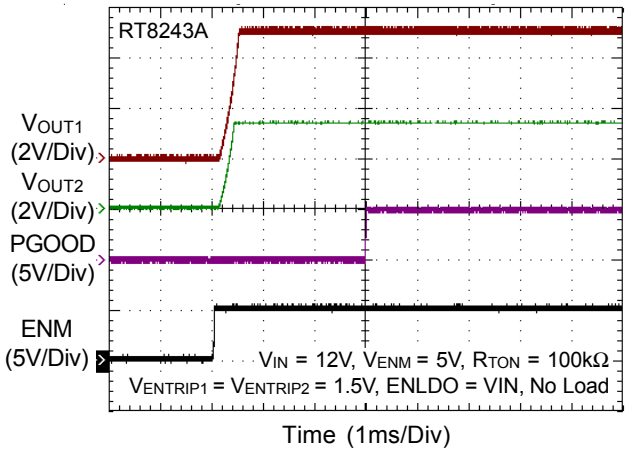
Shutdown Input Current vs. Input Voltage



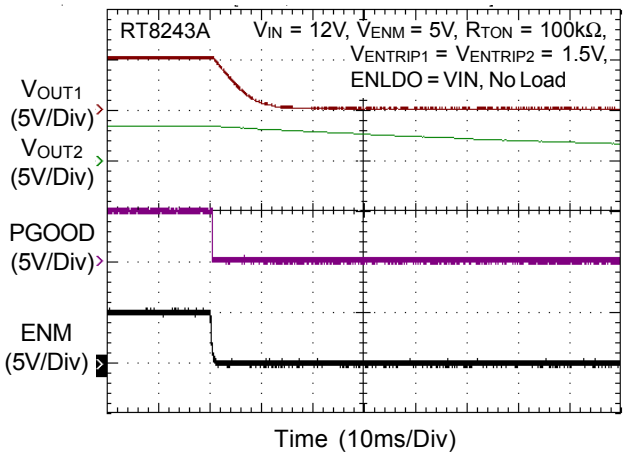
Power On from ENLDO



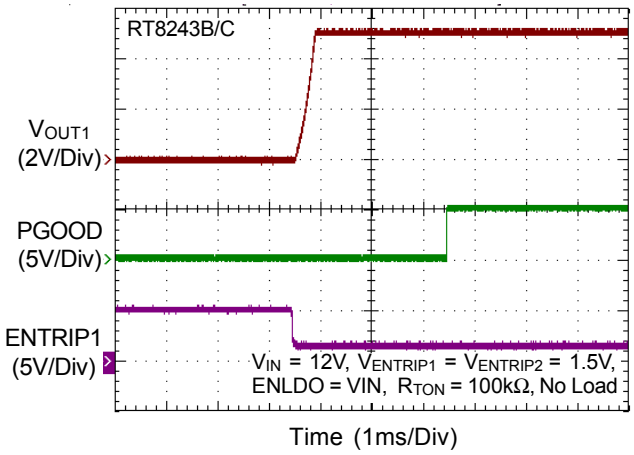
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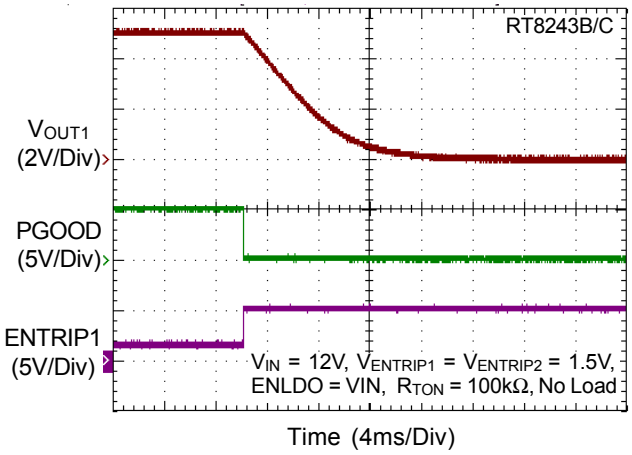
Power Off from ENM



Power On from ENTRIP1

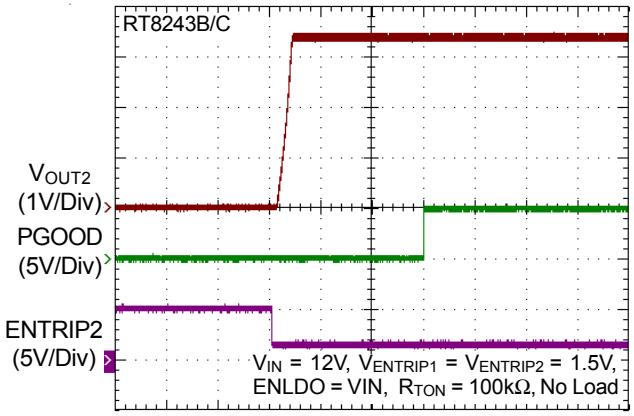


Power Off from ENTRIP1

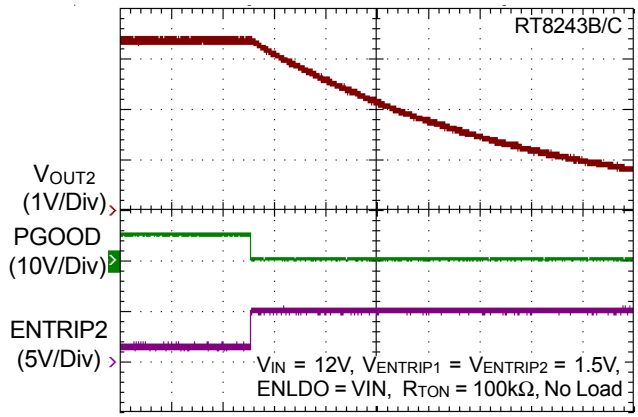


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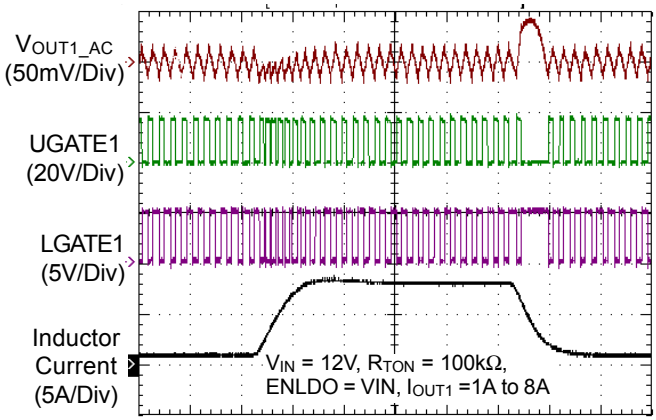
Power On from ENTRIP2



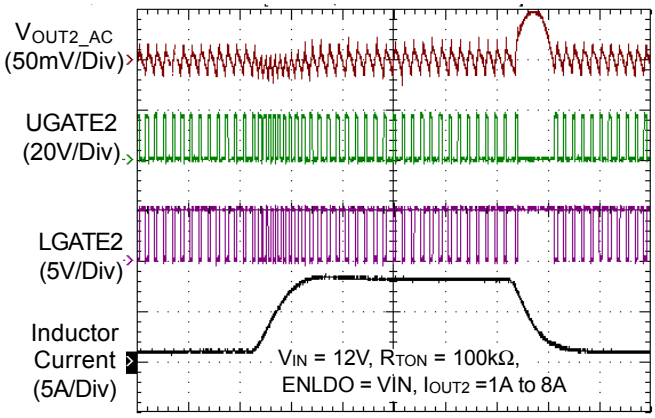
Power Off from ENTRIP2



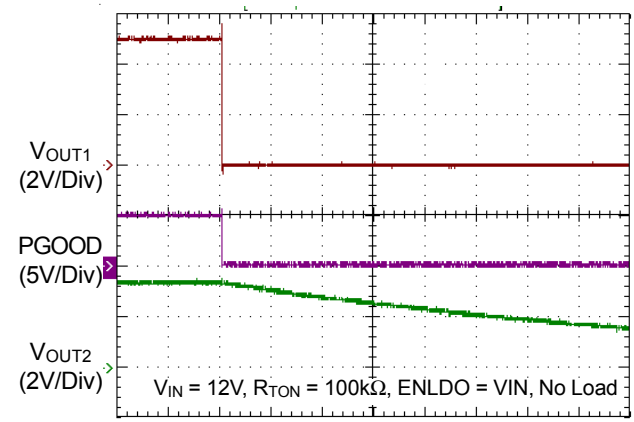
VOUT1 DEM-MODE Load Transient Response



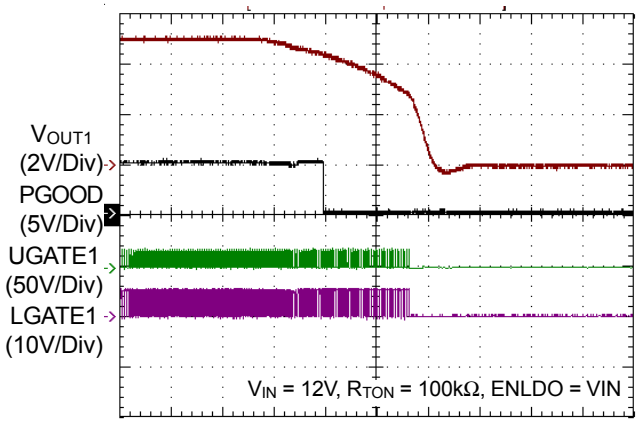
VOUT2 DEM-MODE Load Transient Response



OVP



UVP



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Application Information

The RT8243A/B/C is a dual, Mach Response™ DRV™ mode synchronous buck controller targeted for notebook system power supply solutions. Richtek's Mach Response™ technology provides fast response to load steps. The topology circumvents the poor load transient timing problems of fixed frequency current mode PWMs while avoiding the problems caused by widely varying switching frequency in conventional constant on-time and constant off-time PWM schemes. A special adaptive on-time control trades off the performance and efficiency over wide input voltage range. The RT8243A/B/C includes 5V (LDO5) and 3.3V (LDO3) linear regulators. The LDO5 linear regulator steps down the battery voltage to supply both internal circuitry and gate drivers. The synchronous switch gate drivers are directly powered by LDO5. When V_{OUT1} rises above 4.66V, an automatic circuit disconnects the linear regulator and allows the device to be powered by V_{OUT1} via the BYP1 pin.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current sense resistor, so that the output ripple voltage provides the PWM ramp signal. Referring to the RT8243A/B/C's Function Block Diagram, the synchronous high side MOSFET will be turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this one-shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (400ns typ.). The on-time one-shot will be triggered if the error comparator is high, the low side switch current is below the current limit threshold, and the minimum off-time one-shot has timed out.

PWM Frequency and On-time Control

For each specific input voltage range, the Mach Response™ control architecture runs with pseudo constant frequency by feed forwarding the input and output voltage into the on-time one-shot timer. The high side switch on-time is inversely proportional to the input voltage as measured by V_{IN} and proportional to the output voltage. There are two benefits of a constant switching frequency. First, the frequency can be selected to avoid noise sensitive regions such as the 455kHz IF band. Second, the inductor ripple current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The frequency for 3V SMPS is set higher than the frequency for 5V SMPS. This is done to prevent audio frequency "beating" between the two sides, which switch asynchronously for each side. The TON pin is connected to GND through the external resistor, R_{TON}, to set the switching frequency.

The RT8243A/B/C adaptively changes the operation frequency according to the input voltage. Higher input voltage usually comes from an external adapter, so the RT8243A/B/C operates with higher frequency to have better performance. Lower input voltage usually comes from a battery, so the RT8243A/B/C operates with lower switching frequency for lower switching losses. For a specific input voltage range, the switching cycle period is given by :

For $5.5V < V_{IN} < 6.5V$:

$$t_{S1} = 61.28p \times R_{TON}$$

$$t_{S2} = 44.43p \times R_{TON}$$

For $6.5V < V_{IN} < 12V$:

$$t_{S1} = 51.85p \times R_{TON}$$

$$t_{S2} = 44.43p \times R_{TON}$$

For $12V < V_{IN} < 25V$:

$$t_{S1} = 45.75p \times R_{TON}$$

$$t_{S2} = 39.2p \times R_{TON}$$

The on-time guaranteed in the Electrical Characteristics table is influenced by switching delays in the external high side power MOSFET. Two external factors that influence switching frequency accuracy are resistive drops in the two conduction loops (including inductor and PC board resistance) and the dead time effect. These effects are the largest contributors to the change of frequency with changing load current. The dead time effect increases

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the effective on-time by reducing the switching frequency as one or both dead times. It occurs only in PWM mode when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes PHASEx to go high earlier than normal, hence extending the on-time by a period equal to the low to high dead time. For loads above the critical conduction point, the actual switching frequency is :

$$f = (V_{OUT} + V_{DROP1}) / (t_{ON} \times (V_{IN} + V_{DROP1} - V_{DROP2}))$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path; and t_{ON} is the on-time calculated by the RT8243A/B/C.

Operation Mode Selection

The RT8243A/B supports two operation modes : Diode Emulation Mode and Ultrasonic Mode. The RT8243C only supports Ultrasonic Mode. The operation mode can be set via the ENM pin for RT8243A or SECFB pin for RT8243B.

Table 1. Operation Mode Setting

Part Number	RT8243A	RT8243B	RT8243C
Pin Name	ENM	SECFB	SECFB
Pin-13 Voltage Range	Mode State		
4.5V to 5V	ASM	ASM	ASM
2.3V to 3.6V	DEM	DEM	ASM
1.2V to 1.8V	ASM	ASM	ASM
Below 0.8V	Shutdown	UVP	UVP

Diode Emulation Mode

In Diode Emulation Mode, the RT8243A/B automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial negative current to flow when the inductor free wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next "ON" cycle. The on-time is kept the same as that in the heavy load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation is shown in Figure 3. and can be calculated as follows :

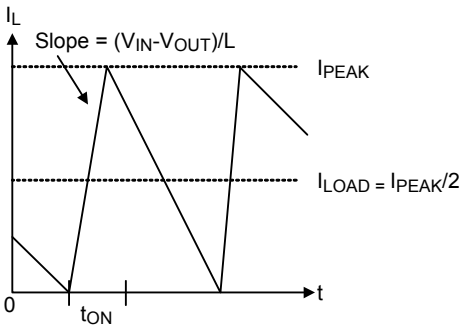


Figure 3. Boundary condition of CCM/DEM

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

The switching waveforms may appear noisy and asynchronous when light loading causes diode emulation operation. This is normal and results in high efficiency. Trade offs in PFM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

Ultrasonic Mode

The RT8243A/B/C activates a unique type of Diode Emulation Mode with a minimum switching frequency of 25kHz, called Ultrasonic Mode. This mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In Ultrasonic Mode, the low side switch gate driver signal is "OR"ed with an internal oscillator (>25kHz). Once the internal oscillator is triggered, the ultrasonic controller pulls LGATEx high and turns on the

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low side MOSFET to induce a negative inductor current. After the output voltage falls below the reference voltage, the controller turns off the low side MOSFET (LGATEx pulled low) and triggers a constant on-time (UGATEx driven high). When the on-time has expired, the controller re-enables the low side MOSFET until the controller detects that the inductor current dropped below the zero crossing threshold.

Linear Regulators (LDOx)

The RT8243A/B/C includes 5V (LDO5) and 3.3V (LDO3) linear regulators. The regulators can supply up to 100mA for external loads. Bypass LDOx with a minimum 4.7µF ceramic capacitor. When V_{OUT1} is higher than the switch over threshold (4.66V), an internal 1.5Ω P-MOSFET switch connects BYP1 to the LDO5 pin while simultaneously disconnects the internal linear regulator.

Current Limit Setting (ENTRIPx)

The RT8243A/B/C has cycle-by-cycle current limit control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASEx is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 4). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and battery and output voltage.

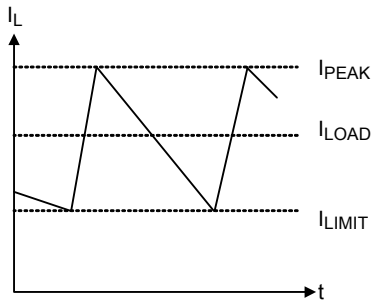


Figure 4. "Valley" Current Limit

The RT8243A/B/C uses the on resistance of the synchronous rectifier as the current sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The R_{ILIM} resistor between the ENTRIPx pin and GND sets the current limit threshold. The resistor, R_{ILIM}, is connected to a current source from ENTRIPx which is 10µA (typ.) at room temperature. The current source has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$. When the voltage drop across the sense resistor or low side MOSFET equals 1/10 the voltage across the R_{ILIM} resistor, positive current limit will be activated. The high side MOSFET will not be turned on until the voltage drop across the MOSFET falls below 1/10 the voltage across the R_{ILIM} resistor.

Choose a current limit resistor according to the following equation :

$V_{ILIM} = (R_{ILIM} \times 10\mu A) / 10 = I_{ILIM} \times R_{DS(ON)}$

$R_{ILIM} = (I_{ILIM} \times R_{DS(ON)}) \times 10 / 10\mu A$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current sense signal at PHASEx and GND. Mount or place the IC close to the low side MOSFET.

Charge Pump (SECFB)

The external 14V charge pump is driven by LGATEx. When LGATEx is low, C1 will be charged by V_{OUT1} through D1. C1 voltage is equal to V_{OUT1} minus the diode drop. When LGATEx becomes high, C1 transfers the charge to C2 through D2 and charges C2 voltage to V_{LGATEX} plus C1 voltage. As LGATEx transitions low on the next cycle, C3 is charged to C2 voltage minus a diode drop through D3. Finally, C3 charges C4 through D4 when LGATEx switches high. Thus, the total charge pump voltage, V_{CP}, is :

$V_{CP} = V_{OUT1} + 2 \times V_{LGATEx} - 4 \times V_D$

where V_{LGATEx} is the peak voltage of the LGATEx driver which is equal to LDO5 and V_D is the forward voltage dropped across the Schottky diode.

The SECFB pin in the RT8243B/C is used to monitor the charge pump via a resistive voltage divider to generate approximately 14V DC voltage and the clock driver uses V_{OUT1} as its power supply. In the event where SECFB drops below its feedback threshold, an ultrasonic pulse will occur to refresh the charge pump driven by LGATEx. If there's an overload on the charge pump in which SECFB can not reach more than its feedback threshold, the controller will enter Ultrasonic Mode. Special care should be taken to ensure that enough normal ripple voltage is present on each cycle to prevent charge pump shutdown.

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The robustness of the charge pump can be increased by reducing the charge pump decoupling capacitor and placing a small ceramic capacitor, C_F (47pF to 220pF), in parallel with the upper leg of the SECFB resistor feedback network, R_{CP1}, as shown below in Figure 5.

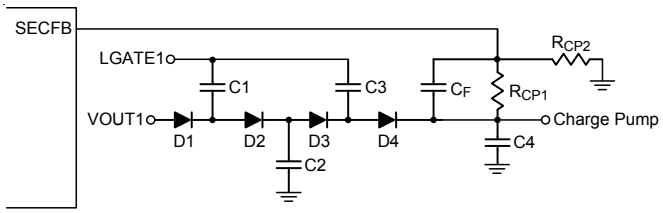


Figure 5. Charge pump circuit connected to SECFB

MOSFET Gate Driver (UGATEx, LGATEx)

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from the LDO5 supply. The average drive current is also calculated by the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOTx and PHASEx pins. A dead time to prevent shoot through is internally generated from high side MOSFET off to low side MOSFET on and low side MOSFET off to high side MOSFET on.

The low side driver is designed to drive high current low $R_{DS(ON)}$ N-MOSFET(s). The internal pull down transistor that drives LGATEx low is robust, with a 1.5Ω typical on-resistance. A 5V bias voltage is delivered from the LDO5 supply. The instantaneous drive current is supplied by an input capacitor connected between LDO5 and GND.

For high current applications, some combinations of high and low side MOSFETs may cause excessive gate drain coupling, which leads to efficiency killing, EMI producing, shoot through currents. This is often remedied by adding a resistor in series with BOOTx, which increases the turn on time of the high side MOSFET without degrading the turn-off time. See Figure 6.

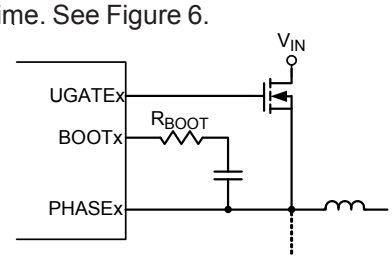


Figure 6. Increasing the UGATEx Rise Time

Soft-Start

The RT8243A/B/C provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, the internal current limit circuit gradually ramps up the inductor current from zero. The maximum current limit value is set externally as described in previous section. The soft-start time is determined by the current limit level and output capacitor value. The current limit threshold ramp up time is typically 2ms from zero to 200mV after ENTRIPx is enabled. A unique PWM duty limit control that prevents output over voltage during soft-start period is designed specifically for FBx floating.

UVLO Protection

The RT8243A/B/C has LDO5 under voltage lock out protection (UVLO). When the LDO5 voltage is lower than 4.05V (typ.) and the LDO3 voltage is lower than 2.2V (typ.), both switch power supplies are shut off. This is a non-latch protection.

Power Good Output (PGOOD)

PGOOD is an open-drain type output and requires a pull up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. It is released when both output voltages are above 90% of the nominal regulation point for RT8243A. For RT8243B/C, besides requiring both output voltages to be above 90% of nominal regulation point, the SECFB threshold must also be above 50% of nominal regulation point in order for PGOOD to be released. The PGOOD signal goes low if either output turns off or is 10% below its nominal regulation point.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage. If the output voltage exceeds 12% of its set voltage threshold, the over voltage protection is triggered and the LGATEx low side gate drivers are forced high. This activates the low side MOSFET switch, which rapidly discharges the output capacitor and pulls the input voltage downward.

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The RT8243A/B/C is latched once OVP is triggered and can only be released by either toggling ENLDO, ENTRIPx or cycling VIN. There is a 5μs delay built into the over voltage protection circuit to prevent false transition.

Note that latching LGATEx high will cause the output voltage to dip slightly negative due to previously stored energy in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the over voltage condition is caused by a short in high side switch, turning the low side MOSFET on 100% will create an electrical short between the battery and GND, hence blowing the fuse and disconnecting the battery from the output.

Output Under voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage. If the output is less than 58% of its set voltage threshold, the under voltage protection will be triggered and then both UGATEx and LGATEx gate drivers will be forced low. The UVP is ignored for at least 5ms (typ.) after a start up or a rising edge on ENTRIPx. Toggle ENTRIPx or cycle VIN to reset the UVP fault latch and restart the controller.

Thermal Protection

The RT8243A/B/C features thermal shutdown to prevent damage from excessive heat dissipation. Thermal shutdown occurs when the die temperature exceeds 150°C. All internal circuitry is inactive during thermal shutdown. The RT8243A/B/C triggers thermal shutdown if LDOx is not supplied from V_{OUTx}, while input voltage on VIN and drawing current from LDOx are too high. Nevertheless, even if LDOx is supplied from V_{OUTx}, overloading LDOx can cause large power dissipation on automatic switches, which may still result in thermal shutdown.

Discharge Mode (Soft Discharge)

When ENTRIPx is low and a transition to standby or shutdown mode occurs, or the output under voltage fault latch is set, the output discharge mode will be triggered. During discharge mode, an internal switch creates a path for discharging the output capacitors' residual charge to GND.

Shutdown Mode

SMPS1, SMPS2, LDO3 and LDO5 all have independent enabling control. Drive ENLDO, ENTRIP1 and ENTRIP2 below the precise input falling edge trip level to place the RT8243A/B/C in its low power shutdown state. The RT8243A/B/C consumes only 20μA of input current while in shutdown. When shutdown mode is activated, the reference turns off. The accurate 0.95V falling edge threshold on ENLDO can be used to detect a specific analog voltage level and to shutdown the device. Once in shutdown, the 1.6V rising edge threshold activates, providing sufficient hysteresis for most applications.

Power Up Sequencing and On/Off Controls (ENTRIPx, ENM)

ENTRIP1 and ENTRIP2 control SMPS power up sequencing. When the RT8243A/B/C is applied in the single channel mode, ENTRIPx disables the respective output when ENTRIPx voltage rises above 4.5V. Furthermore, when the RT8243A is applied in the dual channel mode, the outputs are enabled when ENM voltage rises above 2.3V.

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Table1. Operation Mode Truth Table

Mode	Condition	Comment
Power Up	LDOx < UVLO threshold	Transitions to discharge mode after VIN POR and after REF becomes valid. LDO5 and LDO3 remain active.
Run	ENLDO = high, V_{OUT1} or V_{OUT2} are enabled	Normal Operation.
Over Voltage Protection	Either output >112% of the nominal level.	LGATEx is forced high. LDO3 and LDO5 are active. Exit by VIN POR or by toggling ENLDO, ENTRIPx, and ENM.
Under Voltage Protection	Either output < 58% of the nominal level after 3ms time-out expires and output is enabled	Both UGATEx and LGATEx are forced low and enter discharge mode. LDO3 and LDO5 are active. Exit by VIN POR or by toggling ENLDO, ENTRIPx, and ENM.
Discharge	Either output is still high in standby mode or shutdown mode	During discharge mode, there is one path to discharge the output capacitors' residual charge to GND via an internal switch.
Standby	ENTRIPx or ENM < startup threshold, ENLDO = high.	LDO3 and LDO5 are active.
Shutdown	ENLDO = low	All circuitry are off.
Thermal Shutdown	T_J > 150°C	All circuitry are off. Exit by VIN POR or by toggling ENLDO, ENTRIPx, and ENM.

Table 2. Power Up Sequencing (RT8243A)

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	SMPS1	SMPS2
Low	Low	X	X	Off	Off	Off	Off
">1.6V" => High	Low	X	X	On	On	Off	Off
">1.6V" => High	">2.3V" => High	Off	Off	On	On	Off	Off
">1.6V" => High	">2.3V" => High	Off	On	On	On	Off	On
">1.6V" => High	">2.3V" => High	On	On	On	On	On	On
">1.6V" => High	">2.3V" => High	On	Off	On	On	On	Off

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Output Voltage Setting (FBx)

Connect a resistive voltage divider at the FBx pin between V_{OUTx} and GND to adjust the output voltage between 2V and 5.5V (Figure 7). Choose R2 to be approximately 10kΩ, and solve for R1 using the equation :

$$V_{OUT} = V_{FBx} \times \left(1+\left(\frac{R1}{R2}\right)\right)$$

where V_{FBx} is 2V (typ.).

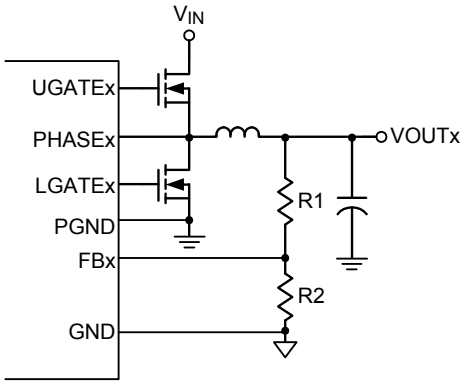


Figure 7. Setting V_{OUTx} with a resistive voltage divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUTx})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current, I_{PEAK} :

$$I_{PEAK} = I_{LOAD(MAX)} + [\ (LIR / 2) \times I_{LOAD(MAX)}\ ]$$

The calculation above shall serve as a general reference. To further improve transient response, the output inductance can be further reduced. Of course, besides the inductor, the output capacitor should also be considered when improving transient response.

Output Capacitor Selection

The capacitor value and ESR determine the amount of output voltage ripple and load transient response. Thus, the capacitor value must be greater than the largest value calculated from below equations.

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (t_{ON} + t_{OFF(MIN)})}{2 \times C_{OUT} \times \left[V_{IN} \times t_{ON} - V_{OUTx}(t_{ON} + t_{OFF(MIN)}) \right]}$$

$$V_{SOAR} = \frac{(\Delta I_{LOAD})^2 \times L}{2 \times C_{OUT} \times V_{OUTx}}$$

$$V_{P-P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f} \right)$$

where V_{SAG} and V_{SOAR} are the allowable amount of undershoot and overshoot voltage during load transient, V_{p-p} is the output ripple voltage, and $t_{OFF(MIN)}$ is the minimum off-time.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for WQFN-20L 3x3 package

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The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

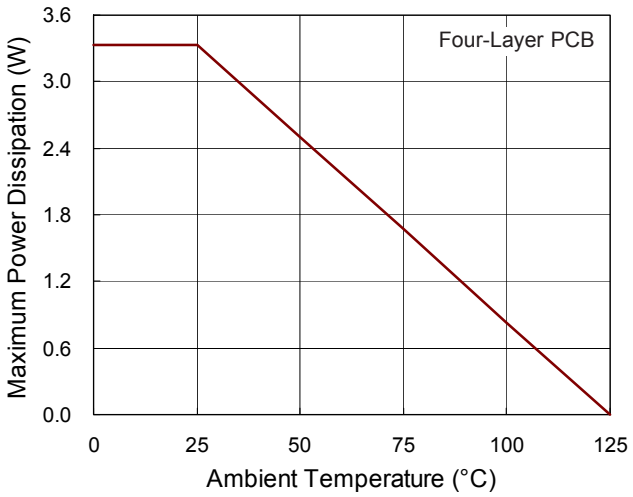


Figure 8. Derating Curve of Maximum Power Dissipation

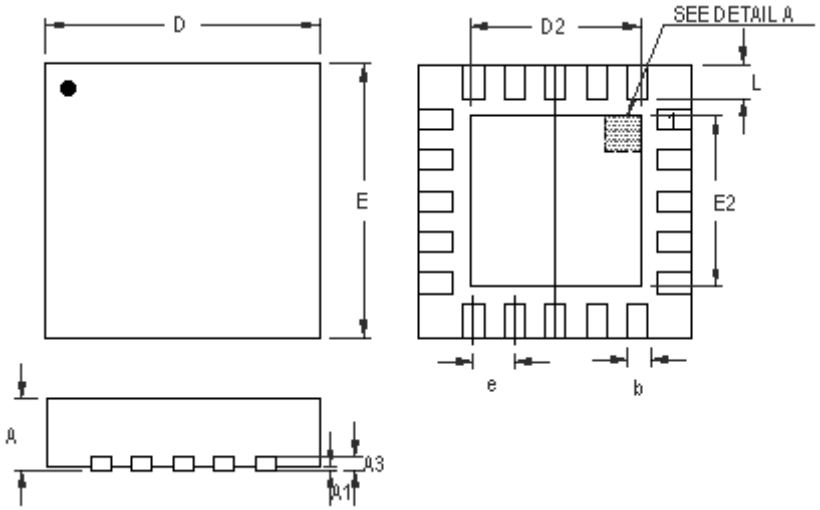
Layout Considerations

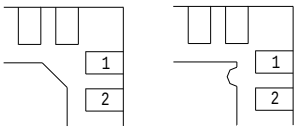
Layout is very important in high frequency switching converter design. Improper PCB layout can radiate excessive noise and contribute to the converter's instability. Certain points must be considered before starting a layout with the RT8243A/B/C.

- Place the filter capacitor close to the IC, within 12mm (0.5 inch) if possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance. Use 0.65mm (25 mils) or wider trace.
- All sensitive analog traces and components such as FBx, ENTRIPx, PGOOD, and TON should be placed away from high voltage switching nodes such as PHASEx, LGATEx, UGATEx, or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Place ground terminal of VIN capacitor(s), V_{OUTx} capacitor(s), and source of low side MOSFETs as close to each other as possible. The PCB trace of PHASEx node, which connects to source of high side MOSFET, drain of low side MOSFET and high voltage side of the inductor, should be as short and wide as possible.

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Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

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