3+2 Voltage Regulator for IMVP-7/VR12™ CPUs

ISL95836

Compliant with IMVP-7/VR12™, the ISL95836 provides a complete solution for microprocessor and graphic processor core power supply. It provides two Voltage Regulators (VRs) with three integrated gate drivers. The first VR can be configured as 3-, 2- or 1-phase VR while the second VR could be configured as 2- or 1-phase VR, providing maximum flexibility. The two VRs share the serial control bus to communicate with the CPU and achieve lower cost and smaller board area compared with the two-chip approach.

Based on Intersil's Robust Ripple Regulator (R3) technology™, the PWM modulator compared to traditional modulators, has faster transient settling time, variable switching frequency during load transients and has improved light load efficiency with it's ability to automatically change switching frequency.

The ISL95836 has several other key features. Both outputs support DCR current sensing with single NTC thermistor for DCR temperature compensation or accurate resistor current sensing. Both outputs come with remote voltage sense, programmable V_{BOOT} voltage, I_{MAX} and switching frequency, adjustable OC protection and separate Power-Good.

Features

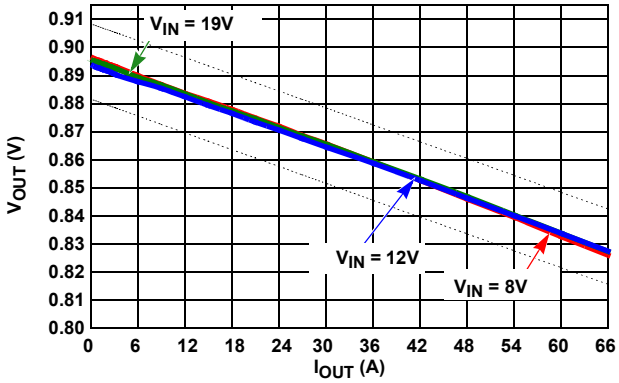
- Serial Data Bus
- Dual Outputs:
  - Configurable 3-, 2- or 1-phase for the 1st Output using 2 integrated Gate Drivers
  - Configurable 2- or 1-phase for the 2nd Output using an Integrated Gate Driver
- 0.5% System Accuracy Over-Temperature
- Supports Multiple Current Sensing Methods
  - Lossless Inductor DCR Current Sensing
  - Precision Resistor Current Sensing
- Differential Remote Voltage Sensing
- Programmable V_{BOOT} Voltage at Start-up
- Resistor Programmable I_{MAX}, Switching Frequency for Both Outputs
- Adaptive Body Diode Conduction Time Reduction

Applications

- IMVP-7/VR12 Compliant Computers

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Load Line Regulation



Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL95836HRTZ	95836 HRTZ	-10 to +100	40 Ld 5x5 TQFN	L40.5x5
ISL95836IRTZ	95836 IRTZ	-40 to +100	40 Ld 5x5 TQFN	L40.5x5

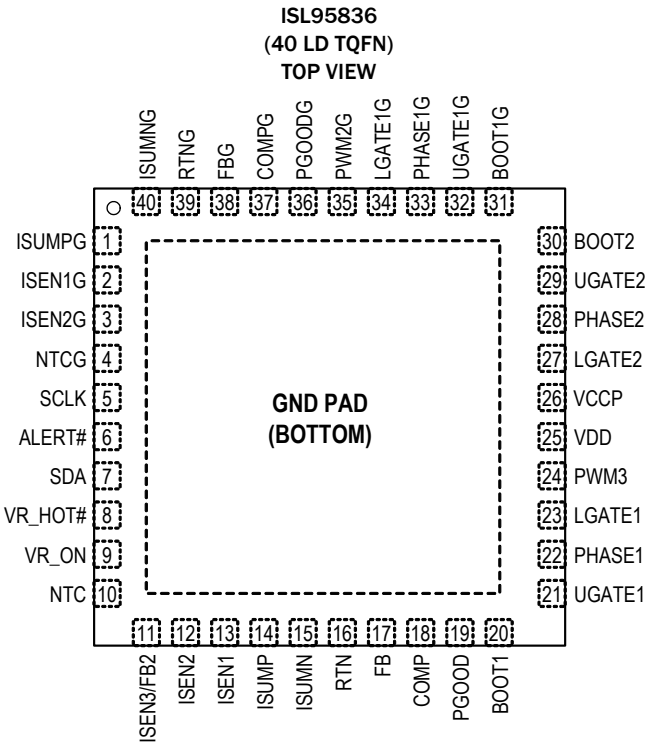
NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL95836. For more information on MSL please see techbrief TB363.

THIS IS A PRE-DEVELOPMENT PRELIMINARY DATASHEET. DEVICE FUNCTIONALITY AND SPECIFICATIONS ARE SUBJECT TO CHANGE

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Pin Configuration



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Pin Descriptions

ISL95836 PIN NUMBER	SYMBOL	DESCRIPTION
BOTTOM PAD	GND	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin. In addition, it is the return path for all the low-side MOSFET gate drivers. It should also be used as the thermal pad for heat removal.
2	ISEN1G	Individual current sensing for VR2 Phase 1.
3	ISEN2G	Individual current sensing for VR2 Phase 2. When ISEN2 is pulled to 5V VDD, the controller will disable VR2 Phases 2.
4	NTCG	The second thermistor input to VR_HOT# circuit. Use it to monitor VR2 temperature.
5, 6, 7	SCLK, ALERT#, SDA	Communication bus between the CPU and the VRs.
8	VR_HOT#	Open drain thermal overload output indicator. Can be considered part of communication bus with CPU.
9	VR_ON	Controller enable input. A high level logic signal on this pin enables the controller.
10	NTC	One of the thermistor inputs to VR_HOT# circuit. Use it to monitor VR1 temperature.
11	INSE3/FB2	When the VR1 is configured in 3-phase mode, this pin is ISEN3. ISEN3 is the individual current sensing for VR1 phase 3. When VR1 is configured in 2-phase mode, this pin is FB2. There is a switch between the FB2 pin and the FB pin. The switch is on when VR1 is in 2-phase mode and is off in 1-phase mode. The components connecting to FB2 are used to adjust the compensation in 1-phase mode to achieve optimum performance for VR1.
12	ISEN2	Individual current sensing for VR1 Phase 2. When ISEN2 and PWM3 are both pulled to 5V VDD, the controller will disable VR1 Phases 3 and 2.
13	ISEN1	Individual current sensing for VR1 Phase 1.

Pin Descriptions (Continued)

ISL95836 PIN NUMBER	SYMBOL	DESCRIPTION
14, 15	ISUMP and ISUMN	VR1 droop current sense input.
16	RTN	VR1 remote voltage sensing return.
17	FB	This pin is the inverting input of the error amplifier for VR1.
18	COMP	This pin is the output of the error amplifier for VR1. Also, aresistor from this pin to GND programs Imax for VR1, and Vboot for both VR1 and VR2.
19	PGOOD	Power-Good open-drain output indicating when VR1 is able to supply regulated voltage. Pull up externally with a 680Ω resistor to VCCP or 1.9kΩ to 3.3V.
20	BOOT1	Connect an MLCC capacitor across the BOOT1 and the PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT1 pin, each time the PHASE1 pin drops below VCCP minus the voltage dropped across the internal boot diode.
21	UGATE1	Output of VR1 Phase-1 high-side MOSFET gate driver. Connect the UGATE1 pin to the gate of the Phase-1 high-side MOSFET.
22	PHASE1	Current return path for the VR1 Phase-1 high-side MOSFET gate driver. Connect the PHASE1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of VR1 Phase 1.
23	LGATE1	Output of VR1 Phase-1 low-side MOSFET gate driver. Connect the LGATE1 pin to the gate of VR1 Phase-1 low-side MOSFET.
24	PWM3	PWM output for VR1 Phase 3. When PWM3 is pulled to 5V VDD, the controller will disable VR1 Phase 3.
25	VDD	5V bias power.
26	VCCP	Input voltage bias for the internal gate drivers. Connect +5V to the VCCP pin. Decouple with at least 1µF of an MLCC capacitor.
27	LGATE2	Output of VR1 Phase-2 low-side MOSFET gate driver. Connect the LGATE2 pin to the gate of VR1 Phase-2 low-side MOSFET.
28	PHASE2	Current return path for VR1 Phase-2 high-side MOSFET gate driver. Connect the PHASE2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of VR1 Phase 2.
29	UGATE2	Output of VR1 Phase-2 high-side MOSFET gate driver. Connect the UGATE2 pin to the gate of VR1 Phase-2 high-side MOSFET.
30	BOOT2	Connect an MLCC capacitor across the BOOT2 and the PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT2 pin, each time the PHASE2 pin drops below VCCP minus the voltage dropped across the internal boot diode.
31	BOOT1G	Connect an MLCC capacitor across the BOOTG and the PHASE1G pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT1G pin, each time the PHASEG pin drops below VCCP minus the voltage dropped across the internal boot diode.
32	UGATE1G	Output of VR2 Phase-1 high-side MOSFET gate driver. Connect the UGATE1G pin to the gate of VR2 Phase-1 high-side MOSFET.
33	PHASE1G	Current return path for VR2 Phase-1 high-side MOSFET gate driver. Connect the PHASEG pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of VR2 Phase 1.
34	LGATE1G	Output of VR2 Phase-1 low-side MOSFET gate driver. Connect the LGATE1G pin to the gate of VR2 Phase-1 low-side MOSFET.
35	PWM2G	PWM output for VR2 Phase 2.
36	PGOODG	Power-Good open-drain output indicating when VR2 is able to supply regulated voltage. Pull up externally with a 680Ω resistor to VCCP or 1.9kΩ to 3.3V.
37	COMPG	This pin is the output of the error amplifier for VR2. Also, aresistor from this pin to GND programs Imax for VR2 and Tmax for both VR1 and VR2.

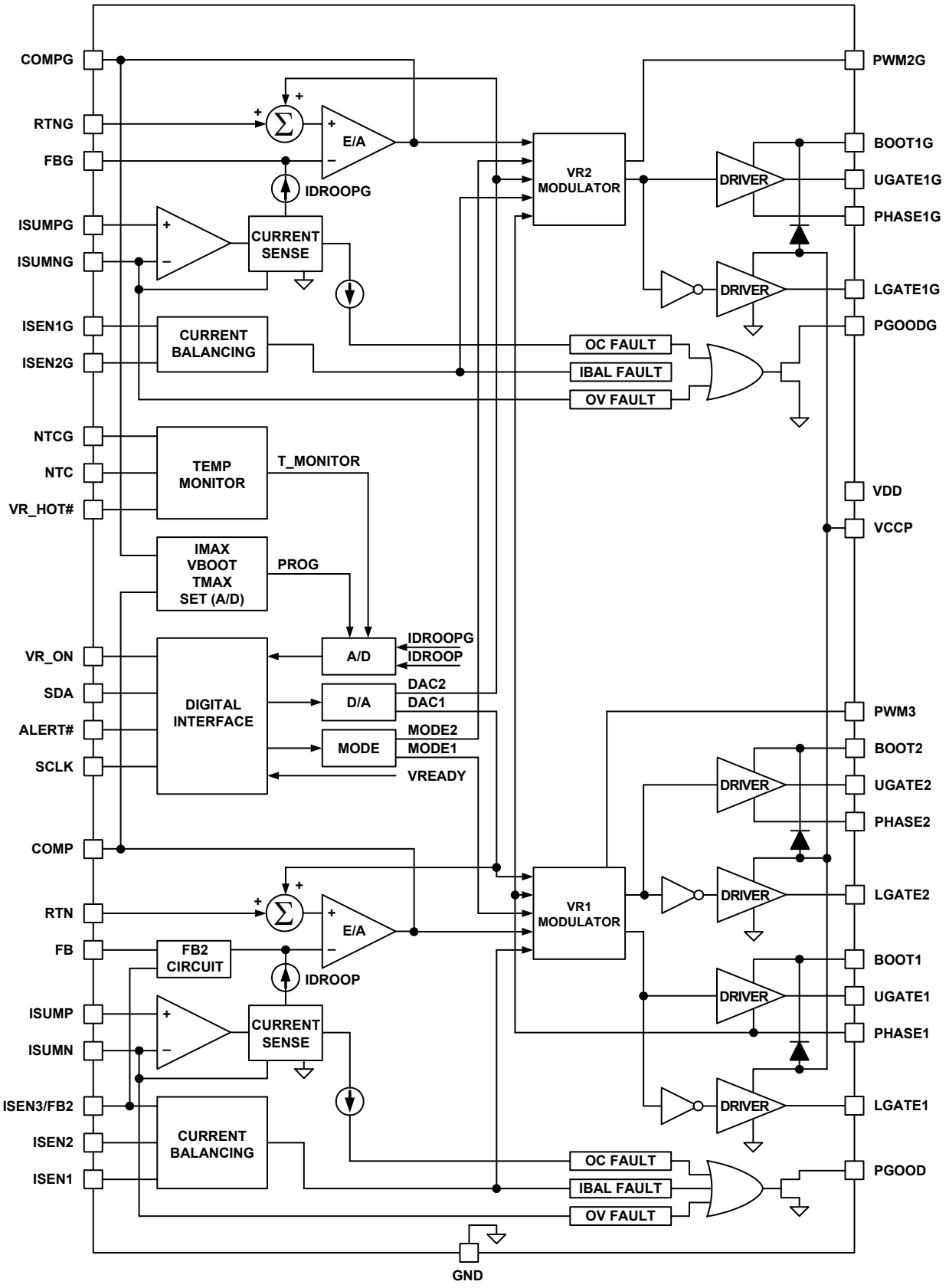
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Pin Descriptions (Continued)

ISL95836 PIN NUMBER	SYMBOL	DESCRIPTION
38	FBG	This pin is the inverting input of the error amplifier for VR2.
39	RTNG	VR2 remote voltage sensing return.
40, 1	ISUMNG and ISUMPG	VR2 droop current sense input. When ISUMNG is pulled to 5V VDD, all the communication to VR2 is disabled.

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Block Diagram



Simplified Application Circuit

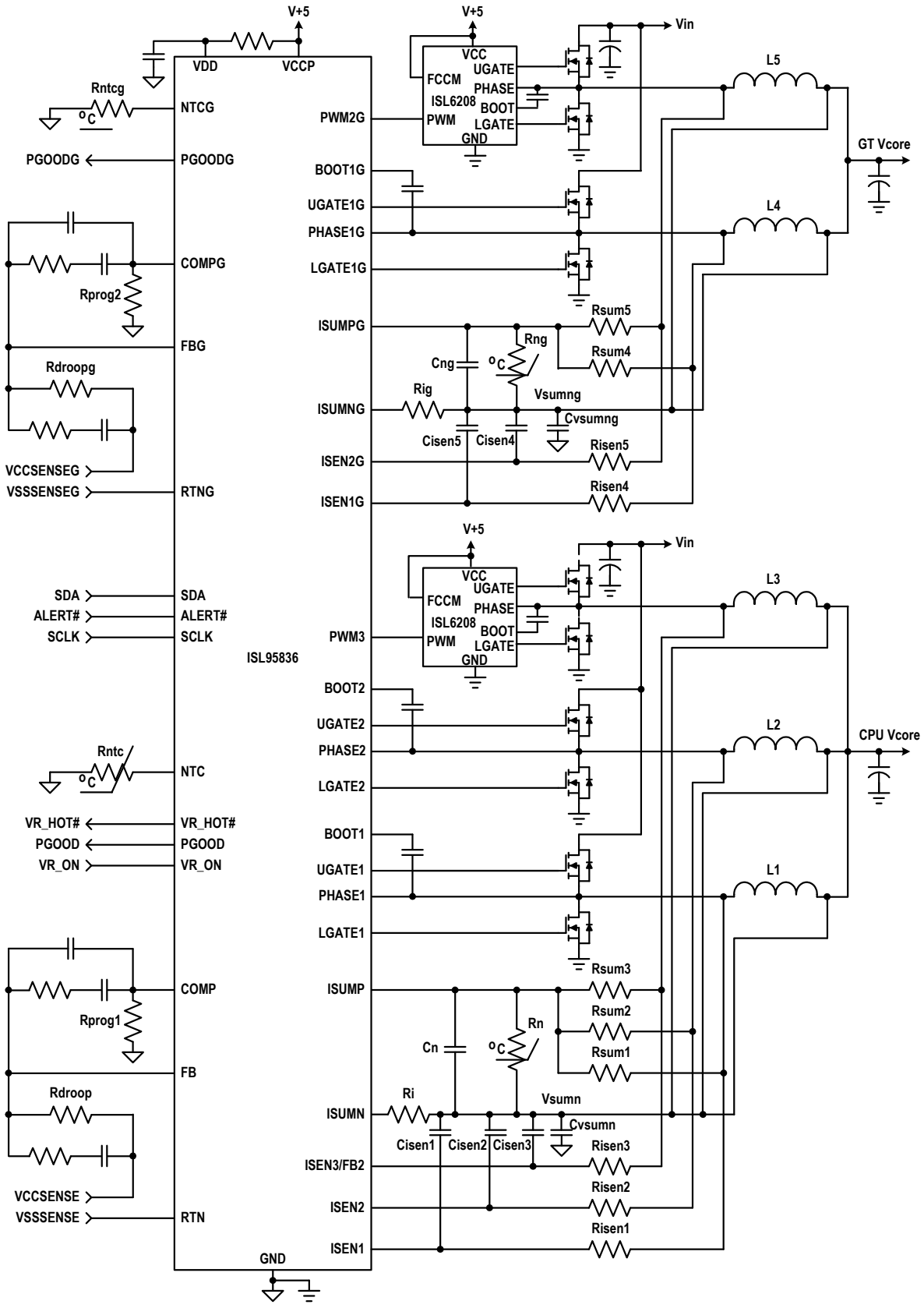


FIGURE 1. TYPICAL ISL95836 APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

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Absolute Maximum Ratings

Supply Voltage, VDD . . . . . -0.3V to +7V
Battery Voltage, VIN . . . . . +28V
Boot Voltage (BOOT) . . . . . -0.3V to +33V
Boot-to-Phase Voltage
(BOOT-PHASE) -0.3V to +7V(DC) . . . . . -0.3V to +9V(<10ns)
Phase Voltage (PHASE) . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . PHASE - 0.3V (DC) to BOOT
. . . . . PHASE - 5V (<20ns Pulse Width, 10µJ) to BOOT
LGATE Voltage
. . . . . -2.5V (<20ns Pulse Width, 5µJ) to VDD+0.3V
All Other Pins . . . . . -0.3V to (VDD +0.3V)
Open Drain Outputs, PGOOD, VR_HOT#, ALERT# . . . . . -0.3V to +7V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per JESD22-C101A) 1k
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld TQFN Package (Notes 4, 5)	29	1

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage, VDD . . . . . +5V ±5%
Battery Voltage, VIN . . . . . +4.5V to 25V
Ambient Temperature
HRTZ . . . . . -10°C to +100°C
IRTZ . . . . . -40°C to +100°C
Junction Temperature
HRTZ . . . . . -10°C to +125°C
IRTZ . . . . . -40°C to +125°C

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CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

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Electrical Specifications

"Operating Conditions: VDD = 5V, T_A = -40°C to +100°C (ISL95836IRTZ), T_A = -10°C to +100°C (ISL95836HRTZ), fSW = 300kHz, unless otherwise noted." **Boldface limits apply over the operating temperature ranges, -10°C to +100°C or -40°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VDD}	VR_ON = 1V		5		mA
		VR_ON = 0V			**1**	µA
Battery Supply Current	I_{VIN}	VR_ON = 0V			**1**	µA
V_{IN} Input Resistance	R_{VIN}	VR_ON = 1V		550		kΩ
POWER-ON-RESET THRESHOLDS						
VDD Power-On-Reset Threshold	$VDDPOR_r$	V_{DD} rising		4.35	**4.5**	V
	$VDDPOR_f$	V_{DD} falling	**4.00**	4.15		V
VIN Power-On-Reset Threshold	$VINPOR_r$	V_{IN} rising		4.00	**4.35**	V
	$VINPOR_f$	V_{IN} falling	**2.8**	3.3		V
SYSTEM AND REFERENCES						
System Accuracy	HRTZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.52V,	**-0.5**		**+0.5**	%
		VID = 0.5V to 0.745V	**-8**		**+8**	mV
		VID = 0.25V to 0.495V	**-15**		**+15**	mV
	IRTZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.52V	**-0.8**		**+0.8**	%
		VID = 0.5V to 0.745V	**-10**		**+10**	mV
		VID = 0.25V to 0.495V	**-18**		**+18**	mV
Internal V_{BOOT}		HRTZ	**1.0945**	1.100	**1.1055**	V
		IRTZ	**1.0912**	1.100	**1.1088**	V
Maximum Output Voltage	$V_{OUT(max)}$	VID = [11111111]		1.52		V

Electrical Specifications "Operating Conditions: VDD = 5V, T_A = -40°C to +100°C (ISL95836IRTZ), T_A = -10°C to +100°C (ISL95836HRTZ), fSW = 300kHz, unless otherwise noted." **Boldface limits apply over the operating temperature ranges, -10°C to +100°C or -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Minimum Output Voltage	$V_{OUT(min)}$	VID = [00000001]		0.25		V
CHANNEL FREQUENCY						
Adjustment Range			**300**		**450**	kHz
AMPLIFIERS						
Current-Sense Amplifier Input Offset		I_{FB} = 0A	**-0.15**		**+0.15**	mV
Error Amp DC Gain	A_{V0}			90		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF		18		MHz
ISEN						
Imbalance Voltage		Maximum of ISENs - Minimum of ISENs			**1**	mV
Input Bias Current				20		nA
POWER-GOOD AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA		0.15	**0.4**	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V			**1**	µA
PGOOD Delay	tpgd			1.2		ms
ALERT# Low Voltage				7	**12**	Ω
VR_HOT# Low Voltage				7	**12**	Ω
ALERT# Leakage Current					**1**	µA
VR_HOT# Leakage Current					**1**	µA
GATE DRIVER						
UGATE Pull-Up Resistance	R_{UGPU}	200mA Source Current		1.0	**1.5**	Ω
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance	R_{UGPD}	250mA Sink Current		1.0	**1.5**	Ω
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-Up Resistance	R_{LGPU}	250mA Source Current		1.0	**1.5**	Ω
LGATE Source Current	I_{LGSRC}	LGATE - VSSP = 2.5V		2.0		A
LGATE Sink Resistance	R_{LGPD}	250mA Sink Current		0.5	**0.9**	Ω
LGATE Sink Current	I_{LGSNK}	LGATE - VSSP = 2.5V		4.0		A
UGATE to LGATE Deadtime	t_{UGFLGR}	UGATE falling to LGATE rising, no load		23		ns
LGATE to UGATE Deadtime	t_{LGFUGR}	LGATE falling to UGATE rising, no load		28		ns
BOOTSTRAP DIODE						
Forward Voltage	V_F	PVCC = 5V, I_F = 2mA		0.58		V
Reverse Leakage	I_R	V_R = 25V		0.2		µA
PROTECTION						
Overvoltage Threshold	OV_H	VSEN rising above setpoint for >1µs	**120**	155	**200**	mV
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		9		mV
VR1 Overcurrent Threshold		3-Phase - PS0 and 1-Phase - all states	**25.5**	30.6	**35.5**	µA
		3-Phase - PS1, 2-Phase - PS0	**16.75**	20.6	**24.25**	µA
		3-Phase - PS2, 2-Phase - PS1 and PS2	**8.5**	10.6	**12.75**	µA
VR2 Overcurrent Threshold		All states	**28.5**	30.6	**33.5**	µA
LOGIC THRESHOLDS						
VR_ON Input Low	V_{IL}				**0.3**	V
VR_ON Input High	V_{IH}	HRTZ	**0.7**			V
	V_{IH}	IRTZ	**0.75**			V

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Electrical Specifications "Operating Conditions: VDD = 5V, T_A = -40°C to +100°C (ISL95836IRTZ), T_A = -10°C to +100°C (ISL95836HRTZ), fSW = 300kHz, unless otherwise noted." **Boldface limits apply over the operating temperature ranges, -10°C to +100°C or -40°C to +100°C. (Continued)**

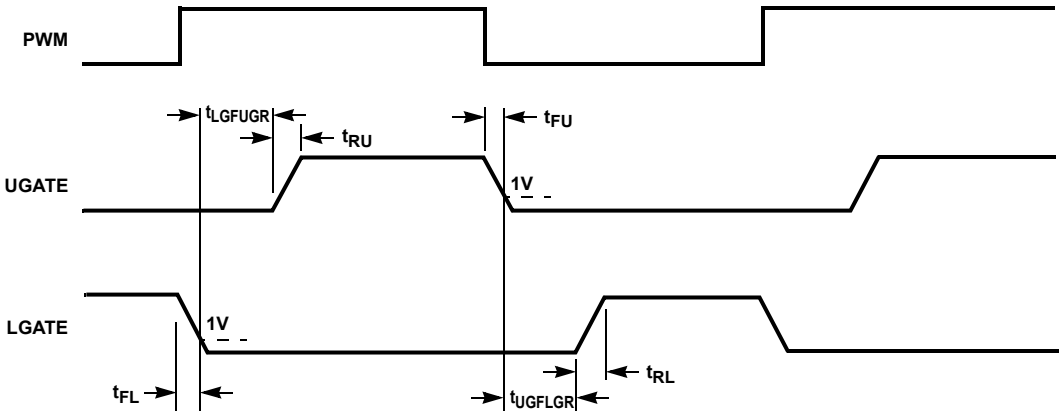
PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
PWM						
PWM Output Low	V_{0L}	Sinking 5mA			**1.0**	V
PWM Output High	V_{0H}	Sourcing 5mA	**3.5**	4.2		V
PWM Tri-State Leakage		PWM = 2.5V		2		µA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	**59**	60	**61**	µA
VR_HOT# Trip Voltage (VR1 and VR2)		Falling	**0.86**	0.873	**0.89**	V
VR_HOT# Reset Voltage (VR1 and VR2)		Rising	**0.905**	0.929	**0.935**	V
Therm_Alert Trip Voltage (VR1 and VR2)		Falling	**0.9**	0.913	**0.93**	V
Therm_Alert Reset Voltage (VR1 and VR2)		Rising	**0.945**	0.961	**0.975**	V
CURRENT MONITOR						
IccMax_Alert Trip Voltage (VR1 and VR2)		Rising	**2.63**	2.66	**2.69**	V
IccMax_Alert reset Voltage (VR1 and VR2)		Falling	**2.585**	2.62	**2.655**	V
INPUTS						
VR_ON Leakage Current	I_{VR_ON}	VR_ON = 0V	**-1**	0		µA
		VR_ON = 1V		18	**35**	µA
SCLK, SDA Leakage		VR_ON = 0V, SCLK & SDA = 0V & 1V	**-1**		**1**	µA
		VR_ON = 1V, SCLK & SDA = 1V	**-5**		**1**	µA
		VR_ON = 1V, SCLK & SDA = 0V	**-85**	-60	**-30**	µA
SLEW RATE (For VID Change)						
Fast Slew Rate			**10**			mV/µs
Slow Slew Rate			**2.5**			mV/µs

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NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Gate Driver Timing Diagram



Theory of Operation

Multiphase R3™ Modulator

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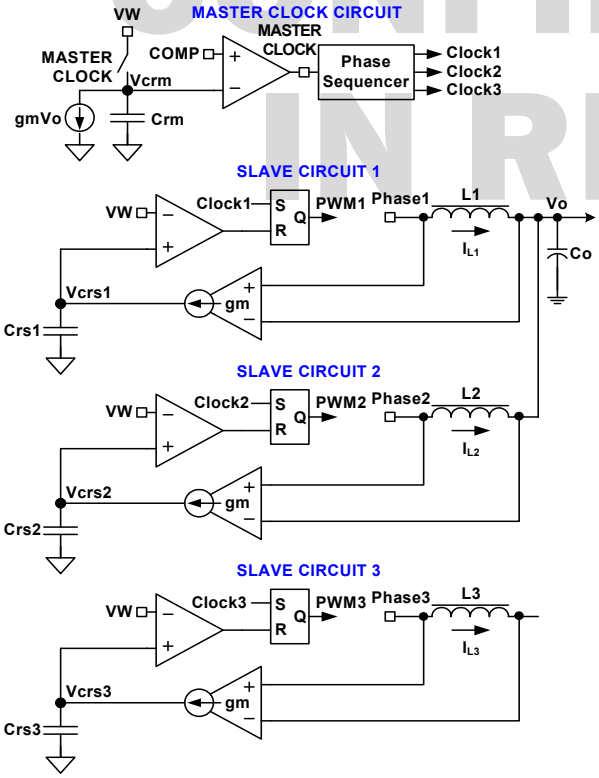


FIGURE 2. R3™ MODULATOR CIRCUIT

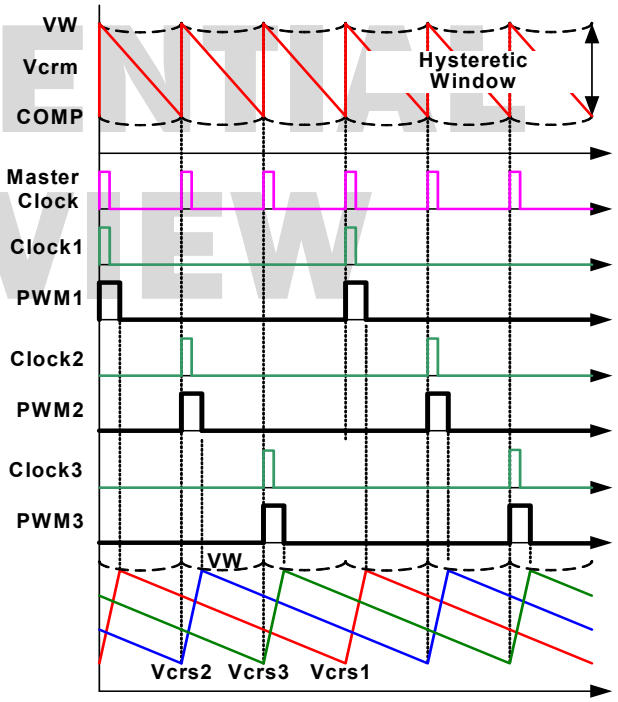


FIGURE 3. R3™ MODULATOR OPERATION PRINCIPLES IN STEADY STATE

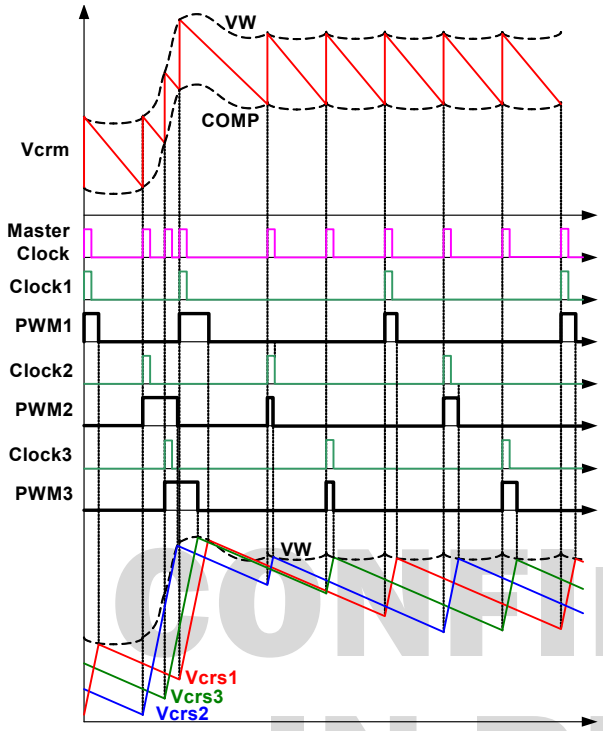


FIGURE 4. R3™ MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

The ISL95836 is a multiphase regulator implementing Intel™ IMVP-7/VR12™ protocol. It has two voltage regulators, VR1 and VR2, on one chip. VR1 can be programmed for 1-, 2- or 3-phase operation, and VR2 could be programmed for 2- or 1-phase operation. The following description is based on VR1, but also applies to VR2 because they are based on the same architecture.

The ISL95836 uses Intersil patented R3™ (Robust Ripple Regulator™) modulator. The R3™ modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 2 conceptually shows the multiphase R3™ modulator circuit, and Figure 3 shows the operation principles.

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to $g_m V_o$, where g_m is a gain factor. C_{rm} voltage V_{crm} is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP, and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits. If VR1 is in 3-phase mode, the master clock signal will be distributed to the three phases, and the Clock1~3 signals will be 120° out-of-phase. If VR1 is in 2-phase mode, the master clock signal will be distributed to Phases 1 and 2, and the Clock1 and Clock2 signals will be 180° out-of-phase. If VR1 is in 1-phase mode, the master clock signal will be distributed to Phases 1 only and be the Clock1 signal.

Each slave circuit has its own ripple capacitor C_{rs}, whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{rs}. The slave circuit turns on its PWM pulse upon receiving the clock signal, and the current source charges C_{rs}. When C_{rs} voltage V_{Crs} hits VW, the slave circuit turns off the PWM pulse, and the current source discharges C_{rs}.

Since the controller works with V_{crs}, which are large-amplitude and noise-free synthesized signals, it achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the ISL95836 uses an error amplifier that allows the controller to maintain a 0.5% output voltage accuracy.

Figure 4 shows the operation principles during load insertion response. The COMP voltage rises during load insertion, generating the master clock signal more quickly, so the PWM pulses turn on earlier, increasing the effective switching frequency, which allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls as the COMP voltage falls, reducing the current PWM pulse width. This kind of behavior gives the controller excellent response speed.

The fact that all the phases share the same VW window voltage also ensures excellent dynamic current balance among phases.

Diode Emulation and Period Stretching

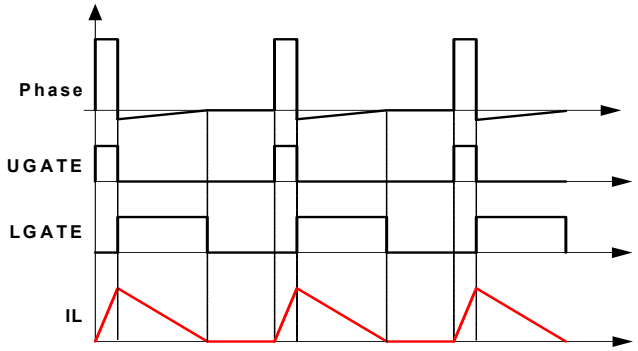


FIGURE 5. DIODE EMULATION

ISL95836 can operate in diode emulation (DE) mode to improve light load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source to drain and doesn't allow reverse current, emulating a diode. As Figure 5 shows, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The controller monitors the current through monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

If the load current is light enough, as Figure 5 shows, the inductor current will reach and stay at zero before the next phase node pulse and the regulator is in discontinuous conduction mode (DCM). If the load current is heavy enough, the inductor current

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will never reach 0A, and the regulator is in CCM although the controller is in DE mode.

Figure 6 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, therefore is the same, making the inductor current triangle the same in the three cases. The controller clamps the ripple capacitor voltage V_{crs} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{crs}, naturally stretching the switching period. The inductor current triangles move further apart from each other such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light load efficiency.

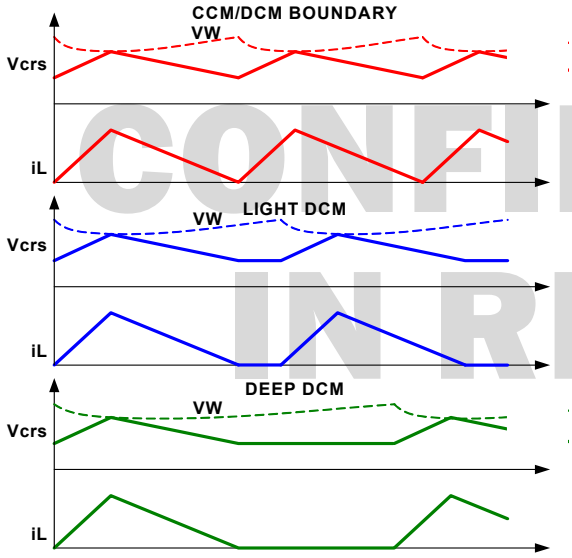


FIGURE 6. PERIOD STRETCHING

Start-up Timing

With the controller's V_{DD} voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the logic high threshold. Figure 7 shows the typical start-up timing of VR1 and VR2. The controller uses digital soft-start to ramp-up DAC to the voltage programmed by the SetVID command. PGOOD is asserted high and ALERT# is asserted low at the end of the ramp up. Similar results occur if VR_ON is tied to V_{DD}, with the soft-start sequence starting 800µs after V_{DD} crosses the POR threshold.

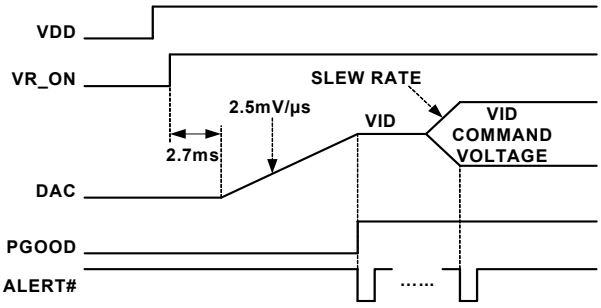


FIGURE 7. VR1 SOFT-START WAVEFORMS

Voltage Regulation and Load Line Implementation

After the start sequence, the controller regulates the output voltage to the value set by the VID information per Table 1. The controller will control the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.52V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

TABLE 1. VID TABLE

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			
0	0	0	0	0	0	0	0	0	0	0.00000
0	0	0	0	0	0	0	1	0	1	0.25000
0	0	0	0	0	0	1	0	0	2	0.25500
0	0	0	0	0	0	1	1	0	3	0.26000
0	0	0	0	0	1	0	0	0	4	0.26500
0	0	0	0	0	1	0	1	0	5	0.27000
0	0	0	0	0	1	1	0	0	6	0.27500
0	0	0	0	0	1	1	1	0	7	0.28000
0	0	0	0	1	0	0	0	0	8	0.28500
0	0	0	0	1	0	0	1	0	9	0.29000
0	0	0	0	1	0	1	0	0	A	0.29500
0	0	0	0	1	0	1	1	0	B	0.30000
0	0	0	0	1	1	0	0	0	C	0.30500
0	0	0	0	1	1	0	1	0	D	0.31000
0	0	0	0	1	1	1	0	0	E	0.31500
0	0	0	0	1	1	1	1	0	F	0.32000
0	0	0	1	0	0	0	0	1	0	0.32500
0	0	0	1	0	0	0	1	1	1	0.33000
0	0	0	1	0	0	1	0	1	2	0.33500
0	0	0	1	0	0	1	1	1	3	0.34000
0	0	0	1	0	1	0	0	1	4	0.34500
0	0	0	1	0	1	0	1	1	5	0.35000
0	0	0	1	0	1	1	0	1	6	0.35500
0	0	0	1	0	1	1	1	1	7	0.36000
0	0	0	1	1	0	0	0	1	8	0.36500
0	0	0	1	1	0	0	1	1	9	0.37000
0	0	0	1	1	0	1	0	1	A	0.37500
0	0	0	1	1	0	1	1	1	B	0.38000
0	0	0	1	1	1	0	0	1	C	0.38500
0	0	0	1	1	1	0	1	1	D	0.39000
0	0	0	1	1	1	1	0	1	E	0.39500
0	0	0	1	1	1	1	1	1	F	0.40000

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TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			
0	0	1	0	0	0	0	0	2	0	0.40500
0	0	1	0	0	0	0	1	2	1	0.41000
0	0	1	0	0	0	1	0	2	2	0.41500
0	0	1	0	0	0	1	1	2	3	0.42000
0	0	1	0	0	1	0	0	2	4	0.42500
0	0	1	0	0	1	0	1	2	5	0.43000
0	0	1	0	0	1	1	0	2	6	0.43500
0	0	1	0	0	1	1	1	2	7	0.44000
0	0	1	0	1	0	0	0	2	8	0.44500
0	0	1	0	1	0	0	1	2	9	0.45000
0	0	1	0	1	0	1	0	2	A	0.45500
0	0	1	0	1	0	1	1	2	B	0.46000
0	0	1	0	1	1	0	0	2	C	0.46500
0	0	1	0	1	1	0	1	2	D	0.47000
0	0	1	0	1	1	1	0	2	E	0.47500
0	0	1	0	1	1	1	1	2	F	0.48000
0	0	1	1	0	0	0	0	3	0	0.48500
0	0	1	1	0	0	0	1	3	1	0.49000
0	0	1	1	0	0	1	0	3	2	0.49500
0	0	1	1	0	0	1	1	3	3	0.50000
0	0	1	1	0	1	0	0	3	4	0.50500
0	0	1	1	0	1	0	1	3	5	0.51000
0	0	1	1	0	1	1	0	3	6	0.51500
0	0	1	1	0	1	1	1	3	7	0.52000
0	0	1	1	1	0	0	0	3	8	0.52500
0	0	1	1	1	0	0	1	3	9	0.53000
0	0	1	1	1	0	1	0	3	A	0.53500
0	0	1	1	1	0	1	1	3	B	0.54000
0	0	1	1	1	1	0	0	3	C	0.54500
0	0	1	1	1	1	0	1	3	D	0.55000
0	0	1	1	1	1	1	0	3	E	0.55500
0	0	1	1	1	1	1	1	3	F	0.56000
0	1	0	0	0	0	0	0	4	0	0.56500
0	1	0	0	0	0	0	1	4	1	0.57000
0	1	0	0	0	0	1	0	4	2	0.57500
0	1	0	0	0	0	1	1	4	3	0.58000
0	1	0	0	0	1	0	0	4	4	0.58500
0	1	0	0	0	1	0	1	4	5	0.59000
0	1	0	0	0	1	1	0	4	6	0.59500

TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			
0	1	0	0	0	1	1	1	4	7	0.60000
0	1	0	0	1	0	0	0	4	8	0.60500
0	1	0	0	1	0	0	1	4	9	0.61000
0	1	0	0	1	0	1	0	4	A	0.61500
0	1	0	0	1	0	1	1	4	B	0.62000
0	1	0	0	1	1	0	0	4	C	0.62500
0	1	0	0	1	1	0	1	4	D	0.63000
0	1	0	0	1	1	1	0	4	E	0.63500
0	1	0	0	1	1	1	1	4	F	0.64000
0	1	0	1	0	0	0	0	5	0	0.64500
0	1	0	1	0	0	0	1	5	1	0.65000
0	1	0	1	0	0	1	0	5	2	0.65500
0	1	0	1	0	0	1	1	5	3	0.66000
0	1	0	1	0	1	0	0	5	4	0.66500
0	1	0	1	0	1	0	1	5	5	0.67000
0	1	0	1	0	1	1	0	5	6	0.67500
0	1	0	1	0	1	1	1	5	7	0.68000
0	1	0	1	1	0	0	0	5	8	0.68500
0	1	0	1	1	0	0	1	5	9	0.69000
0	1	0	1	1	0	1	0	5	A	0.69500
0	1	0	1	1	0	1	1	5	B	0.70000
0	1	0	1	1	1	0	0	5	C	0.70500
0	1	0	1	1	1	0	1	5	D	0.71000
0	1	0	1	1	1	1	0	5	E	0.71500
0	1	0	1	1	1	1	1	5	F	0.72000
0	1	1	0	0	0	0	0	6	0	0.72500
0	1	1	0	0	0	0	1	6	1	0.73000
0	1	1	0	0	0	1	0	6	2	0.73500
0	1	1	0	0	0	1	1	6	3	0.74000
0	1	1	0	0	1	0	0	6	4	0.74500
0	1	1	0	0	1	0	1	6	5	0.75000
0	1	1	0	0	1	1	0	6	6	0.75500
0	1	1	0	0	1	1	1	6	7	0.76000
0	1	1	0	1	0	0	0	6	8	0.76500
0	1	1	0	1	0	0	1	6	9	0.77000
0	1	1	0	1	0	1	0	6	A	0.77500
0	1	1	0	1	0	1	1	6	B	0.78000
0	1	1	0	1	1	0	0	6	C	0.78500
0	1	1	0	1	1	0	1	6	D	0.79000

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TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			
0	1	1	0	1	1	1	0	6	E	0.79500
0	1	1	0	1	1	1	1	6	F	0.80000
0	1	1	1	0	0	0	0	7	0	0.80500
0	1	1	1	0	0	0	1	7	1	0.81000
0	1	1	1	0	0	1	0	7	2	0.81500
0	1	1	1	0	0	1	1	7	3	0.82000
0	1	1	1	0	1	0	0	7	4	0.82500
0	1	1	1	0	1	0	1	7	5	0.83000
0	1	1	1	0	1	1	0	7	6	0.83500
0	1	1	1	0	1	1	1	7	7	0.84000
0	1	1	1	1	0	0	0	7	8	0.84500
0	1	1	1	1	0	0	1	7	9	0.85000
0	1	1	1	1	0	1	0	7	A	0.85500
0	1	1	1	1	0	1	1	7	B	0.86000
0	1	1	1	1	1	0	0	7	C	0.86500
0	1	1	1	1	1	0	1	7	D	0.87000
0	1	1	1	1	1	1	0	7	E	0.87500
0	1	1	1	1	1	1	1	7	F	0.88000
1	0	0	0	0	0	0	0	8	0	0.88500
1	0	0	0	0	0	0	1	8	1	0.89000
1	0	0	0	0	0	1	0	8	2	0.89500
1	0	0	0	0	0	1	1	8	3	0.90000
1	0	0	0	0	1	0	0	8	4	0.90500
1	0	0	0	0	1	0	1	8	5	0.91000
1	0	0	0	0	1	1	0	8	6	0.91500
1	0	0	0	0	1	1	1	8	7	0.92000
1	0	0	0	1	0	0	0	8	8	0.92500
1	0	0	0	1	0	0	1	8	9	0.93000
1	0	0	0	1	0	1	0	8	A	0.93500
1	0	0	0	1	0	1	1	8	B	0.94000
1	0	0	0	1	1	0	0	8	C	0.94500
1	0	0	0	1	1	0	1	8	D	0.95000
1	0	0	0	1	1	1	0	8	E	0.95500
1	0	0	0	1	1	1	1	8	F	0.96000
1	0	0	1	0	0	0	0	9	0	0.96500
1	0	0	1	0	0	0	1	9	1	0.97000
1	0	0	1	0	0	1	0	9	2	0.97500
1	0	0	1	0	0	1	1	9	3	0.98000
1	0	0	1	0	1	0	0	9	4	0.98500

TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			
1	0	0	1	0	1	0	1	9	5	0.99000
1	0	0	1	0	1	1	0	9	6	0.99500
1	0	0	1	0	1	1	1	9	7	1.00000
1	0	0	1	1	0	0	0	9	8	1.00500
1	0	0	1	1	0	0	1	9	9	1.01000
1	0	0	1	1	0	1	0	9	A	1.01500
1	0	0	1	1	0	1	1	9	B	1.02000
1	0	0	1	1	1	0	0	9	C	1.02500
1	0	0	1	1	1	0	1	9	D	1.03000
1	0	0	1	1	1	1	0	9	E	1.03500
1	0	0	1	1	1	1	1	9	F	1.04000
1	0	1	0	0	0	0	0	A	0	1.04500
1	0	1	0	0	0	0	1	A	1	1.05000
1	0	1	0	0	0	1	0	A	2	1.05500
1	0	1	0	0	0	1	1	A	3	1.06000
1	0	1	0	0	1	0	0	A	4	1.06500
1	0	1	0	0	1	0	1	A	5	1.07000
1	0	1	0	0	1	1	0	A	6	1.07500
1	0	1	0	0	1	1	1	A	7	1.08000
1	0	1	0	1	0	0	0	A	8	1.08500
1	0	1	0	1	0	0	1	A	9	1.09000
1	0	1	0	1	0	1	0	A	A	1.09500
1	0	1	0	1	0	1	1	A	B	1.10000
1	0	1	0	1	1	0	0	A	C	1.10500
1	0	1	0	1	1	0	1	A	D	1.11000
1	0	1	0	1	1	1	0	A	E	1.11500
1	0	1	0	1	1	1	1	A	F	1.12000
1	0	1	1	0	0	0	0	B	0	1.12500
1	0	1	1	0	0	0	1	B	1	1.13000
1	0	1	1	0	0	1	0	B	2	1.13500
1	0	1	1	0	0	1	1	B	3	1.14000
1	0	1	1	0	1	0	0	B	4	1.14500
1	0	1	1	0	1	0	1	B	5	1.15000
1	0	1	1	0	1	1	0	B	6	1.15500
1	0	1	1	0	1	1	1	B	7	1.16000
1	0	1	1	1	0	0	0	B	8	1.16500
1	0	1	1	1	0	0	1	B	9	1.17000
1	0	1	1	1	0	1	0	B	A	1.17500
1	0	1	1	1	0	1	1	B	B	1.18000

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TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			
1	0	1	1	1	1	0	0	B	C	1.18500
1	0	1	1	1	1	0	1	B	D	1.19000
1	0	1	1	1	1	1	0	B	E	1.19500
1	0	1	1	1	1	1	1	B	F	1.20000
1	1	0	0	0	0	0	0	C	0	1.20500
1	1	0	0	0	0	0	1	C	1	1.21000
1	1	0	0	0	0	1	0	C	2	1.21500
1	1	0	0	0	0	1	1	C	3	1.22000
1	1	0	0	0	1	0	0	C	4	1.22500
1	1	0	0	0	1	0	1	C	5	1.23000
1	1	0	0	0	1	1	0	C	6	1.23500
1	1	0	0	0	1	1	1	C	7	1.24000
1	1	0	0	1	0	0	0	C	8	1.24500
1	1	0	0	1	0	0	1	C	9	1.25000
1	1	0	0	1	0	1	0	C	A	1.25500
1	1	0	0	1	0	1	1	C	B	1.26000
1	1	0	0	1	1	0	0	C	C	1.26500
1	1	0	0	1	1	0	1	C	D	1.27000
1	1	0	0	1	1	1	0	C	E	1.27500
1	1	0	0	1	1	1	1	C	F	1.28000
1	1	0	1	0	0	0	0	D	0	1.28500
1	1	0	1	0	0	0	1	D	1	1.29000
1	1	0	1	0	0	1	0	D	2	1.29500
1	1	0	1	0	0	1	1	D	3	1.30000
1	1	0	1	0	1	0	0	D	4	1.30500
1	1	0	1	0	1	0	1	D	5	1.31000
1	1	0	1	0	1	1	0	D	6	1.31500
1	1	0	1	0	1	1	1	D	7	1.32000
1	1	0	1	1	0	0	0	D	8	1.32500
1	1	0	1	1	0	0	1	D	9	1.33000
1	1	0	1	1	0	1	0	D	A	1.33500
1	1	0	1	1	0	1	1	D	B	1.34000
1	1	0	1	1	1	0	0	D	C	1.34500
1	1	0	1	1	1	0	1	D	D	1.35000
1	1	0	1	1	1	1	0	D	E	1.35500
1	1	0	1	1	1	1	1	D	F	1.36000
1	1	1	0	0	0	0	0	E	0	1.36500
1	1	1	0	0	0	0	1	E	1	1.37000
1	1	1	0	0	0	1	0	E	2	1.37500

TABLE 1. VID TABLE (Continued)

VID								Hex		V_O (V)
7	6	5	4	3	2	1	0			
1	1	1	0	0	0	1	1	E	3	1.38000
1	1	1	0	0	1	0	0	E	4	1.38500
1	1	1	0	0	1	0	1	E	5	1.39000
1	1	1	0	0	1	1	0	E	6	1.39500
1	1	1	0	0	1	1	1	E	7	1.40000
1	1	1	0	1	0	0	0	E	8	1.40500
1	1	1	0	1	0	0	1	E	9	1.41000
1	1	1	0	1	0	1	0	E	A	1.41500
1	1	1	0	1	0	1	1	E	B	1.42000
1	1	1	0	1	1	0	0	E	C	1.42500
1	1	1	0	1	1	0	1	E	D	1.43000
1	1	1	0	1	1	1	0	E	E	1.43500
1	1	1	0	1	1	1	1	E	F	1.44000
1	1	1	1	0	0	0	0	F	0	1.44500
1	1	1	1	0	0	0	1	F	1	1.45000
1	1	1	1	0	0	1	0	F	2	1.45500
1	1	1	1	0	0	1	1	F	3	1.46000
1	1	1	1	0	1	0	0	F	4	1.46500
1	1	1	1	0	1	0	1	F	5	1.47000
1	1	1	1	0	1	1	0	F	6	1.47500
1	1	1	1	0	1	1	1	F	7	1.48000
1	1	1	1	1	0	0	0	F	8	1.48500
1	1	1	1	1	0	0	1	F	9	1.49000
1	1	1	1	1	0	1	0	F	A	1.49500
1	1	1	1	1	0	1	1	F	B	1.50000
1	1	1	1	1	1	0	0	F	C	1.50500
1	1	1	1	1	1	0	1	F	D	1.51000
1	1	1	1	1	1	1	0	F	E	1.51500
1	1	1	1	1	1	1	1	F	F	1.52000

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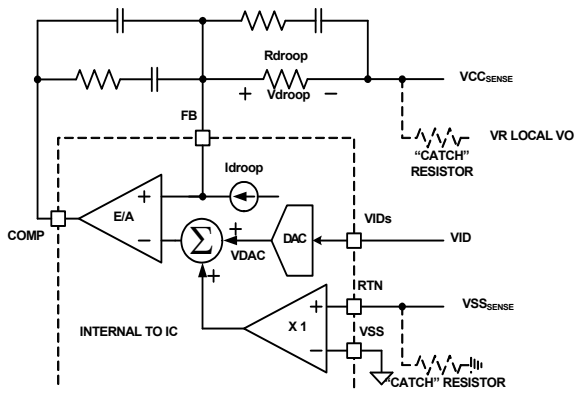


FIGURE 8. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

As the load current increases from zero, the output voltage will droop from the VID table value by an amount proportional to the load current to achieve the load line. The controller can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors (as shown in Figure 1) or through resistors in series with the inductors (as shown in Figure 2). In both methods, capacitor C_n voltage represents the inductor total currents. A droop amplifier converts C_n voltage into an internal current source with the gain set by resistor R_i. The current source is used for load line implementation, current monitor and overcurrent protection.

Figure 8 shows the load line implementation. The controller drives a current source I_{droop} out of the FB pin, described by Equation 1.

$$I_{droop} = \frac{V_{Cn}}{R_i} \quad \text{(EQ. 1)}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding thus sustaining the load line accuracy with reduced cost.

I_{droop} flows through resistor R_{droop} and creates a voltage drop, as shown in Equation 2.

$$V_{droop} = R_{droop} \times I_{droop} \quad \text{(EQ. 2)}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can both change the load line slope. Since I_{droop} also sets the overcurrent protection level, it is recommended to first scale I_{droop} based on OCP requirement, then select an appropriate R_{droop} value to obtain the desired load line slope.

Differential Voltage Sensing

Figure 8 also shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and adds it to the DAC output. The error amplifier regulates the inverting and the non-inverting input voltages to be equal, as shown in Equation 3:

Rewriting Equation 3 and substitution of Equation 2 gives:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 3)}$$

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \quad \text{(EQ. 4)}$$

Equation 4 is the exact equation required for load line implementation.

The VCC_{SENSE} and VSS_{SENSE} signals come from the processor die. The feedback will be open circuit in the absence of the processor. As Figure 8 shows, it is recommended to add a "catch" resistor to feed the VR local output voltage back to the compensator, and add another "catch" resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, will provide voltage feedback if the system is powered up without a processor installed.

Phase Current Balancing

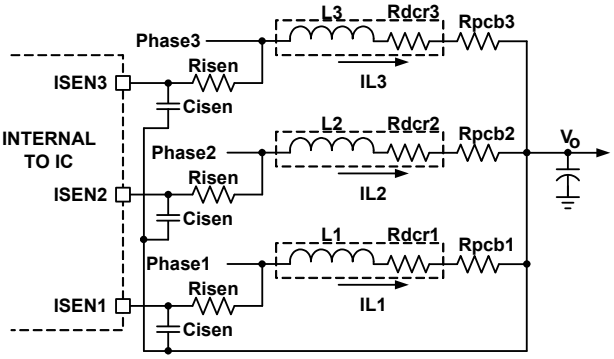


FIGURE 9. CURRENT BALANCING CIRCUIT

The controller monitors individual phase average current by monitoring the ISEN1, ISEN2, and ISEN3 voltages. Figure 9 shows the recommended current balancing circuit. Each phase node voltage is averaged by a low-pass filter consisting of R_{isen} and C_{isen}, and presented to the corresponding ISEN pin. R_{isen} should be routed to inductor phase-node pad in order to eliminate the effect of phase node parasitic PCB DCR. Equations 5 thru 7 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} \quad \text{(EQ. 5)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} \quad \text{(EQ. 6)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} \quad \text{(EQ. 7)}$$

where R_{dcr1}, R_{dcr2} and R_{dcr3} are inductor DCR; R_{pcb1}, R_{pcb2} and R_{pcb3} are parasitic PCB DCR between the inductor output side pad and the output voltage rail; and I_{L1}, I_{L2} and I_{L3} are inductor average currents.

The controller will adjust the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus to achieve $I_{L1} = I_{L2} = I_{L3}$, when there are $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Using the same components for L1, L2 and L3 will provide a good match of R_{dcr1}, R_{dcr2} and R_{dcr3}. Board layout will determine

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R_{pcb1}, R_{pcb2} and R_{pcb3}. It is recommended to have symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

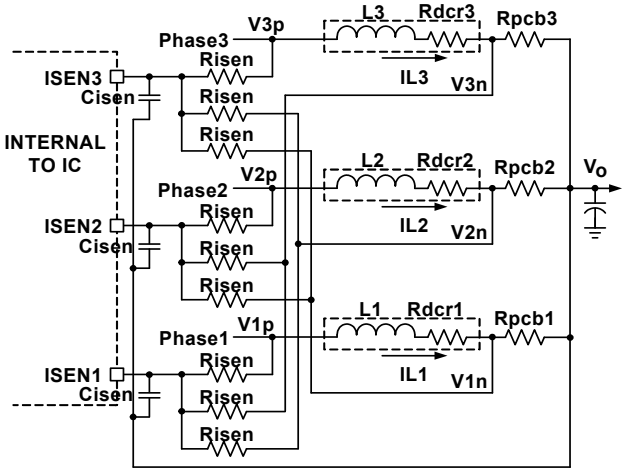


FIGURE 10. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Sometimes, it is difficult to implement symmetrical layout. For the circuit shown in Figure 9, asymmetric layout causes different R_{pcb1}, R_{pcb2} and R_{pcb3} thus current imbalance. Figure 10 shows a recommended differential-sensing current balancing circuit. The current sensing traces should be routed to the inductor pads so they only pick up the inductor DCR voltage. Each ISEN pin sees the average voltage of three sources: its own phase inductor phase-node pad, and the other two phases inductor output side pads. Equations 8 thru 10 give the ISEN pin voltages:

$$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n} \quad \text{(EQ. 8)}$$

$$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 9)}$$

$$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 10)}$$

The controller will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, as shown in Equations 11 and 12:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 11)}$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 12)}$$

Rewriting Equation 11 gives Equation 13:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 13)}$$

and rewriting Equation 12 gives Equation 14:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 14)}$$

Combining Equations 13 and 14 gives:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 15)}$$

Therefore:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad \text{(EQ. 16)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) will be achieved when there is $R_{dcr1} = R_{dcr2} = R_{dcr3}$. R_{pcb1}, R_{pcb2} and R_{pcb3} will not have any effect.

Since the slave ripple capacitor voltages mimic the inductor currents, R^{3}™ modulator can naturally achieve excellent current balancing during steady state and dynamic operations. Figure 11 shows current balancing performance of the evaluation board with load transient of 12A/51A at different rep rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at low rep rate, but cannot keep up when the rep rate gets into the hundred-kHz range, where it's out of the control loop bandwidth. The controller achieves excellent current balancing in all cases.

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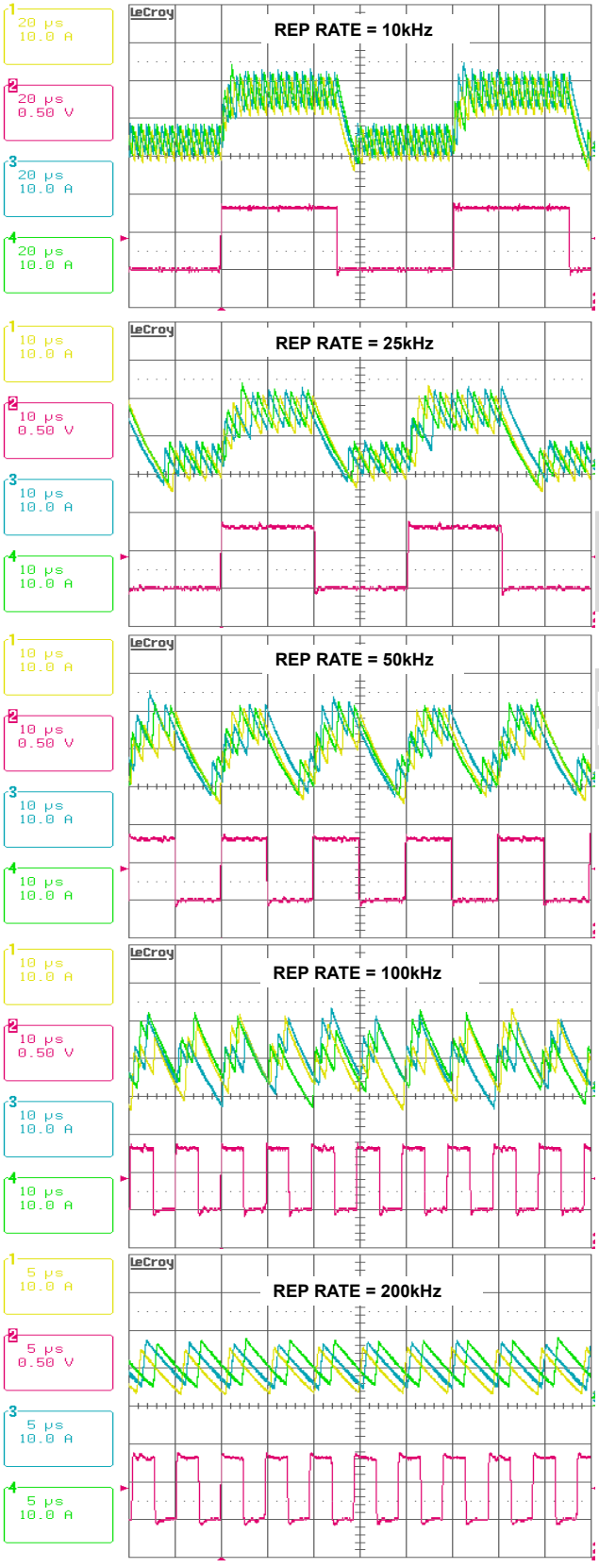


FIGURE 11. CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: IL1, CH2: I_{LOAD}, CH3: IL2, CH4: IL3

CCM Switching Frequency

The resistor form COMPG and GND sets four different switching frequencies: 300kHz, 350kHz, 400kHz and 450kHz. Please refer Table 8 for details.

Modes of Operation

TABLE 2. VR1 MODES OF OPERATION

PWM3	ISEN2	CONFIG.	PS	MODE	OCP Threshold (µA)
To External Driver	To Power Stage	3-phase CPU VR Config.	0	3-phase CCM	60
			1	2-phase CCM	40
			2	1-phase DE	20
			3		
Tied to 5V		2-phase CPU VR Config.	0	2-phase CCM	60
			1	1-phase CCM	30
			2	1-phase DE	
			3		
	Tied to 5V	1-phase CPU VR Config.	0	1-phase CCM	60
			1		
			2	1-phase DE	
			3		

VR1 can be configured for 3, 2 or 1-phase operation. Table 2 shows VR1 configurations and operational modes, programmed by the PWM3 pin and the ISEN2 pin status, and the PS command. For 2-phase configuration, tie the PWM3 pin to 5V. In this configuration, phases 1 and 2 are active. For 1-phase configuration, tie the PWM3 pin and the ISEN2 pin to 5V. In this configuration, only phase-1 is active.

In 3-phase configuration, VR1 operates in 3-phase CCM in PS0. It enters 2-phase CCM in PS1 by dropping phase 3 and reducing the overcurrent and the way-overcurrent protection levels to 2/3 of the initial values. It enters 1-phase DE mode in PS2 or PS3 by dropping phases 3 and 2, and reduces the overcurrent and the way-overcurrent protection levels to 1/3 of the initial values.

In 2-phase configuration, VR1 operates in 2-phase CCM in PS0. It enters 1-phase CCM in PS1 and enters 1-phase DE mode in PS2 or PS3 by dropping phase 2, and reducing the overcurrent and the way-overcurrent protection levels to 1/2 of the initial values.

In 1-phase configuration, VR1 operates in 1-phase CCM in PS0 and PS1, and enters 1-phase DE mode in PS2 and PS3.

TABLE 3. VR2 MODES OF OPERATION

ISEN2G	PS	MODE	OCP Threshold (µA)
To Power Stage	0	2-phase CCM	60
	1	1-phase CCM	30
	2	1-phase DE	
	3		

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TABLE 3. VR2 MODES OF OPERATION

ISEN2G	PS	MODE	OCP Threshold (µA)
Tied to 5V	0	1-phase CCM	60
	1		
	2	1-phase DE	
	3		

Table 3 shows VR2 operational modes, programmed by the ISEN2G pin status and PS command. For 2-phase configuration, connect the ISEN2G pin to power stage. In this configuration, phases 1 and 2 are active. For 1-phase configuration, tie tthe ISEN2G pin to 5V. In this configuration, only phase-1 is active.

VR2 can be disabled completely by tying ISUMNG to 5V, and all communication to VR2 will be rejected.

Dynamic Operation

VR1 and VR2 behave the same during dynamic operation. The controller responds to VID changes by slewing to the new voltage at a slew rate indicated in the SetVID command. There are three SetVID slew rates, namely SetVID_fast, SetVID_slow and SetVID_decay.

SetVID_fast command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a minimum 10mV/µs slew rate.

SetVID_slow command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a minimum 2.5mV/µs slew rate.

SetVID_decay command prompts the controller to enter DE mode. The output voltage will decay down to the new VID value at a slew rate determined by the load. If the voltage decay rate is too fast, the controller will limit the voltage slew rate at SetVID_slow slew rate.

ALERT# will be asserted low at the end of SetVID_fast and SetVID_slow VID transitions.

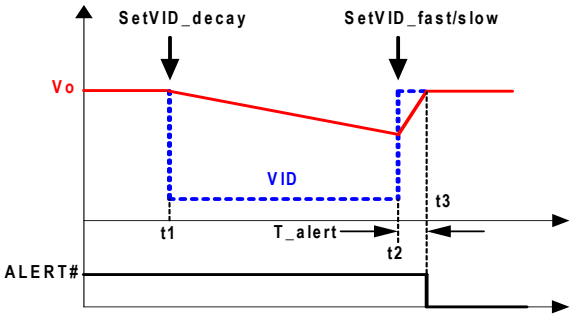


FIGURE 12. SETVID DECAY PRE-EMPTIVE BEHAVIOR

Figure 12 shows SetVID Decay Pre-Emptive behavior. The controller receives a SetVID_decay command at t1. The VR enters DE mode and the output voltage Vo decays down slowly. At t2, before Vo reaches the intended VID target of the SetVID_decay command, the controller receives a SetVID_fast (or SetVID_slow) command to go to a voltage higher than the actual Vo. The controller will turn around immediately and slew Vo to the new target voltage at the slew rate specified by the SetVID command. At t3, Vo reaches the new target voltage and the controller asserts the ALERT# signal.

The R$^{3™}$ modulator intrinsically has voltage feed-forward. The output voltage is insensitive to a fast slew rate input voltage change.

VR_HOT#/ALERT# Behavior

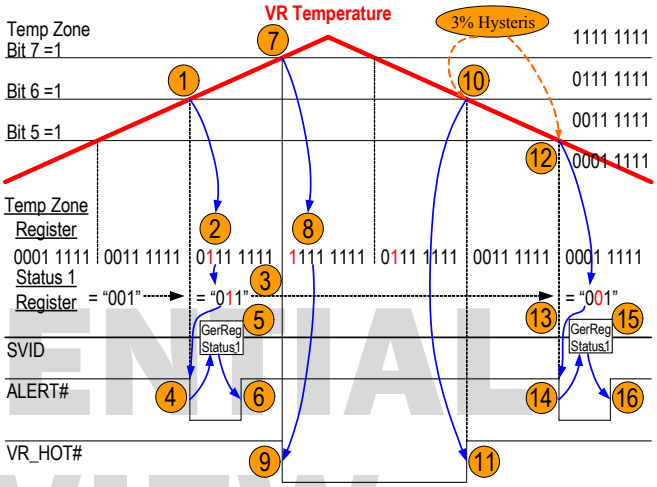


FIGURE 13. VR_HOT#/ALERT# BEHAVIOR

The controller drives 60µA current source out of the NTC pin and the NTCG pin alternatively at 1kHz frequency with 50% duty cycle. The current source flows through the respective NTC resistor networks on the pins and creates voltages that are monitored by the controller through an A/D converter (ADC) to generate the Tzone value. Table 4 shows the programming table for Tzone. The user needs to scale the NTC and the NTCG network resistance such that it generates the NTC (and NTCG) pin voltage that corresponds to the left-most column. Do not use any capacitor to filter the voltage.

TABLE 4. TZONE TABLE

VNTC (V)	TMAX (%)	TZONE
0.84	>100	FFh
0.88	100	FFh
0.92	97	7Fh
0.96	94	3Fh
1.00	91	1Fh
1.04	88	0Fh
1.08	85	07h
1.12	82	03h
1.16	79	01h
1.2	76	01h
>1.2	<76	00h

Figure 13 shows the how the NTC and the NTCG network should be designed to get correct VR_HOT#/ALERT# behavior when the system temperature rises and falls, manifested as the NTC and the NTCG pin voltage falls and rises. The series of events are:

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1. The temperature rises so the NTC pin (or the NTCG pin) voltage drops. Tzone value changes accordingly.
2. The temperature crosses the threshold where Tzone register Bit 6 changes from 0 to 1.
3. The controller changes Status_1 register bit 1 from 0 to 1.
4. The controller asserts ALERT#.
5. The CPU reads Status_1 register value to know that the alert assertion is due to Tzone register bit 6 flipping.
6. The controller clears ALEERT#.
7. The temperature continues rising.
8. The temperature crosses the threshold where Tzone register Bit 7 changes from 0 to 1.
9. The controllers asserts VR_HOT# signal. The CPU throttles back and the system temperature starts dropping eventually.
10. The temperature crosses the threshold where Tzone register bit 6 changes from 1 to 0. This threshold is 1 ADC step lower than the one when VR_HOT# gets asserted, to provide 3% hysteresis.
11. The controllers de-asserts VR_HOT# signal.
12. The temperature crosses the threshold where Tzone register bit 5 changes from 1 to 0. This threshold is 1 ADC step lower than the one when ALERT# gets asserted during the temperature rise to provide 3% hysteresis.
13. The controller changes Status_1 register bit 1 from 1 to 0.
14. The controller asserts ALERT#.
15. The CPU reads Status_1 register value to know that the alert assertion is due to Tzone register bit 5 flipping.
16. The controller clears ALERT#.

FB2 Function

The FB2 function is only available for VR1 in 2-phase configuration.

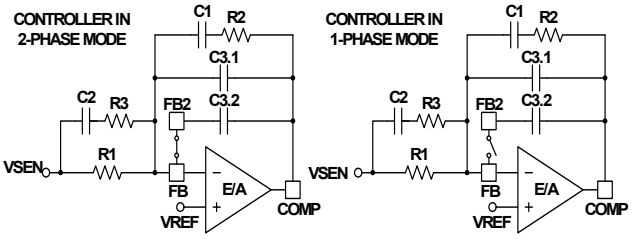


FIGURE 14. FB2 FUNCTION

Figure 14 shows the FB2 function. A switch (called FB2 switch) turns on to short the FB and the FB2 pins when the controller is in 2-phase mode. Capacitors C3.1 and C3.2 are in parallel, serving as part of the compensator. When the controller enters 1-phase mode, the FB2 switch turns off, removing C3.2 and leaving only C3.1 in the compensator. The compensator gain will increase with the removal of C3.2. By properly sizing C3.1 and C3.2, the compensator cab be optimal for both 2-phase mode and 1-phase mode.

When the FB2 switch is off, C3.2 is disconnected from the FB pin. However, the controller still actively drives the FB2 pin voltage to follow the FB pin voltage such that C3.2 voltage always follows C3.1 voltage. When the controller turns on the FB2 switch, C3.2 will be reconnected to the compensator smoothly.

The FB2 function ensures excellent transient response in both 2-phase mode and 1-phase mode. If one decides not to use the FB2 function, simply populate C3.1 only.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative and the amount is the MOSFET $r_{DS(ON)}$ voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero-crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it'll flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it'll flow through the high-side MOSFET body diode, causing the phase node to have a spike until it decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET and adjusts the phase comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 40ns to minimize the body diode-related loss.

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Protections

VR1 and VR2 both provide overcurrent, current-balance and overvoltage fault protections. The controller also provides over-temperature protection. The following discussion is based on VR1 and also applies to VR2.

The controller determines overcurrent protection (OCP) by comparing the average value of the droop current I_{droop} with an internal current source threshold as Table 2 shows. It declares OCP when I_{droop} is above the threshold for 120µs.

For overcurrent conditions above 1.5x the OCP level, the PWM outputs will immediately shut off and PGOOD will go low to maximize protection. This protection is also referred to as way-overcurrent protection or fast-overcurrent protection, for short-circuit protection.

The controller monitors the ISEN pin voltages to determine current-balance protection. If the ISEN pin voltage difference is greater than 9mV for 1ms, the controller will declare a fault and latch off.

The controller takes the same actions for all of the above fault protections: de-assertion of both PGOODs and turn-off of all the high-side and low-side power MOSFETs. Any residual inductor current will decay through the MOSFET body diodes.

The controller will declare an overvoltage fault and de-assert PGOOD if the output voltage exceeds the VID set value by +200mV. The controller will immediately declare an OV fault, de-assert PGOOD, and turn on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below the VID set value when all power MOSFETs are turned off. If the output voltage rises above the VID set value +200mV again, the protection process is repeated. This behavior provides the

maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground.

The overvoltage fault threshold is 1.7V when output voltage ramps up from 0V. And the overvoltage fault threshold is restored to VID set value + 200mV after the output voltage settles.

All the above fault conditions can be reset by bringing VR_ON low or by bringing V_{DD} below the POR threshold. When VR_ON and V_{DD} return to their high operating levels, a soft-start will occur

Table 5 summarizes the fault protections.

TABLE 5. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	120µs	PWM tri-state, PGOOD latched low	VR_ON toggle or VDD toggle
Phase Current Unbalance	1ms		
Way-Overcurrent (1.5x0C)	Immediately		
Overvoltage +200mV		PGOOD latched low. Actively pulls the output voltage to below VID value, then tri-state.	

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Supported Data And Configuration Registers

The controller supports the following data and configuration registers.

TABLE 6. SUPPORTED DATA AND CONFIGURATION REGISTERS

Index	Register Name	Description	Default Value
00h	Vendor ID	Uniquely identifies the VR vendor. Assigned by Intel.	12h
01h	Product ID	Uniquely identifies the VR product. Intersil assigns this number.	1Fh
02h	Product Revision	Uniquely identifies the revision of the VR control IC. Intersil assigns this data.	
05h	Protocol ID	Identifies what revision of SVID protocol the controller supports.	01h
06h	Capability	Identifies the SVID VR capabilities and which of the optional telemetry registers are supported.	81h
10h	Status_1	Data register read after ALERT# signal. Indicating if a VR rail has settled, has reached VRHOT condition or has reached ICC max.	00h
11h	Status_2	Data register showing status_2 communication.	00h
12h	Temperature Zone	Data register showing temperature zones that have been entered.	00h
1Ch	Status_2_ LastRead	This register contains a copy of the Status_2 data that was last read with the GetReg (Status_2) command.	00h
21h	ICC max	Data register containing the ICC max the platform supports, set at start-up by resistors Rprog1 and Rprog2. The platform design engineer programs this value during the design process. Binary format in amps, i.e. 100A = 64h	Refer to Table 7
22h	Temp max	Data register containing the temperature max the platform support, set at startup by resistor Rprog2. The platform design engineer programs this value during the design process. Binary format in degree C, i.e. 100C = 64h	Refer to Table 8
24h	SR-fast	Slew Rate Normal. The fastest slew rate the platform VR can sustain. Binary format in mV/µs. i.e. 0Ah = 10mV/µs.	0Ah
25h	SR-slow	Is 4x slower than normal. Binary format in mV/µs. i.e. 02h = 2.5mV/µs	02h
26h	Vboot	If programmed by the platform, the VR supports Vboot voltage during start-up ramp. The VR will ramp to V_{BOOT} and hold at V_{BOOT} until it receives a new SetVID command to move to a different voltage.	00h
30h	Vout max	This register is programmed by the master and sets the maximum VID the VR will support. If a higher VID code is received, the VR will respond with “not supported” acknowledge.	FBh
31h	VID Setting	Data register containing currently programmed VID voltage. VID data format.	00h
32h	Power State	Register containing the current programmed power state.	00h

TABLE 6. SUPPORTED DATA AND CONFIGURATION REGISTERS (Continued)

Index	Register Name	Description	Default Value
33h	Voltage Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is a sign bit, 0 = positive margin, 1 = negative margin. Remaining 7 bits are # VID steps for the margin. 00h = no margin, 01h = +1 VID step 02h = +2 VID steps...	00h
34h	Multi VR Config	Data register that configures multiple VRs behavior on the same SVID bus.	VR1: 00h VR2: 01h

Key Component Selection

Inductor DCR Current-Sensing Network

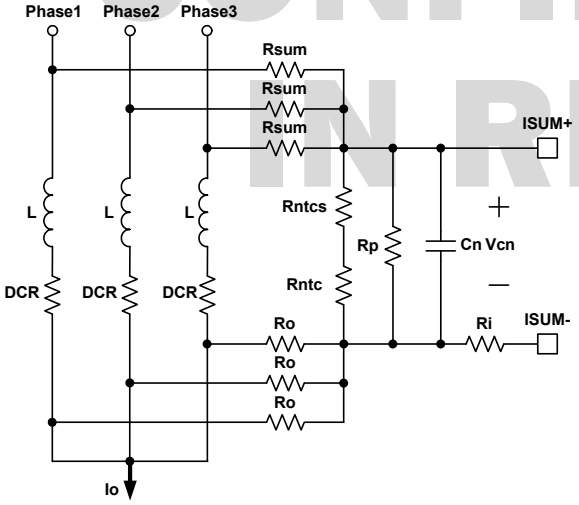


FIGURE 15. DCR CURRENT-SENSING NETWORK

Figure 15 shows the inductor DCR current-sensing network for a 3-phase solution. An inductor current flows through the DCR and creates a voltage drop. Each inductor has two resistors in R_{sum} and R_o connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{sum} and R_o resistors are connected in a summing network as shown, and feed the total current information to the NTC network (consisting of R_{ntcs}, R_{ntc} and R_p) and capacitor C_n. R_{ntc} is a negative temperature coefficient (NTC) thermistor, used to temperature-compensate the inductor DCR change.

The inductor output side pads are electrically shorted in the schematic, but have some parasitic impedance in actual board layout, which is why one cannot simply short them together for the current-sensing summing network. It is recommended to use 1Ω~10Ω R_o to create quality signals. Since R_o value is much smaller than the rest of the current sensing circuit, the following analysis will ignore it for simplicity.

The summed inductor current information is presented to the capacitor C_n. Equations 17 thru 21 describe the frequency-domain relationship between inductor total current $I_o(s)$ and C_n voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad \text{(EQ. 17)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad \text{(EQ. 18)}$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 19)}$$

$$\omega_L = \frac{DCR}{L} \quad \text{(EQ. 20)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n} \quad \text{(EQ. 21)}$$

where N is the number of phases.

Transfer function $A_{cs}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, giving higher reading of the inductor DC current. The NTC R_{ntc} values decrease as its temperature decreases. Proper selections of R_{sum}, R_{ntcs}, R_p and R_{ntc} parameters ensure that V_{Cn} represent the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. It is recommended to have a higher ratio of V_{cn} to the inductor DCR voltage, so the droop circuit has higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ and R_{ntc} = 10kΩ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. One can apply full load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is recommended to follow the Intersil evaluation board layout and current-sensing network parameters to minimize engineering time.

$V_{Cn}(s)$ also needs to represent real-time $I_o(s)$ for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ has a pole w_{sns} and a zero w_L. One needs to match w_L and w_{sns} so $A_{cs}(s)$ is unity gain at all frequencies. By forcing w_L equal to w_{sns} and solving for the solution, Equation 22 gives Cn value.

$$C_n = \frac{L}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad \text{(EQ. 22)}$$

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For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.9mΩ and L = 0.36µH, Equation 22 gives C_n = 0.397µF.

Assuming the compensator design is correct, Figure 16 shows the expected load transient response waveforms if C_n is correctly selected. When the load current I_{core} has a square change, the output voltage V_{core} also has a square response.

If C_n value is too large or too small, $V_{Cn}(s)$ will not accurately represent real-time $I_o(s)$ and will worsen the transient response. Figure 17 shows the load transient response when C_n is too small. V_{core} will sag excessively upon load insertion and may create a system failure. Figure 18 shows the transient response when C_n is too large. V_{core} is sluggish in drooping to its final value. There will be excessive overshoot if load insertion occurs during this time, which may potentially hurt the CPU reliability.

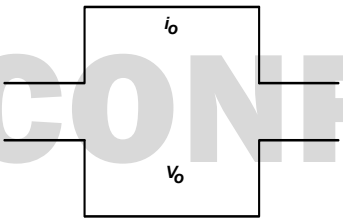


FIGURE 16. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

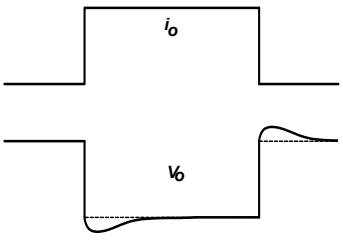


FIGURE 17. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

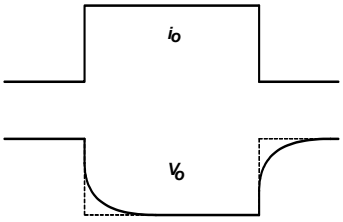


FIGURE 18. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

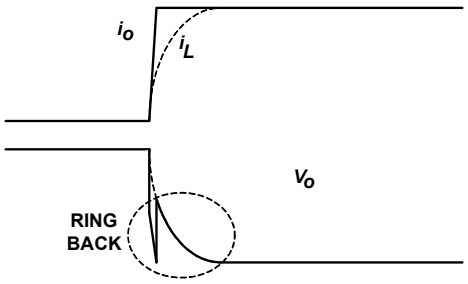


FIGURE 19. OUTPUT VOLTAGE RING BACK PROBLEM

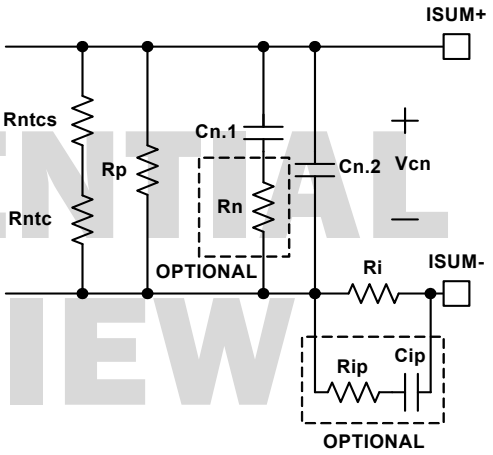


FIGURE 20. OPTIONAL CIRCUITS FOR RING BACK REDUCTION

Figure 19 shows the output voltage ring back problem during load transient response. The load current i_o has a fast step change, but the inductor current i_L cannot accurately follow. Instead, i_L responds in first order system fashion due to the nature of current loop. The ESR and ESL effect of the output capacitors makes the output voltage V_o dip quickly upon load current change. However, the controller regulates V_o according to the droop current i_{droop}, which is a real-time representation of i_L; therefore it pulls V_o back to the level dictated by i_L, causing the ring back problem. This phenomenon is not observed when the output capacitor have very low ESR and ESL, such as all ceramic capacitors.

Figure 20 shows two optional circuits for reduction of the ring back.

C_n is the capacitor used to match the inductor time constant. It usually takes the parallel of two (or more) capacitors to get the desired value. Figure 20 shows that two capacitors $C_{n.1}$ and $C_{n.2}$ are in parallel. Resistor R_n is an optional component to reduce the V_o ring back. At steady state, $C_{n.1}$ + $C_{n.2}$ provides the desired C_n capacitance. At the beginning of i_o change, the effective capacitance is less because R_n increases the impedance of the $C_{n.1}$ branch. As Figure 17 explains, V_o tends to dip when C_n is too small, and this effect will reduce the V_o ring back. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when R_n is bigger. However, the presence of R_n increases the ripple of the V_n signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. R_n value

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usually is a few ohms. $C_{n.1}$, $C_{n.2}$ and R_n values should be determined through tuning the load transient response waveforms on an actual board.

R_{ip} and C_{ip} form an R-C branch in parallel with R_i, providing a lower impedance path than R_i at the beginning of i_o change. R_{ip} and C_{ip} do not have any effect at steady state. Through proper selection of R_{ip} and C_{ip} values, i_{droop} can resemble i_o rather than i_L, and V_o will not ring back. The recommended value for R_{ip} is 100Ω. C_{ip} should be determined through tuning the load transient response waveforms on an actual board. The recommended range for C_{ip} is 100pF~2000pF. However, it should be noted that the R_{ip} -C_{ip} branch may distort the i_{droop} waveform. Instead of being triangular as the real inductor current, i_{droop} may have sharp spikes, which may adversely affect i_{droop} average value detection and therefore may affect OCP accuracy. User discretion is advised.

Resistor Current-Sensing Network

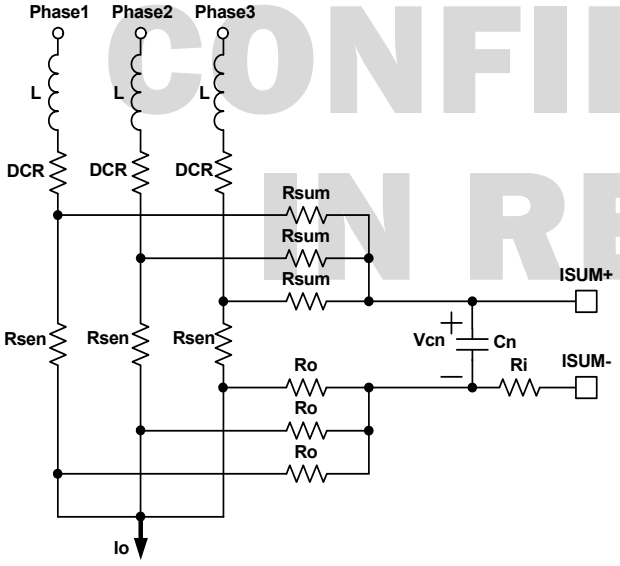


FIGURE 21. RESISTOR CURRENT-SENSING NETWORK

Figure 21 shows the resistor current-sensing network for a 2-phase solution. Each inductor has a series current-sensing resistor R_{sen}. R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n. R_{sum} and C_n form a a filter for noise attenuation. Equations 23 thru 25 give $V_{Cn}(s)$ expression:

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{Rsen}(s) \quad \text{(EQ. 23)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{Rsen}}} \quad \text{(EQ. 24)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 25)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. Current-sensing resistor R_{sen} value will not have significant variation over-temperature, so there is no need for the NTC network.

The recommended values are R_{sum} = 1kΩ and C_n = 5600pF.

Overcurrent Protection

Refer to Equation 1 on page 17 and Figures 15, 19 and 21; resistor R_i sets the droop current I_{droop}. Tables 2 and 3 show the internal OCP threshold. It is recommended to design I_{droop} without using the R_{comp} resistor.

For example, the OCP threshold is 60µA for 3-phase solution. We will design I_{droop} to be 40.9µA at full load, so the OCP trip level is 1.5x of the full load current.

For inductor DCR sensing, Equation 26 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o \quad \text{(EQ. 26)}$$

Substitution of Equation 26 into Equation 1 gives Equation 27:

$$I_{droop} = \frac{1}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \quad \text{(EQ. 27)}$$

Therefore:

$$R_i = \frac{R_{ntcnet} \times DCR \times I_o}{N \times \left(R_{ntcnet} + \frac{R_{sum}}{N} \right) \times I_{droop}} \quad \text{(EQ. 28)}$$

Substitution of Equation 18 and application of the OCP condition in Equation 28 gives Equation 29:

$$R_i = \frac{\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{N \times \left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + \frac{R_{sum}}{N} \right) \times I_{droopmax}} \quad \text{(EQ. 29)}$$

where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.9mΩ, I_{omax} = 94A and $I_{droopmax}$ = 48µA, Equation 29 gives R_i = 487Ω.

For resistor sensing, Equation 30 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 30)}$$

Substitution of Equation 30 into Equation 1 gives Equation 31:

$$I_{droop} = \frac{1}{R_i} \times \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 31)}$$

Therefore:

$$R_i = \frac{R_{sen} \times I_o}{N \times I_{droop}} \quad \text{(EQ. 32)}$$

Substitution of Equation 32 and application of the OCP condition in Equation 28 gives Equation 33:

$$R_i = \frac{R_{sen} \times I_{omax}}{N \times I_{droopmax}} \quad \text{(EQ. 33)}$$

where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given N = 3,

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R_{sen} = 1mΩ, I_{omax} = 94A and $I_{droopmax}$ = 48µA, Equation 33 gives R_i = 652Ω.

Load Line Slope

Refer to Figure 8.

For inductor DCR sensing, substitution of Equation 27 into Equation 2 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \quad \text{(EQ. 34)}$$

For resistor sensing, substitution of Equation 31 into Equation 2 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{R_{sen} \times R_{droop}}{N \times R_i} \quad \text{(EQ. 35)}$$

Substitution of Equation 28 and rewriting Equation 34, or substitution of Equation 32 and rewriting Equation 35 give the same result in Equation 36:

$$R_{droop} = \frac{I_o}{I_{droop}} \times LL \quad \text{(EQ. 36)}$$

One can use the full load condition to calculate R_{droop}. For example, given I_{omax} = 94A, $I_{droopmax}$ = 48µA and LL = 1.9mΩ, Equation 36 gives R_{droop} = 3.72kΩ.

It is recommended to start with the R_{droop} value calculated by Equation 36, and fine tune it on the actual board to get accurate load line slope. One should record the output voltage readings at no load and at full load for load line slope calculation. Reading the output voltage at lighter load instead of full load will increase the measurement error.

Compensator

Figure 16 shows the desired load transient response waveforms. Figure 22 shows the equivalent circuit of a voltage regulator (VR) with the droop function. A VR is equivalent to a voltage source (= VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope LL, i.e. constant output impedance, in the entire frequency range, V_o will have square response when I_o has a square change.

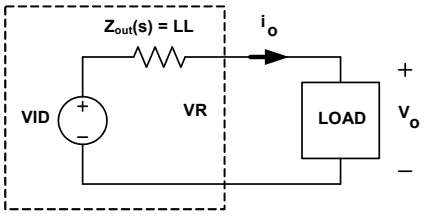


FIGURE 22. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

Intersil provides a Microsoft Excel-based spreadsheet to help design the compensator and the current sensing network, so the VR achieves constant output impedance as a stable system. Please go to www.intersil.com/design/ to request spreadsheet. Figure 26 shows a screenshot of the spreadsheet.

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 23 conceptually shows T1(s) measurement set-up and Figure 24 conceptually shows T2(s) measurement set-up. The VR senses the inductor current, multiplies it by a gain of the load line slope, then adds it on top of the sensed output voltage and feeds it to the compensator. T(1) is measured after the summing node, and T2(s) is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) can be actually measured on an ISL95836 regulator.

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s) and has more meaning of system stability.

T2(s) is the voltage loop gain with closed droop loop. It has more meaning of output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin, and output impedance equal or smaller than the load line slope.

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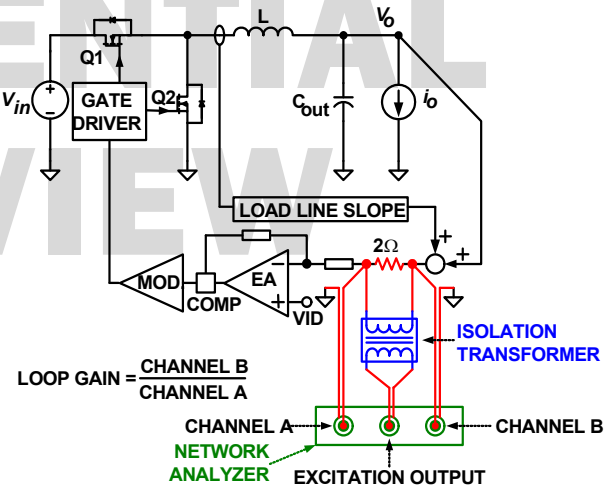


FIGURE 23. LOOP GAIN T1(s) MEASUREMENT SET-UP

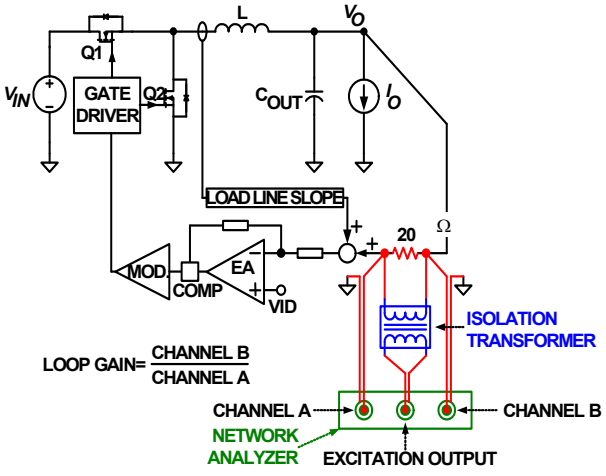


FIGURE 24. LOOP GAIN T2(s) MEASUREMENT SET-UP

Programming Resistors

TABLE 7. RCOMP PROGRAMMING TABLE

RCOMP (kohm)				
Min.	Typ.	Max.	V_{BOOT} (V)	VR1 ICCMAX (A)
0	3.2		0	99
	5.714		0	94
	9.224		0	80
	13.33		0	70
	17.143		0	60
	20.952		0	53
	24.762		0	48
	28.571		0	43
	32.381		0	38
	36.19		0	38
	41.9		0	33
	49.52		0	24
	57.14		0	18
	64.76		1.1	18
	72.38		1.1	24
	80		1.1	33
	89.52		1.1	38
	100.952		1.1	43
	112.381		1.1	48
	123.81		1.1	53
	137.14		1.1	60
	152.38		1.1	70
	167.62		1.1	18
	184.76		1.1	24
	275	open	1.1	33

TABLE 8. RCOMPG PROGRAMMING TABLE

RCOMPG (kΩ)			SWITCHING FREQUENCY (kHz)	VR2 ICCMAX (A)
Min.	Typ.	Max.		
0	3.2		450	70
	5.714		450	57
	9.224		450	45
	13.33		450	33
	17.143		450	24
	20.952		450	18
	24.762		400	18
	28.571		400	24
	32.381		400	33
	36.19		400	33
	41.9		400	45
	49.52		400	57

TABLE 8. RCOMPG PROGRAMMING TABLE

RCOMPG (kΩ)			SWITCHING FREQUENCY (kHz)	VR2 ICCMAX (A)
Min.	Typ.	Max.		
	57.14		400	70
	64.76		350	70
	72.38		350	57
	80		350	45
	89.52		350	33
	100.952		350	24
	112.381		350	18
	123.81		300	18
	137.14		300	24
	152.38		300	33
	167.62		300	45
	184.76		300	57
	275	open	300	70

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There are two programming resistors: R_{COMP} and R_{COMPG}. Table 7 shows how to select R_{COMP} based on V_{BOOT} and VR1 ICCMAX register settings. VR1 can power to 0V V_{BOOT} or an internally-set V_{BOOT} based on R_{COMP} value. When the controller works with an actual CPU, select R_{COMP} such that VR1 powers up to V_{BOOT} = 0V as required by the SVID command. In the absence of a CPU, such as testing of the VR alone, select R_{COMP} such that VR1 powers up to the internally-set V_{BOOT}, which by default is 1.1V. Determine the maximum current VR1 can support and set the VR1 ICCMAX register value accordingly by selecting the appropriate R_{COMP} value. The CPU will read the VR1 ICCMAX register value and ensure that the CPU CORE current doesn't exceed the value specified by VR1 ICCMAX.

Table 8 shows how to select R_{COMP} based on VR1 and VR2 CCM switching frequency and VR2 ICCMAX register settings. There are four switching frequecies to choose from: 300kHz, 350kHz, 400kHz, and 450kHz. There are also six VR2 ICCMAX values to choose.

Current Balancing

Refer to Figures 1 thru 2. The controller achieves current balancing through matching the ISEN pin voltages. R_{isen} and C_{isen} form filters to remove the switching ripple of the phase node voltages. It is recommended to use rather long $R_{isen}C_{isen}$ time constant such that the ISEN voltages have minimal ripple and represent the DC current flowing through the inductors. Recommended values are R_s = 10kΩ and C_s = 0.22µF.

Slew Rate Compensation Circuit For VID Transition

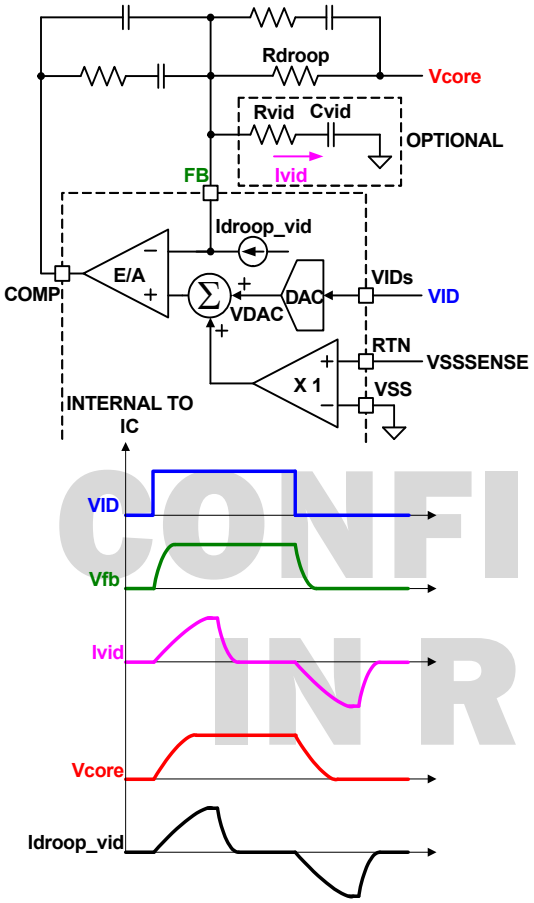


FIGURE 25. SLEW RATE COMPENSATION CIRCUIT FOR VID TRANSITION

During a large VID transition, the DAC steps through the VIDs at a controlled slew rate. For example, the DAC may change a tick (5mV) per 0.5µs, controlling output voltage V_{core} slew rate at 10mV/µs.

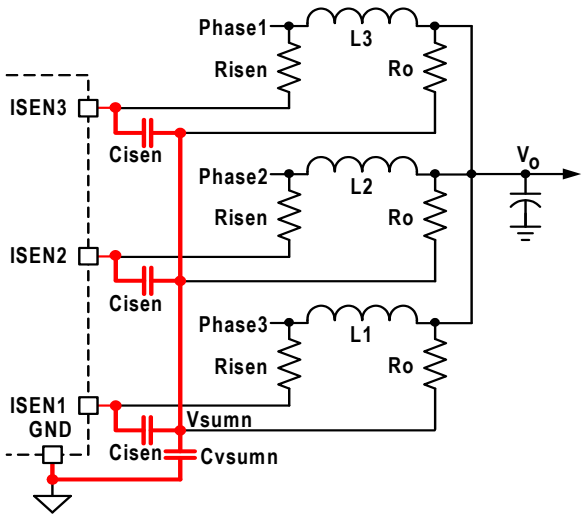
Figure 25 shows the waveforms of VID transition. During VID transition, the output capacitor is being charged and discharged, causing C_{out} x dV_{core}/dt current on the inductor. The controller senses the inductor current increase during the up transition, as the I_{droop_vid} waveform shows, and will droop the output voltage V_{core} accordingly, making V_{core} slew rate slow. Similar behavior occurs during the down transition. To get the correct V_{core} slew rate during VID transition, one can add the R_{vid}-C_{vid} branch, whose current I_{vid} cancels I_{droop_vid}.

It's recommended to choose the R, C values from the reference design as a starting point. then tweak the actual values on the board to get the best performance.

During normal transient response, the FB pin voltage is held constant, therefore is virtual ground in small signal sense. The R_{vid} - C_{vid} network is between the virtual ground and the real ground, and hence has no effect on transient response.

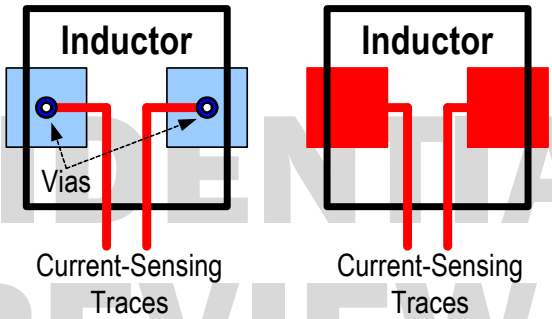
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Layout Guidelines

ISL95836 PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
BOTTOM PAD	GND	Connect this ground pad to the ground plane through low impedance path. Recommend use of at least 5 vias to connect to ground planes in PCB internal layers.
2	ISEN1G	Each ISEN pin has a capacitor (Cisen) decoupling it to VSUMNG, then through another capacitor (Cvsumng) to GND. Place Cisen capacitors as close as possible to the controller and keep the following loops small: 1. ISEN1G pin to ISEN2G pin 2. Any ISENG pin to GND
3	ISEN2G	
4	NTCG	The NTC thermistor needs to be placed close to the thermal source that is monitored to determine AXG Vcore thermal throttling. Recommend placing it at the hottest spot of the AXG Vcore VR.
5, 6, 7	SCLK, ALERT#, SDA	Follow Intel recommendation.
8	VR_HOT#	No special consideration.
9	VR_ON	No special consideration.
10	NTC	The NTC thermistor needs to be placed close to the thermal source that is monitored to determine CPU Vcore thermal throttling. Recommend placing it at the hottest spot of the CPU Vcore VR.
10	PGOOD	
9	NC	No special consideration.
10	VR_HOT#	No special consideration.
11	ISEN3	Each ISEN pin has a capacitor (Cisen) decoupling it to VSUMN, then through another capacitor (Cvsumn) to GND. Place Cisen capacitors as close as possible to the controller and keep the following loops small: 1. Any ISEN pin to another ISEN pin 2. Any ISEN pin to GND The red traces in the following drawing show the loops that need to minimized. 
12	ISEN2	
13	ISEN1	

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Layout Guidelines (Continued)

ISL95836 PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
14	ISUMP	Place the current sensing circuit in general proximity of the controller. Place capacitor Cn very close to the controller. Place the NTC thermistor next to VR1 phase-1 inductor (L1) so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of VSUMP and VSUMN signals to the controller. Run these two signals traces in parallel fashion with decent width (>20mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. Route R63 and R71 to VR1 phase-1 side pad of inductor L1. Route R88 to the output side pad of inductor L1. Route R65 and R72 to VR1 phase-2 side pad of inductor L2. Route R90 to the output side pad of inductor L2. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces. 
15	ISUMN	
16	RTN	Place the RTN filter in close proximity of the controller for good decoupling.
17	FB	Place the compensator components in general proximity of the controller.
18	COMP	
19	PGOOD	No special consideration.
20	BOOT1	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
21	UGATE1	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE1 trace to VR1 phase-1 high-side MOSFET (Q2 and Q8) source pins instead of general copper.
22	PHASE1	
23	LGATE1	Place the RTNG filter in close proximity of the controller for good decoupling.
24	PWM3	No special consideration.
25	VDD	A capacitor decouples it to GND. Place it in close proximity of the controller.
26	VCCP	A capacitor decouples it to GND. Place it in close proximity of the controller.
27	LGATE2	If available, run VSSP2 trace in parallel with LGATE2 trace. Use decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
28	PHASE2	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE2 trace to VR1 phase-2 high-side MOSFET (Q4 and Q10) source pins instead of general copper.
29	UGATE2	
30	BOOT2	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
31	BOOT1G	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
32	UGATE1G	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE1G trace to VR2 phase-1 high-side MOSFET source pins instead of general copper
33	PHASE1G	
34	LGATE1G	Use decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
35	PWM2G	No special consideration.
36	PGOODG	No special consideration.

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Layout Guidelines (Continued)

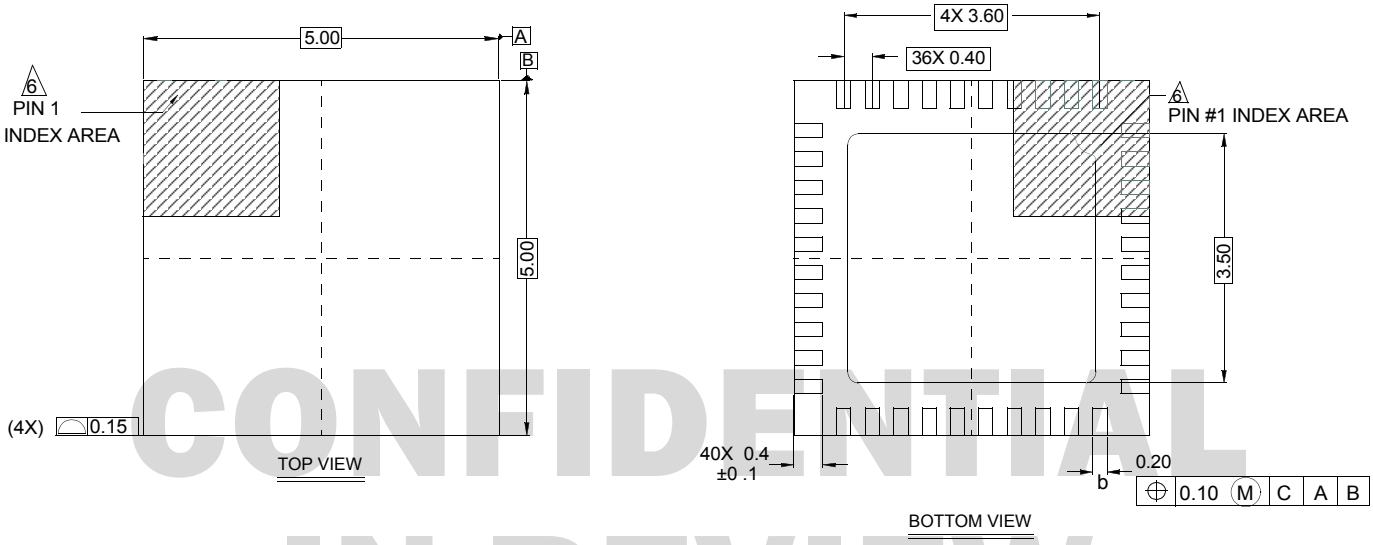
ISL95836 PIN NUMBER	SYMBOL	LAYOUT GUIDELINES
37	COMPG	Place the compensator components in general proximity of the controller.
38	FBG	
39	RTNG	Place the RTNG filter in close proximity of the controller for good decoupling.
40	ISUMNG	Place the current sensing circuit in general proximity of the controller. Place capacitor Cn very close to the controller. Place the NTC thermistor next to VR2 phase-1 inductor (L1) so it senses the inductor temperature correctly. See ISUMN and ISUMP pins for layout guidelines of current-sensing trace routing.
1	ISUMPG	

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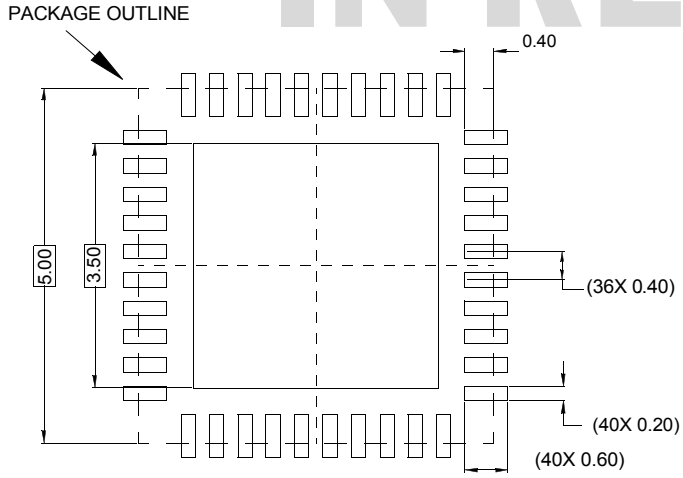
Package Outline Drawing

L40.5x5

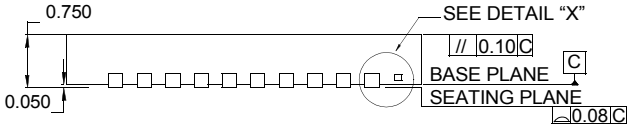
40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 4/07



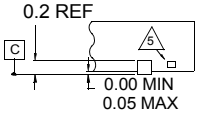
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TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
March 12, 2011	FN7835.0	Preliminary.

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