

Synchronous Buck NexFET™ Power Stage

FEATURES

- Over 92% System Efficiency at 15A
- Max Rated Continuous Current 25A, Peak 60A
- High Frequency Operation (up to 2 MHz)
- High Density - SON 3.5x4.5-mm Footprint
- Ultra Low Inductance Package
- System Optimized PCB Footprint
- Ultra Low Quiescent (ULQ) Current Mode
- 3.3V and 5V PWM Signal Compatible
- Diode Emulation Mode with FCCM
- Input Voltages up to 24V
- Three-State PWM Input
- Integrated Bootsrap Diode
- Shoot Through Protection
- RoHS Compliant – Lead Free Terminal Plating
- Halogen Free

APPLICATIONS

- Ultrabook/Notebook DC/DC Converters
- Multiphase Vcore and DDR Solutions
- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD97374Q4M	SON 3.5 × 4.5-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

DESCRIPTION

The CSD97374Q4M NexFET™ Power Stage is a highly optimized design for use in a high power, high density Synchronous Buck converter. This product integrates the driver IC and NexFET technology to complete the power stage switching function. The driver IC has a built-in selectable diode emulation function that enables DCM operation to improve light load efficiency. In addition, the driver IC supports ULQ mode that enables Connected Standby for Windows™ 8 . With the PWM input in tri-state, quiescent current is reduced to 130 µA, with immediate response. When SKIP# is held at tri-state, the current is reduced to 8 µA (typically 20 µs is required to resume switching). This combination produces a high current, high efficiency, and high speed switching device in a small 3.5 × 4.5-mm outline package. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

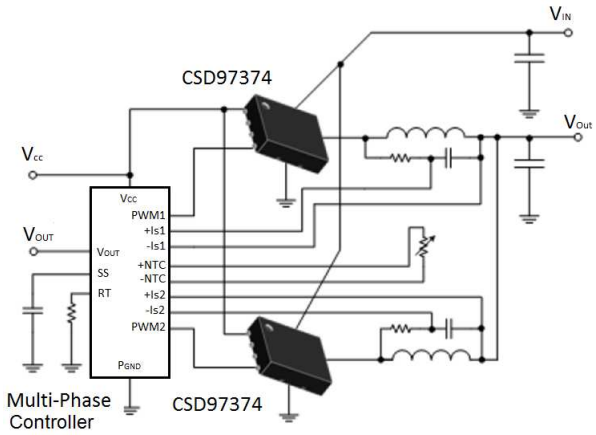


Figure 1. Application Diagram

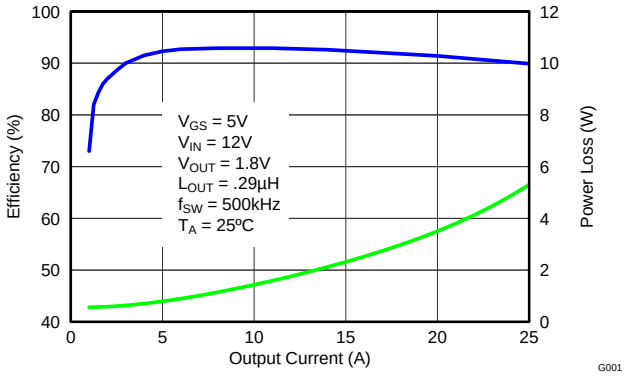


Figure 2. Efficiency and Power Loss

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

T_A = 25°C (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
V_{IN} to P_{GND}		-0.3	30	V
V_{SW} to P_{GND} , V_{IN} to V_{SW}		-0.3	30	V
V_{SW} to P_{GND}, V_{IN} to V_{SW} (<10ns)		-7	33	V
V_{DD} to P_{GND}		–0.3	6	V
PWM, SKIP# to P_{GND}		–0.3	6	V
BOOT to P_{GND}		–0.3	35	V
BOOT to P_{GND} (<10ns)		-2	38	V
BOOT to BOOT_R		–0.3	6	V
ESD Rating	Human Body Model (HBM)		2000	V
	Charged Device Model (CDM)		500	V
Power Dissipation, P_D			8	W
Operating Temperature Range, T_J		-40	150	°C
Storage Temperature Range, T_{STG}		–55	150	°C

(1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

T_A = 25° (unless otherwise noted)

Parameter	Conditions	MIN	MAX	UNIT
Gate Drive Voltage, V_{DD}		4.5	5.5	V
Input Supply Voltage, V_{IN}			24	V
Continuous Output Current, I_{OUT}	V_{IN} = 12V, V_{DD} = 5V, V_{OUT} = 1.8V, f_{SW} = 500kHz, L_{OUT} = 0.29µH(1)		25	A
Peak Output Current, I_{OUT-PK}(2)			60	A
Switching Frequency, f_{SW}	C_{BST} = 0.1µF (min)		2000	kHz
On Time Duty Cycle			85	%
Minimum PWM On Time		40		ns
Operating Temperature		–40	125	°C

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) System conditions as defined in Note 1. Peak Output Current is applied for t_p = 10ms, duty cycle ≤ 1%

THERMAL INFORMATION

T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Top of package)(1)			22.8	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board(2)			2.5	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45 -cm²), 2-oz (.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch, 0.06-inch (1.52-mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1mm of the package.

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ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = POR to 5.5V (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}					
Power Loss(1)	V_{IN} = 12V, V_{DD} = 5V, V_{OUT} = 1.8V, I_{OUT} = 15A, f_{SW} = 500kHz, L_{OUT} = 0.29µH , T_J = 25°C		2.3		W
Power Loss(2)	V_{IN} = 19V, V_{DD} = 5V, V_{OUT} = 1.8V, I_{OUT} = 15A, f_{SW} = 500kHz, L_{OUT} = 0.29µH , T_J = 25°C		2.5		W
Power Loss(2)	V_{IN} = 19V, V_{DD} = 5V, V_{OUT} = 1.8V, I_{OUT} = 15A, f_{SW} = 500kHz, L_{OUT} = 0.29µH , T_J = 125°C		2.8		W
V_{IN}					
V_{IN} Quiescent Current, I_Q	PWM=Floating, V_{DD} = 5V, V_{IN}= 24V			1	µA
V_{DD}					
Standby Supply Current, I_{DD}	PWM = Float, SKIP# = V_{DD} or 0V		130		µA
	SKIP# = Float		8		µA
Operating Supply Current, I_{DD}	PWM = 50% Duty cycle, f_{SW} = 500kHz		8.2		mA
POWER-ON RESET AND UNDER VOLTAGE LOCKOUT					
Power-On Reset, V_{DD} Rising				4.15	V
UVLO, V_{DD} Falling		3.7			V
Hysteresis			0.2		mV
PWM and SKIP# I/O Specifications					
Input Impedance, R_I	Pull Up to V_{DD}		1700		kΩ
	Pull Down (to GND)		800		
Logic Level High, V_{IH}		2.65			V
Logic Level Low, V_{IL}				0.6	
Hysteresis, V_{IH}			0.2		
Tri-State Voltage, V_{TS}		1.3		2	
Tri-state Activation Time (falling) PWM, $t_{THOLD(off1)}$			60		ns
Tri-state Activation Time (rising) PWM, $t_{THOLD(off2)}$			60		
Tri-state Activation Time (falling) SKIP#, t_{TSKF}			1		µs
Tri-state Activation Time (rising) SKIP#, t_{TSKR}			1		
Tri-state Exit Time PWM, $t_{3RD(PWM)}$(2)				100	ns
Tri-state Exit Time SKIP#, $t_{3RD(SKIP\#)}$(2)				50	µs
BOOTSTRAP SWITCH					
Forward Voltage, V_{FBST}	I_F = 10mA		120	240	mV
Reverse Leakage, I_{RLEAK}(2)	V_{BST} – V_{DD} = 25V			2	µA

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(2) Specified by design

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TYPICAL CHARACTERISTICS

T_J = 125°C, unless stated otherwise.

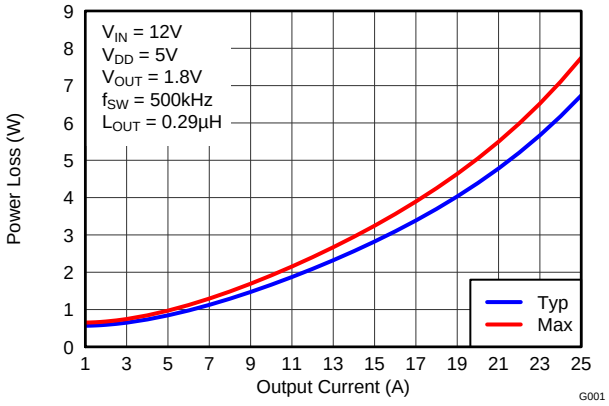


Figure 3. Power Loss vs Output Current

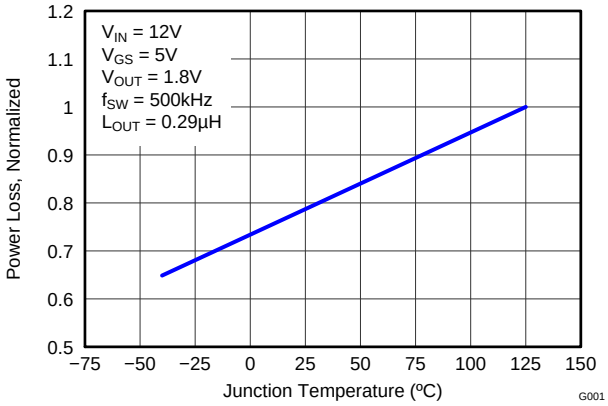


Figure 4. Power Loss vs Temperature

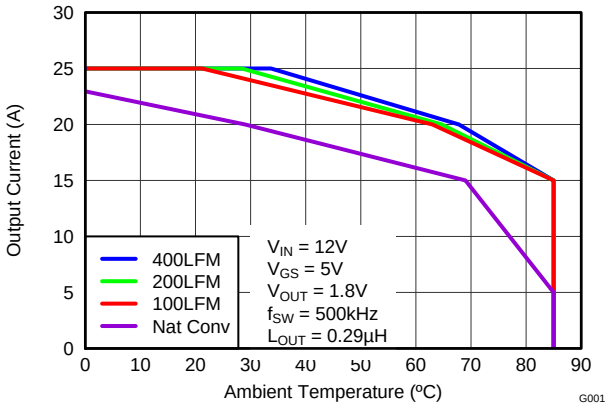


Figure 5. Safe Operating Area – PCB Horizontal Mount (1)

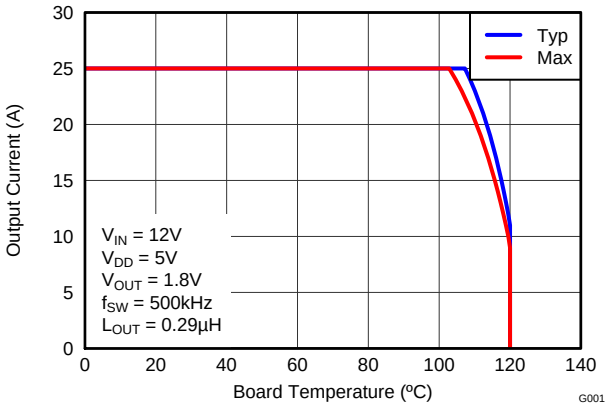


Figure 6. Typical Safe Operating Area (1)

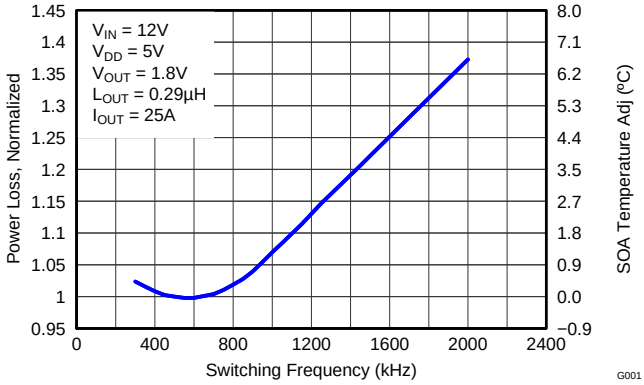


Figure 7. Normalized Power Loss vs Frequency

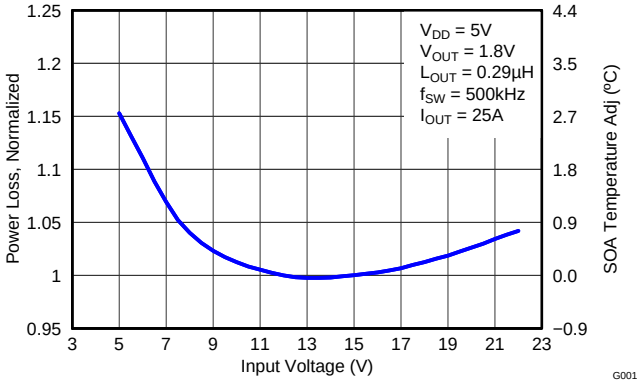


Figure 8. Normalized Power Loss vs Input Voltage

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TYPICAL CHARACTERISTICS (continued)

T_J = 125°C, unless stated otherwise.

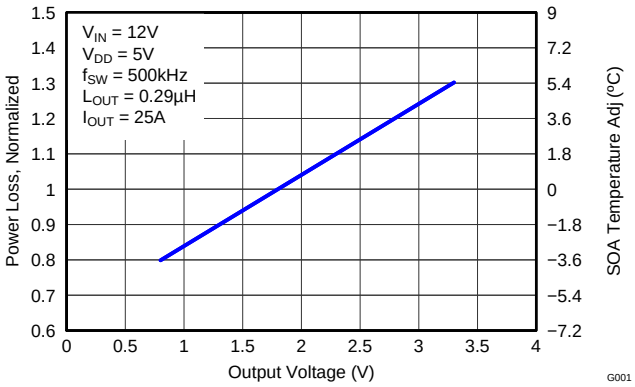


Figure 9. Normalized Power Loss vs Output Voltage

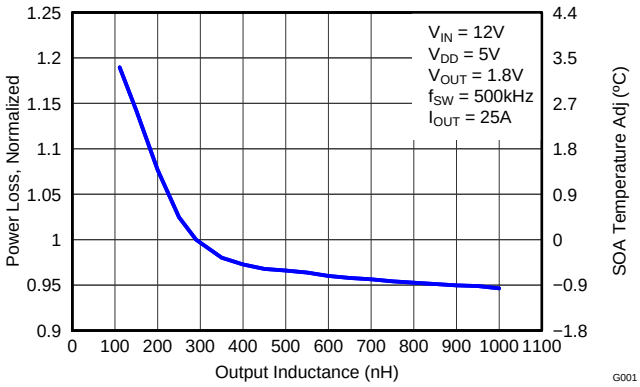


Figure 10. Normalized Power Loss vs Output Inductance

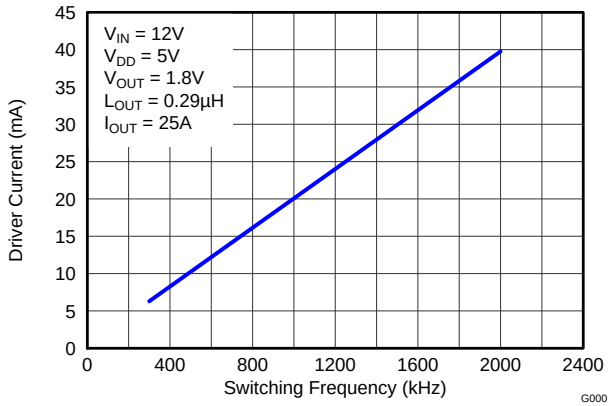


Figure 11. Driver Current vs Frequency

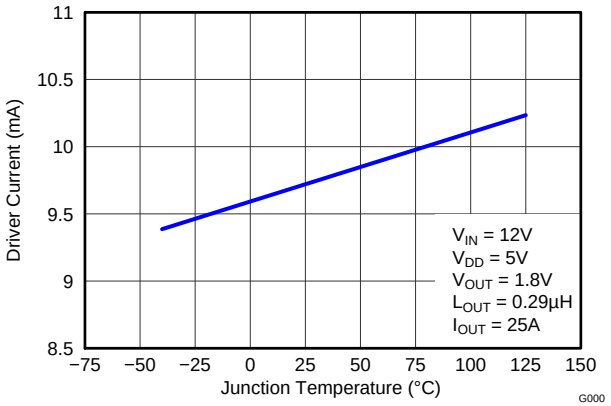


Figure 12. Driver Current vs Temperature

1. The Typical CSD97374Q4M System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness. See the Application Information section for detailed explanation.

PIN CONFIGURATION

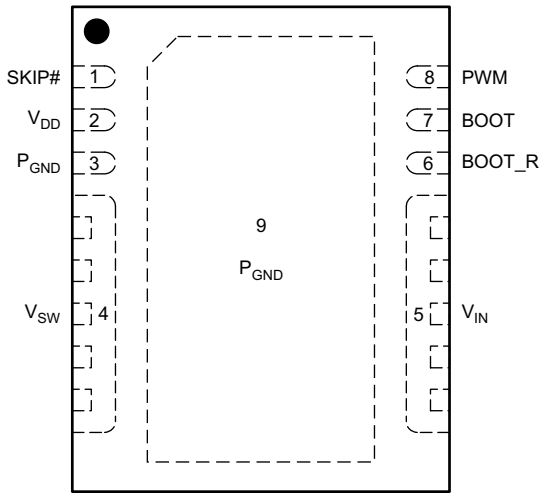


Figure 13. Top View

PIN DESCRIPTION

PIN		DESCRIPTION
NO.	NAME	
1	SKIP#	This pin enables the Diode Emulation function. When this pin is held Low, Diode Emulation Mode is enabled for the Sync FET. When SKIP# is High, the CSD97374Q4M operates in Forced Continuous Conduction Mode. A tri-state voltage on SKIP# puts the driver into a very low power state.
2	V_{DD}	Supply Voltage to Gate Drivers and internal circuitry.
3	P_{GND}	Power Ground, Needs to be connected to Pin 9 and PCB
4	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
5	V_{IN}	Input Voltage Pin. Connect input capacitors close to this pin.
6	BOOT_R	Bootstrap capacitor connection. Connect a minimum 0.1µF 16V X5R, ceramic cap from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the Control FET. The bootstrap diode is integrated.
7	BOOT	
8	PWM	Pulse Width modulated 3-state input from external controller. Logic Low sets Control FET gate low and Sync FET gate high. Logic High sets Control FET gate high and Sync FET gate Low. Open or High Z sets both MOSFET gates low if greater than the 3-State Shutdown Hold-off Time (t_{3HT})
9	P_{GND}	Power Ground

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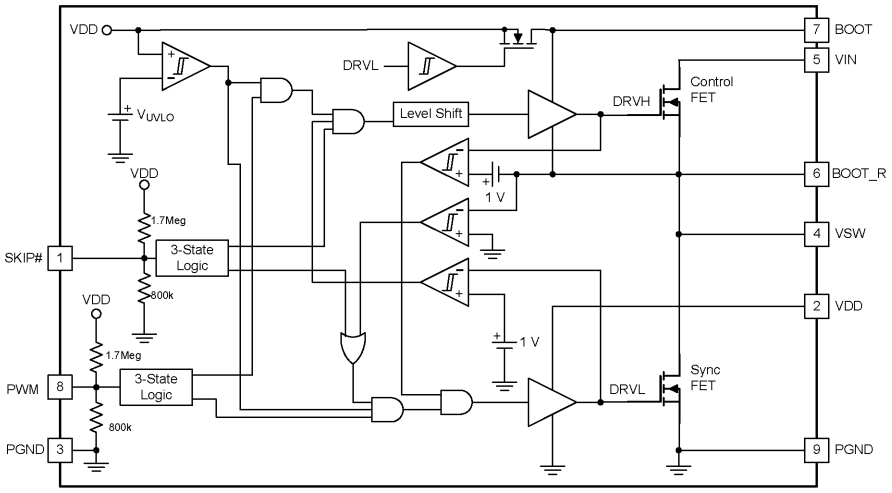


Figure 14. Functional Block Diagram

FUNCTIONAL DESCRIPTION

POWERING CSD97374Q4M AND GATE DRIVERS

An external V_{DD} voltage is required to supply the integrated gate driver IC and provide the necessary gate drive power for the MOSFETS. A 1µF 10V X5R or higher ceramic capacitor is recommended to bypass V_{DD} pin to P_{GND}. A bootstrap circuit to provide gate drive power for the Control FET is also included. The bootstrap supply to drive the Control FET is generated by connecting a 100nF 16V X5R ceramic capacitor between BOOT and BOOT_R pins. An optional R_{BOOT} resistor can be used to slow down the turn on speed of the Control FET and reduce voltage spikes on the V_{SW} node. A typical 1Ω to 4.7Ω value is a compromise between switching loss and V_{SW} spike amplitude.

Undervoltage Lockout Protection (UVLO)

The undervoltage lockout (UVLO) comparator evaluates the VDD voltage level. As V_{VDD} rises, both the Control FET and Sync FET gates hold actively low at all times until V_{VDD} reaches the higher UVLO threshold (V_{UVLO_H})., Then the driver becomes operational and responds to PWM and SKIP# commands. If VDD falls below the lower UVLO threshold (V_{UVLO_L} = V_{UVLO_H} – Hysteresis), the device disables the driver and drives the outputs of the Control FET and Sync FET gates actively low. Figure 15 shows this function.

CAUTION

Do not start the driver in the very low power mode (SKIP# = Tri-state).

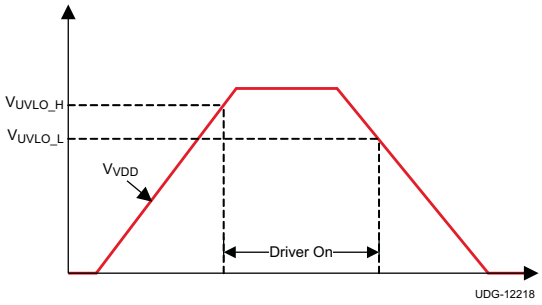


Figure 15. UVLO Operation

PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low power state with zero exit latency. The pin incorporates a weak pull-up to maintain the voltage within the tri-state window during low-power modes. Operation into and out of tri-state mode follows the timing diagram outlined in Figure 16.

When VDD reaches the UVLO_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined the PWM voltage range between PWM logic high (V_{IH}) and logic low (V_{IL}) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3 V (typical) and 5 V (typical) PWM drive signals.

When the PWM exits tri-state, the driver enters CCM for a period of 4 µs, regardless of the state of the SKIP# pin. Normal operation requires this time period in order for the auto-zero comparator to resume.

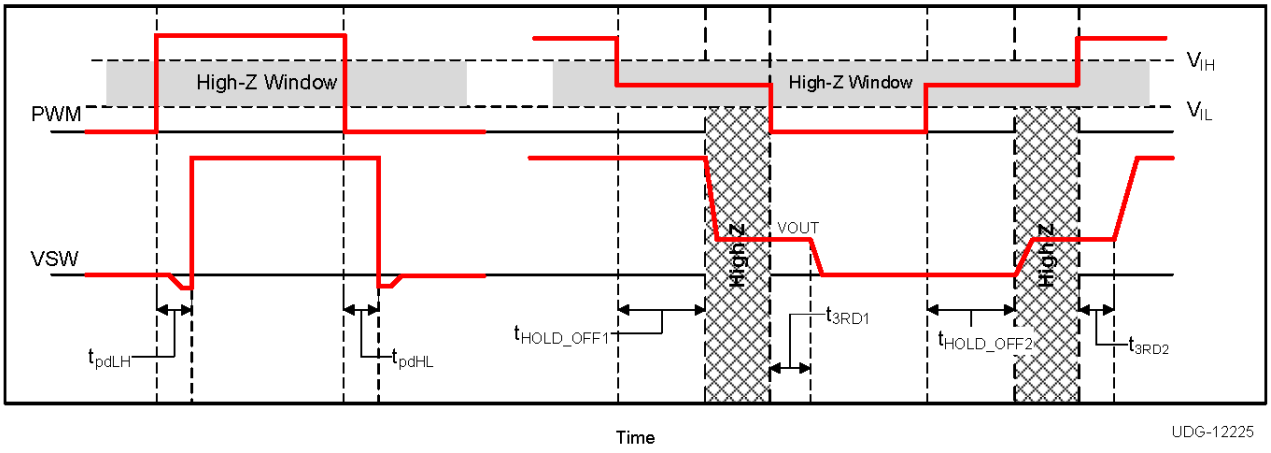


Figure 16. PWM Tri-State Timing Diagram

SKIP# Pin

The SKIP# pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When SKIP# is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When SKIP# is high, the ZX comparator disables, and the converter enters FCCM mode. When both SKIP# and PWM are tri-stated, normal operation forces the gate driver outputs low and the driver enters a low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When SKIP# is pulled low, the driver wakes up and is able to accept PWM pulses in less than 50 µs.

Table 1 shows the logic functions of UVLO, PWM, SKIP#, the Control FET Gate and the Sync FET Gate.

Table 1. Logic Functions of the Driver IC

UVLO	PWM	SKIP#	Sync FET Gate	Control FET Gate	MODE
Active	—	—	Low	Low	Disabled
Inactive	Low	Low	High(1)	Low	DCM(1)
Inactive	Low	High	High	Low	FCCM
Inactive	High	H or L	Low	High	
Inactive	Tri-state	H or L	Low	Low	LQ
Inactive	—	Tri-state	Low	Low	ULQ

(1) Until zero crossing protection occurs.

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Zero Crossing (ZX) Operation

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a *valley*, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and the BST pin is replaced by a FET which is gated by the DRVL signal.

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APPLICATION INFORMATION

The Power Stage CSD97374Q4M is a highly optimized design for synchronous buck applications using NexFET devices with a 5V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems centric environment. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the power MOSFETs. System level performance curves such as Power Loss, Safe Operating Area and normalized graphs allow engineers to predict the product performance in the actual application.

Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are primarily needed by engineers to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 3 plots the power loss of the CSD97374Q4M as a function of load current. This curve is measured by configuring and running the CSD97374Q4M as it would be in the final application (see Figure 17). The measured power loss is the CSD97374Q4M device power loss which consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\textbf{Power Loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 3 is measured at the maximum recommended junction temperature of T_J = 125°C under isothermal test conditions.

Safe Operating Curves (SOA)

The SOA curves in the CSD97374Q4M datasheet give engineers guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 5 and Figure 6 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness.

Normalized Curves

The normalized curves in the CSD97374Q4M data sheet give engineers guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

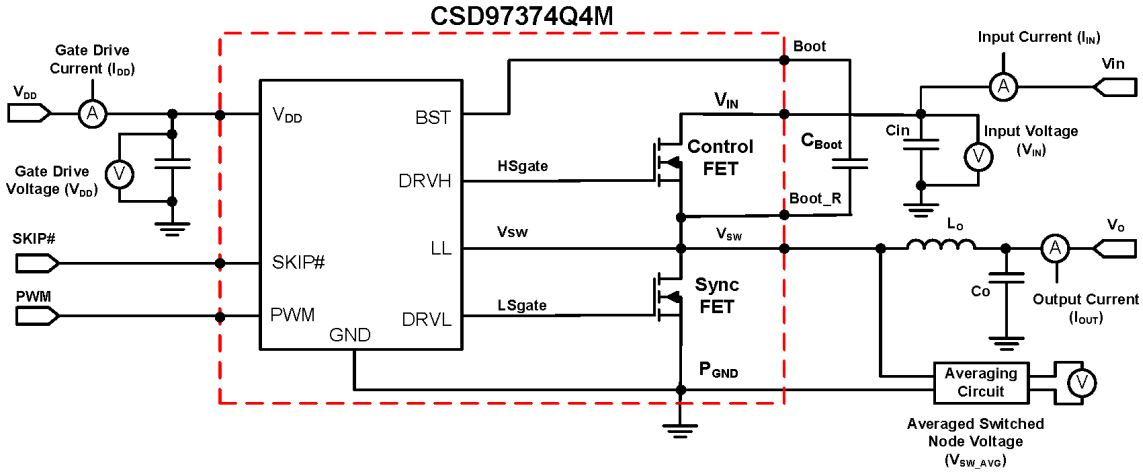


Figure 17. Power Loss Test Circuit

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Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see the Design Example). Though the Power Loss and SOA curves in this datasheet are taken for a specific set of test conditions, the following procedure will outline the steps engineers should take to predict product performance for any set of system conditions.

Design Example

Operating Conditions: Output Current (I_{OUT}) = 15A, Input Voltage (V_{IN}) = 7V, Output Voltage (V_{OUT}) = 1.5V, Switching Frequency (f_{SW}) = 800kHz, Output Inductor (L_{OUT}) = 0.2µH

Calculating Power Loss

- Typical Power Loss at 15A = 2.8W (Figure 3)
- Normalized Power Loss for switching frequency ≈ 1.02 (Figure 7)
- Normalized Power Loss for input voltage ≈ 1.07 (Figure 8)
- Normalized Power Loss for output voltage ≈ 0.94(Figure 9)
- Normalized Power Loss for output inductor ≈ 1.08 (Figure 10)
- **Final calculated Power Loss = 2.8W × 1.02 × 1.07 × 0.94 × 1.08 ≈ 3.1W**

Calculating SOA Adjustments

- SOA adjustment for switching frequency ≈ 0.3°C (Figure 7)
- SOA adjustment for input voltage ≈ 1.2°C (Figure 8)
- SOA adjustment for output voltage ≈ –1.1°C (Figure 9)
- SOA adjustment for output inductor ≈ 1.4°C (Figure 10)
- **Final calculated SOA adjustment = 0.3 + 1.2 + (–1.1) + 1.4 ≈ 1.8°C**

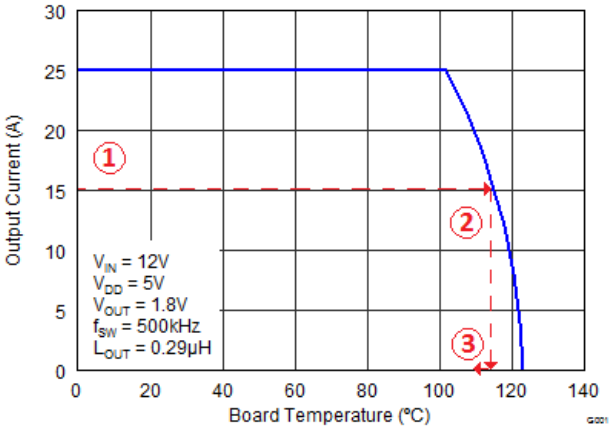


Figure 18. Power Stage CSD97374Q4M SOA

In the design example above, the estimated power loss of the CSD97374Q4M would increase to 3.1W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 1.8°C. Figure 18 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 1.8°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

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RECOMMENDED PCB DESIGN OVERVIEW

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. Below is a brief description on how to address each parameter.

Electrical Performance

The CSD97374Q4M has the ability to switch at voltage rates greater than 10kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, inductor and output capacitors.

- The placement of the input capacitors relative to V_{IN} and P_{GND} pins of CSD97374Q4M device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the V_{IN} and P_{GND} pins (see Figure 19). The example in Figure 19 uses 1 x 1nF 0402 25V and 3 x 10µF 1206 25V ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C5, C8 and C6, C19 should follow in order.
- The bootstrap cap C_{BOOT} 0.1µF 0603 16V ceramic capacitor should be closely connected between BOOT and BOOT_R pins
- The switching node of the output inductor should be placed relatively close to the Power Stage CSD97374Q4M V_{SW} pins. Minimizing the V_{SW} node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. (2)

Thermal Performance

The CSD97374Q4M has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 19 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

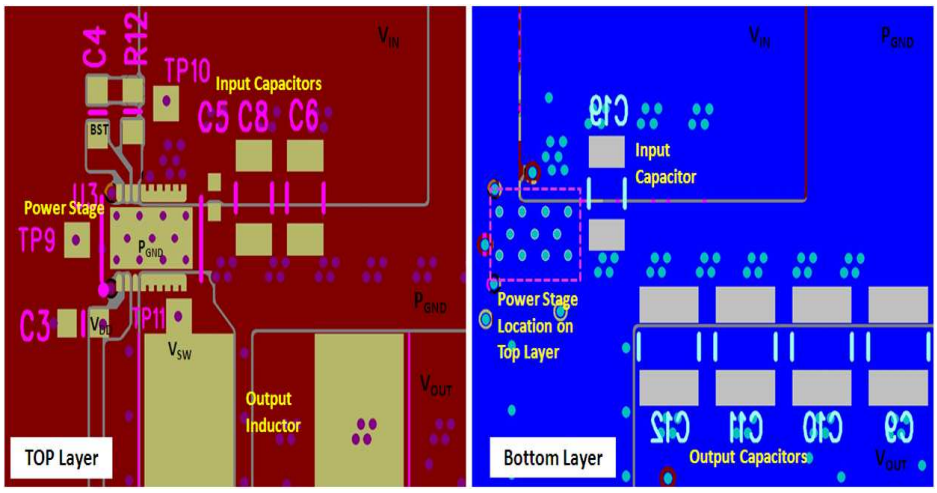
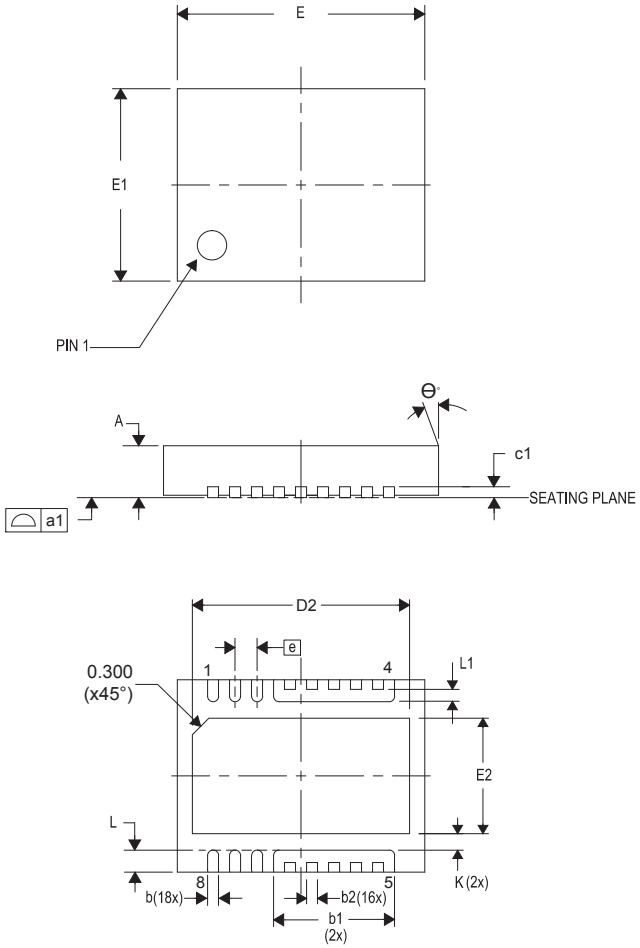


Figure 19. Recommended PCB Layout (Top Down View)

(2) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

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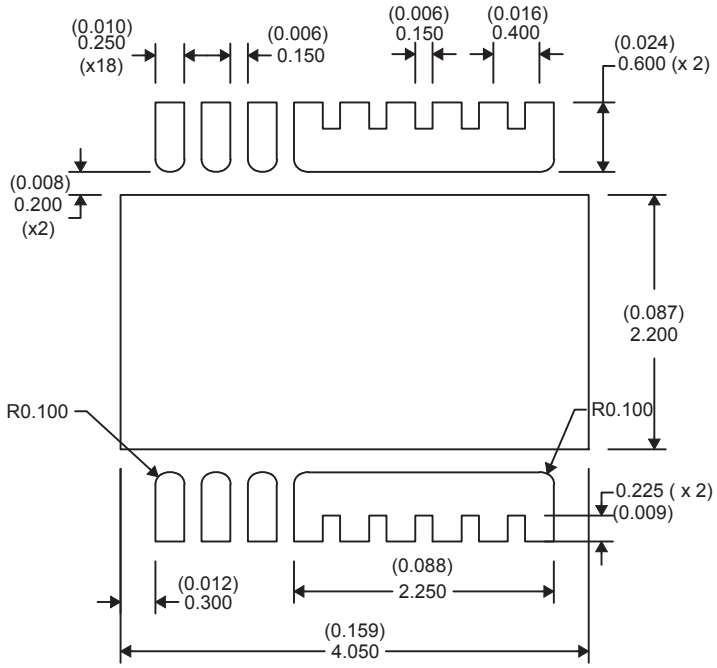
MECHANICAL DATA



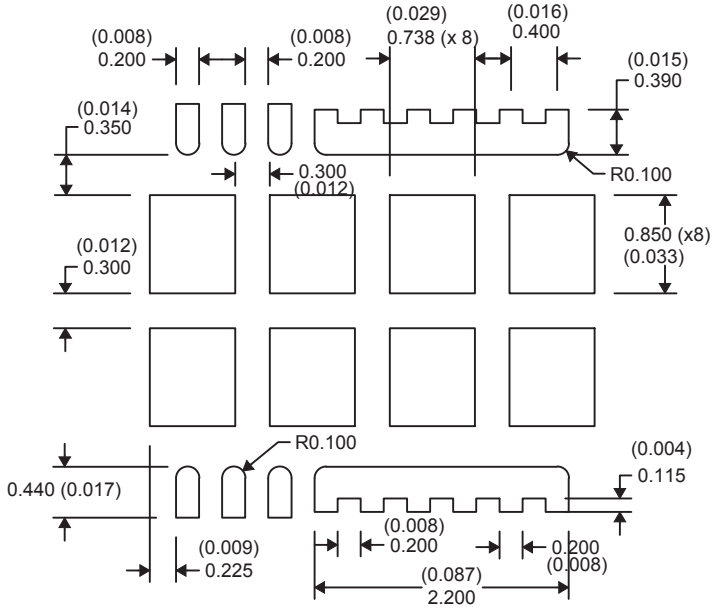
DIM	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.800	0.900	1.000	0.031	0.035	0.039
a1	0.000	0.000	0.080	0.000	0.000	0.003
b	0.150	0.200	0.250	0.006	0.008	0.010
b1	2.000	2.200	2.400	0.079	0.087	0.095
b2	0.150	0.200	0.250	0.006	0.008	0.010
c1	0.150	0.200	0.250	0.006	0.008	0.010
D2	3.850	3.950	4.050	0.152	0.156	0.160
E	4.400	4.500	4.600	0.173	0.177	0.181
E1	3.400	3.500	3.600	0.134	0.138	0.142
E2	2.000	2.100	2.200	0.079	0.083	0.087
e	0.400 TYP			0.016 TYP		
K	0.300 TYP			0.012 TYP		
L	0.300	0.400	0.500	0.012	0.016	0.020
L1	0.180	0.230	0.280	0.007	0.009	0.011
θ	0.00	—	—	0.00	—	—

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Recommended PCB Land Pattern



Recommended Stencil Opening



NOTE: Dimensions are in mm (inches).

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REVISION HISTORY

Changes from Original (January 2013) to Revision A **Page**

- Changed the ROC table, From: V_{SW} to P_{GND}, V_{IN} to V_{SW} (<20ns) MIN = -5 To: V_{SW} to P_{GND}, V_{IN} to V_{SW} (<10ns) MIN = -7 2
- Changed the ROC table, From: BOOT to P_{GND} (<20ns) MIN = -3 To: BOOT to P_{GND} (<10ns) MIN = -2 2
- Changed Logic Level High, V_{IH} From: MAX = 2.6 To: MIN = 2.65 3
- Changed Logic Level Low, V_{IL} From: MIN = 0.6 To: MAX = 0.6 3
- Changed Tri-State Voltage, V_{TS} From: MIN = 1.2 To: MIN = 1.3 3

Changes from Revision A (March 2013) to Revision B **Page**

- Changed the Mechanical Drawing image 13
- Changed the Recommended PCB Land Pattern image 14
- Changed the Recommended Stencil Opening image 14

Changes from Revision B (May 2013) to Revision C **Page**

- Added dimension row b2 to the MECHANICAL DATA table 13

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD97374Q4M	NRND	VSON-CLIP	DPC	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	97374M	
FX021	NRND	VSON-CLIP	DPC	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	97374M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

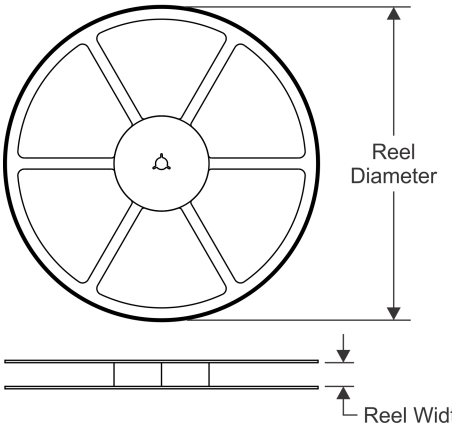
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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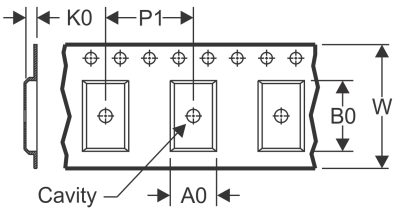
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

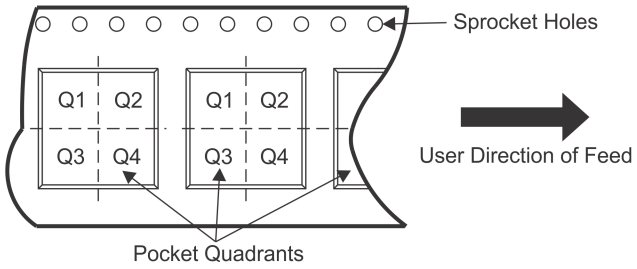


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

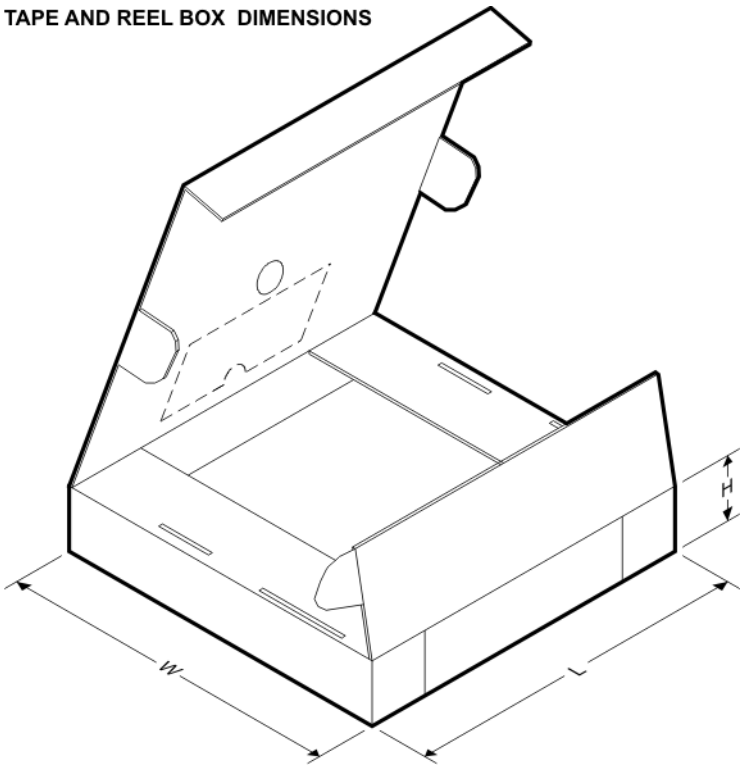
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD97374Q4M	VSON-CLIP	DPC	8	2500	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD97374Q4M	VSON-CLIP	DPC	8	2500	367.0	367.0	35.0

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