Single Synchronous Buck Controller

General Description

The RT8209A/B/C PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers.

The constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT8209A/B/C achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs. The buck conversion allows this device to directly step down high voltage batteries for the highest possible efficiency. The RT8209A/B/C is intended for CPU core, chipset, DRAM, or other low voltage supplies as low as 0.75V. The RT8209A is in a WQFN-16L 3x3 package, the RT8209B is in a WQFN-14L 3.5x3.5 package and the RT8209C is available in a TSSOP-14 package.

Ordering Information

RT8209 □□□

- Package Type
  - QW : WQFN-16L 3x3 (W-Type)
  - QW : WQFN-14L 3.5x3.5 (W-Type)
  - C : TSSOP-14
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
  - Z : ECO (Ecological Element with Halogen Free and Pb free)
- A : WQFN-16L 3x3
- B : WQFN-14L 3.5x3.5
- C : TSSOP-14

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

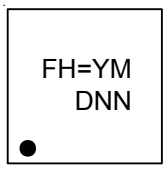
- **Ultra-High Efficiency**
- **Resistor Programmable Current Limit by Low Side $R_{DS(ON)}$ Sense (Lossless Limit)**
- **Quick Load Step Response within 100ns**
- **1% V_{FB} Accuracy over Line and Load**
- **4.5V to 26V Battery Input Range**
- **Resistor Programmable Frequency**
- **Integrated Bootstrap Switch**
- **Integrated Negative Current Limiter**
- **Over/Under Voltage Protection**
- **4 Steps Current Limit During Soft-Start**
- **Power Good Indicator**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook Computers
- System Power Supplies
- I/O Supplies

Marking Information

RT8209AGQW



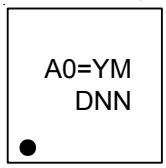
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YMDNN : Date Code

RT8209AZQW



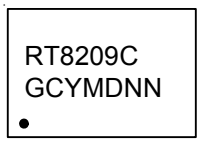
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RT8209BGQW



A0= : Product Code
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RT8209CGC

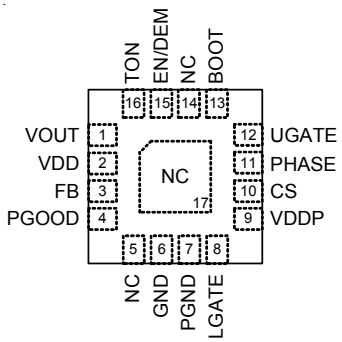


RT8209CGC : Product Code
YMDNN : Date Code

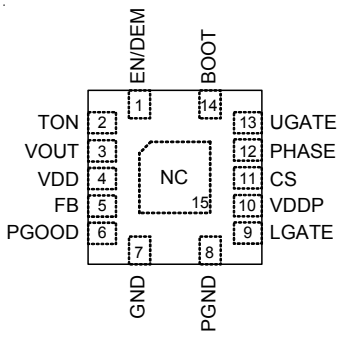
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Pin Configurations

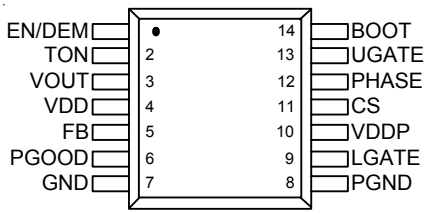
(TOP VIEW)



RT8209A (WQFN-16L 3x3)

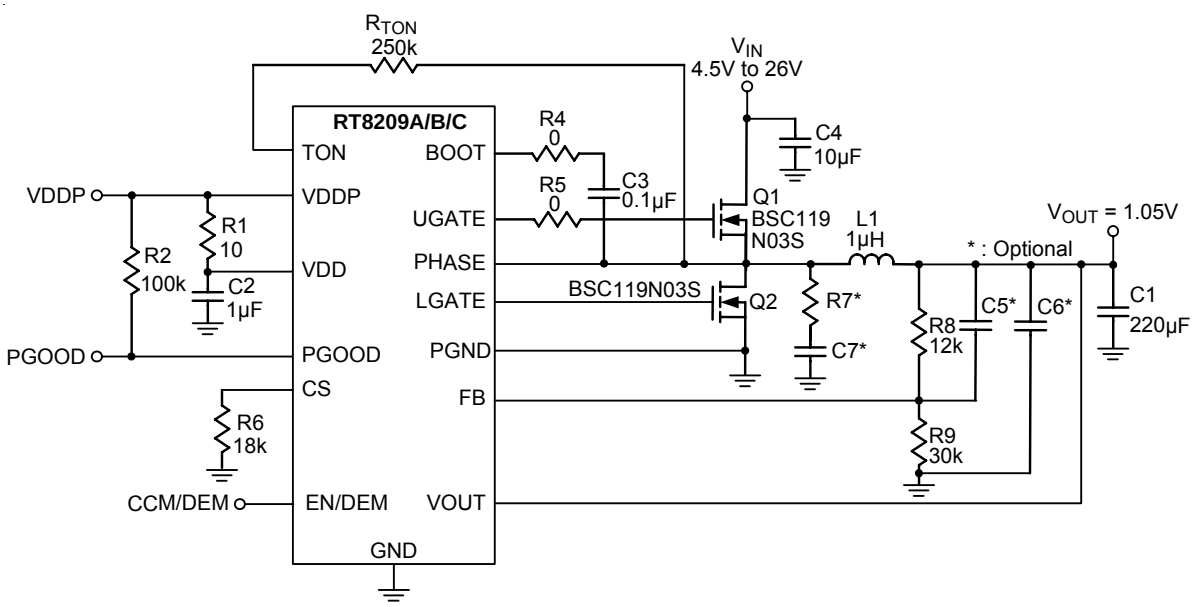


RT8209B (WQFN-14L 3.5x3.5)



RT8209C (TSSOP-14)

Typical Application Circuit



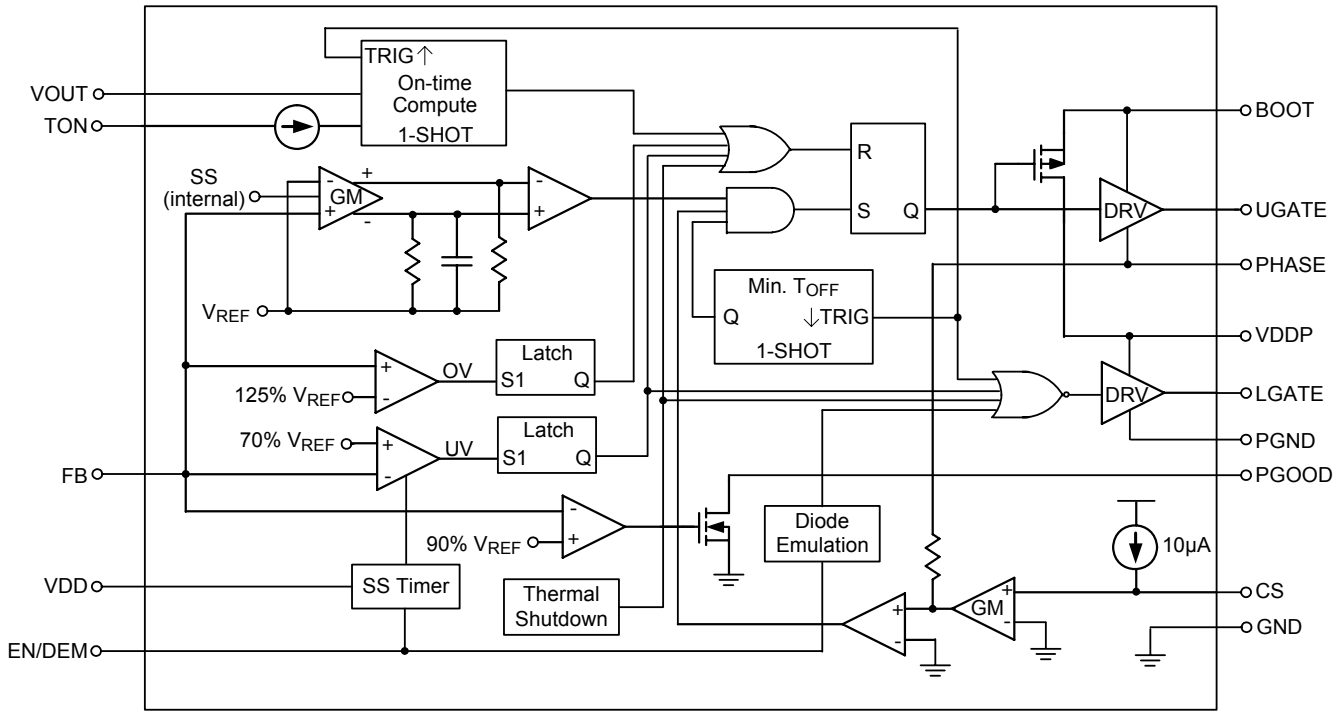
Functional Pin Description

Pin No.		Pin Name	Pin Function
RT8209A	RT8209B/C		
1	3	VOUT	Output Voltage Pin. Connect to the output of PWM converter. VOUT is an input of the PWM controller.
2	4	VDD	Analog supply voltage input for the internal analog integrated circuit. Bypass to GND with a 1µF ceramic capacitor.
3	5	FB	Feedback Input Pin. Connect FB to a resistor voltage divider from VOUT to GND to adjust VOUT from 0.75V to 3.3V
4	6	PGOOD	Power good signal open-drain output of PWM converter. This pin will be pulled high when the output voltage is within the target range.
5, 14 17 (Exposed pad)	RT8209B : 15 (Exposed pad)	NC	No internal connection. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

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Pin No.		Pin Name	Pin Function
RT8209A	RT8209B/C		
6	7	GND	Analog Ground.
7	8	PGND	Power Ground.
8	9	LGATE	Low side N-MOSFET gate driver output for PWM. This pin swings between GND and VDDP.
9	10	VDDP	VDDP is the gate driver supply for external MOSFETs. Bypass to GND with a 1μF ceramic capacitor.
10	11	CS	Over Current Trip Point Set Input. Connect resistor from this pin to signal ground to set threshold for both over current and negative over current limit.
11	12	PHASE	The UGATE High Side Gate Driver Return. Also serves as anode of over current comparator.
12	13	UGATE	High side N-MOSFET floating gate driver output for the PWM converter. This pin swings between PHASE and BOOT.
13	14	BOOT	Bootstrap Capacitor Connection for PWM Converter. Connect to an external ceramic capacitor to PHASE.
15	1	EN/DEM	Enable/Diode Emulation Mode Control Input. Connect to VDD for diode-emulation mode, connect to GND for shutdown and floating the pin for CCM mode.
16	2	TON	On Time/Frequency Adjustment Pin. Connect to PHASE through a resistor. TON is an input for the PWM controller.

Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- VDD, VDDP, VOUT, EN/DEM, FB, PGOOD, TON to GND ---------- –0.3V to 6V
- BOOT to GND ---------- –0.3V to 38V
- BOOT to PHASE ---------- –0.3V to 6V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - < 20ns ---------- –8V to 38V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –5V to 7.5V
- CS to GND ---------- –0.3V to 6V
- LGATE to GND ---------- –0.3V to 6V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –2.5V to 7.5V
- PGND to GND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–16L 3x3 ---------- 1.471W
  - WQFN–14L 3.5x3.5 ---------- 1.667W
  - TSSOP-14 ---------- 0.741W
- Package Thermal Resistance (Note 2)
  - WQFN–16L 3x3, θ_{JA} ---------- 68°C/W
  - WQFN–16L 3x3, θ_{JC} ---------- 7.5°C/W
  - WQFN–14L 3.5x3.5, θ_{JA} ---------- 60°C/W
  - WQFN–14L 3.5x3.5, θ_{JC} ---------- 7.5°C/W
  - TSSOP-14, θ_{JA} ---------- 135°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 4.5V to 26V
- Supply Voltage, V_{DD}, V_{DDP} ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

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Electrical Characteristics

(V_{IN} = 15V, V_{DD} = V_{DDP} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
Quiescent Supply Current	I_{VDD}	V_{FB} = 0.8V, EN/DEM = 5V	--	500	800	μA
	I_{VDDP}	V_{FB} = 0.8V, EN/DEM = 5V	--	1	10	
Shutdown Current	I_{SHDN_VDD}	EN/DEM = 0V	--	1	10	μA
	I_{SHDN_VDDP}	EN/DEM = 0V	--	--	1	
FB Reference Voltage	V_{REF}	V_{DD} = 4.5V to 5.5V	0.742	0.750	0.758	V
FB Input Bias Current		V_{FB} = 0.75V	–1	0.1	1	μA
Output Voltage Range	V_{OUT}		0.75	--	3.3	V
On Time		V_{PHASE} = 12V, V_{OUT} = 2.5V, R_{TON} = 250kΩ	336	420	504	ns
Minimum Off-Time			250	400	550	ns
VOUT Shutdown Discharge Resistance		EN/DEM = GND	--	20	--	Ω
Current Sensing						
Current Limiter Source Current		CS to GND	9	10	11	μA
Current Comparator Offset			–10	--	10	mV
Zero Crossing Threshold		PHASE to GND, EN/DEM = 5V	–10	--	5	mV
Fault Protection						
Current Limit Threshold		GND – PHASE, V_{CS} = 50mV	40	50	60	mV
		GND – PHASE, V_{CS} = 200mV	190	200	210	
Current Limit Setting Range		CS to GND	50	--	200	mV
Output UV Threshold		UVP detect	60	70	80	%
OVP Threshold	V_{FB_OVP}	OVP detect	120	125	130	%
OV Fault Delay		FB forced above OV threshold	--	20	--	μs
VDD Under Voltage Lockout Threshold		Rising edge, PWM disabled below this level	4.1	4.3	4.5	V
		Hysteresis	--	80	--	mV
Current Limit Step Duration at Soft-Start		Each step	--	128	--	clks
UVP Blanking Time		From EN signal going high	--	512	--	clks
Thermal Shutdown	T_{SHDN}	Hysteresis = 10°C	--	155	--	°C
Driver On-Resistance						
UGATE Drive Source	$R_{UGATEsr}$	V_{BOOT} – V_{PHASE} = 5V	--	2	5	Ω
UGATE Drive Sink	$R_{UGATEsk}$	V_{BOOT} – V_{PHASE} = 5V	--	1	5	Ω
LGATE Drive Source	$R_{LGATEsr}$	LGATE, High State	--	1	5	Ω
LGATE Drive Sink	$R_{LGATEsk}$	LGATE, Low State	--	0.5	2.5	Ω
UGATE Driver Source/Sink Current		V_{UGATE} – V_{PHASE} = 2.5V, V_{BOOT} – V_{PHASE} = 5V	--	1	--	A
LGATE Driver Source Current		V_{LGATE} = 2.5V	--	1	--	A
LGATE Driver Sink Current		V_{LGATE} = 2.5V	--	3	--	A
Dead Time		LGATE Rising (V_{PHASE} = 1.5V)	--	30	--	ns
		UGATE Rising	--	30	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal BOOT Charging Switch On Resistance		VDDP to BOOT, 10mA	--	--	80	Ω
Logic I/O						
EN/DEM Logic Input Voltage		EN/DEM Low	--	--	0.8	V
		EN/DEM High	2.9	--	--	
		EN/DEM float	--	2	--	
Logic Input Current		EN/DEM = VDD	--	1	5	μA
		EN/DEM = 0	–5	1	--	
PGOOD						
PGOOD Threshold		V_{FB} with respect to reference, PGOOD from Low to High	87	90	93	%
		V_{FB} with respect to reference, PGOOD from High to Low	--	125	--	
		Hysteresis	--	3	--	
Fault Propagation Delay		Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage		I_{SINK} = 1mA	--	--	0.4	V
Leakage Current		High state, forced to 5V	--	--	1	μA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the package.

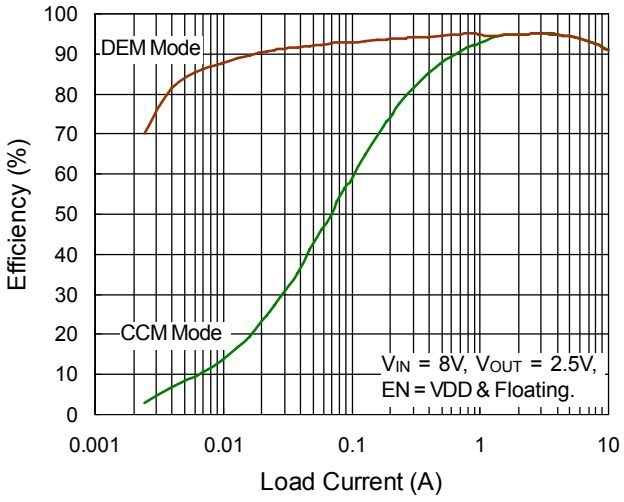
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

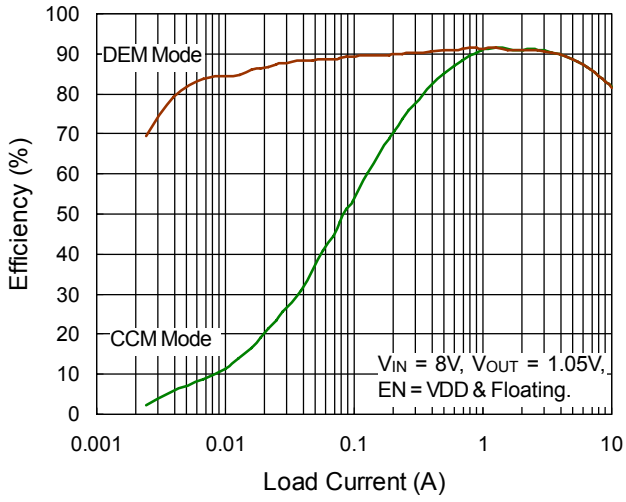
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Typical Operating Characteristics

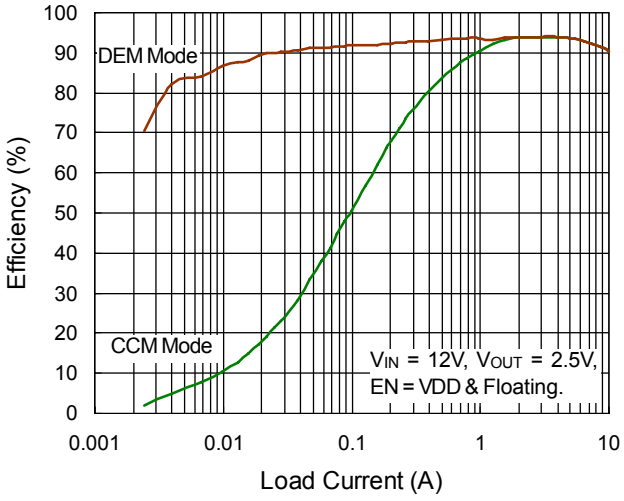
2.5V Efficiency vs. Load Current



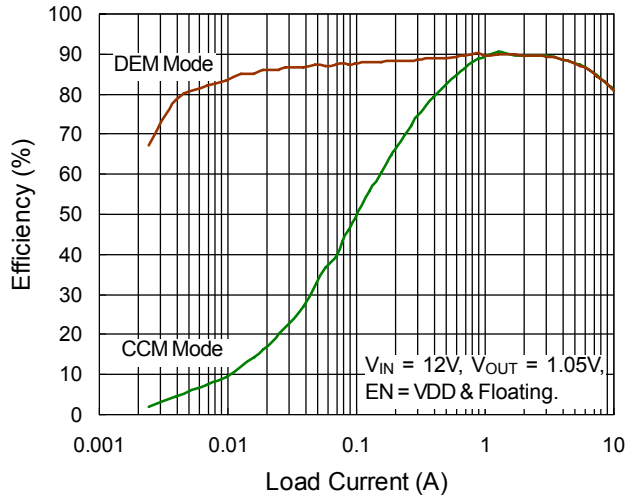
1.05V Efficiency vs. Load Current



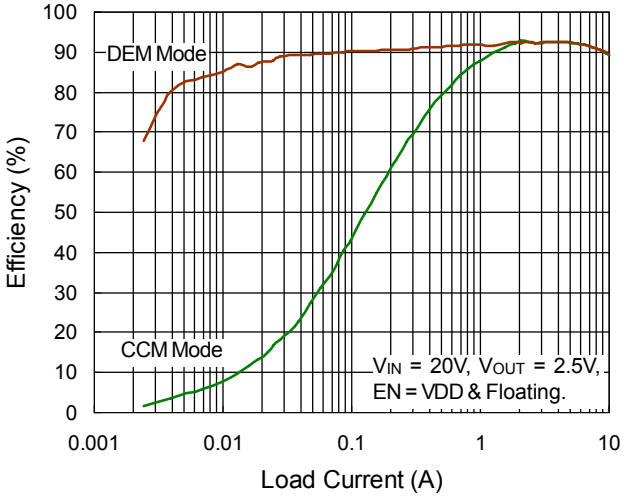
2.5V Efficiency vs. Load Current



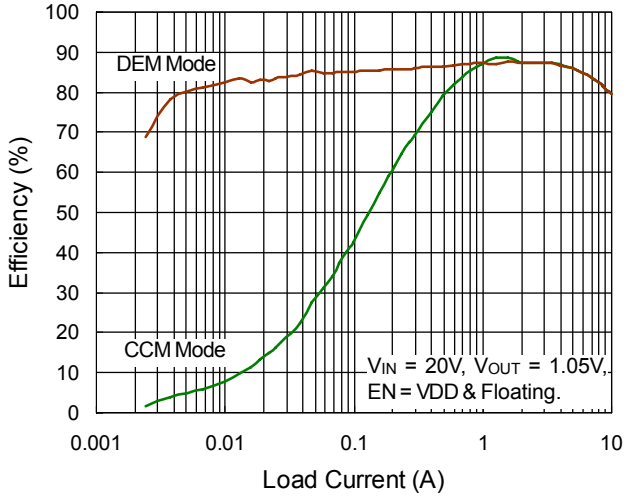
1.05V Efficiency vs. Load Current



2.5V Efficiency vs. Load Current

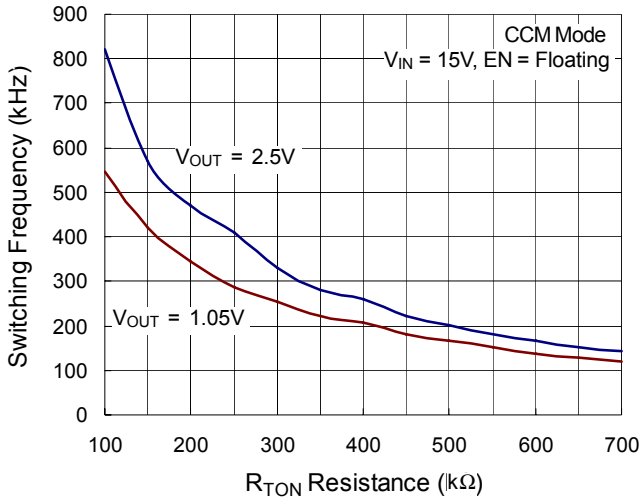


1.05V Efficiency vs. Load Current

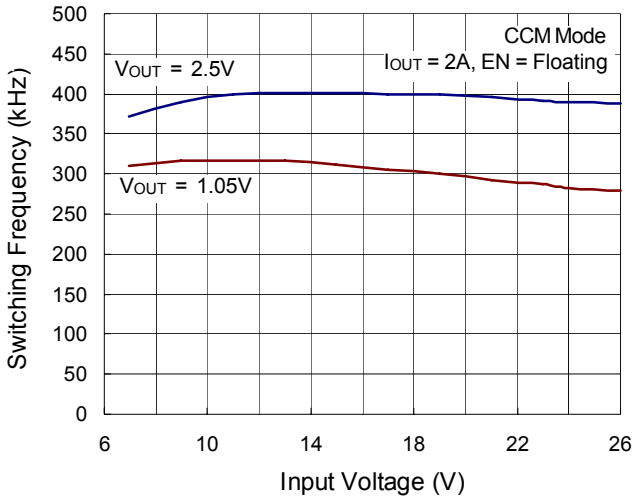


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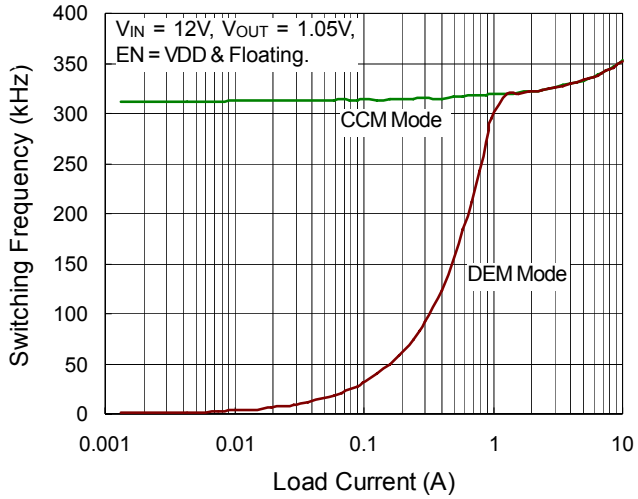
Switching Frequency vs. R_{TON} Resistance



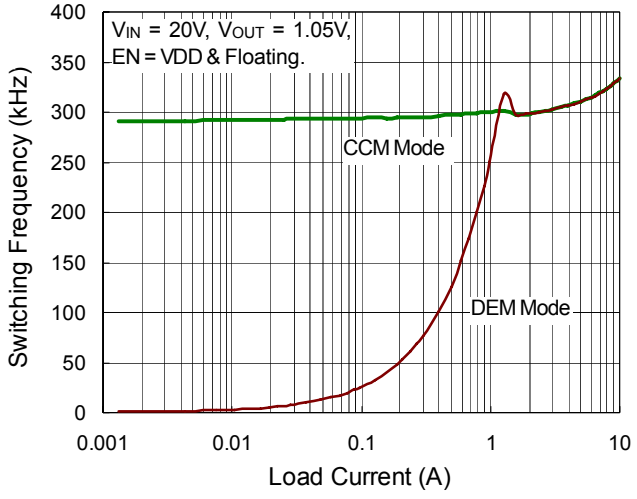
Switching Frequency vs. Input Voltage



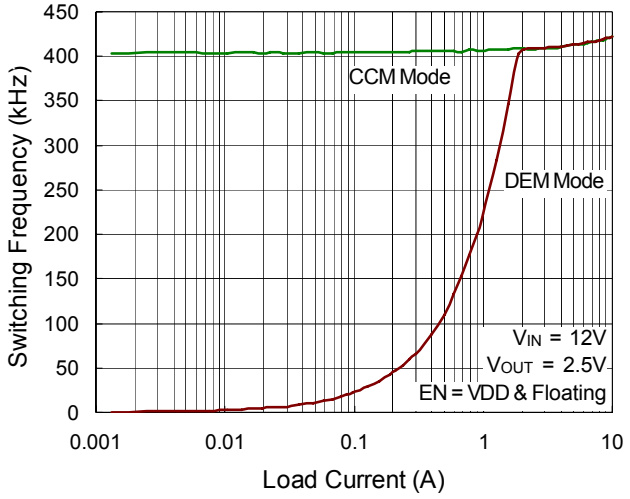
1.05V Switching Frequency vs. Load Current



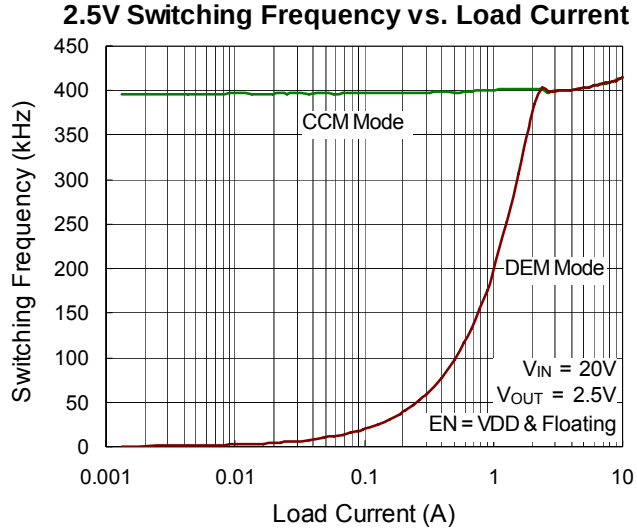
1.05V Switching Frequency vs. Load Current



2.5V Switching Frequency vs. Load Current

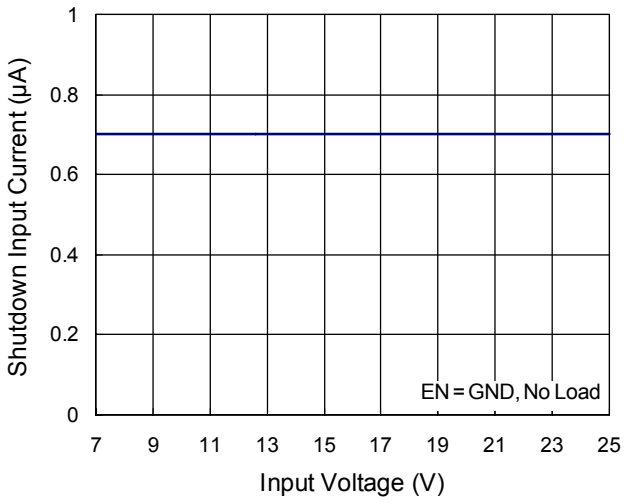


2.5V Switching Frequency vs. Load Current

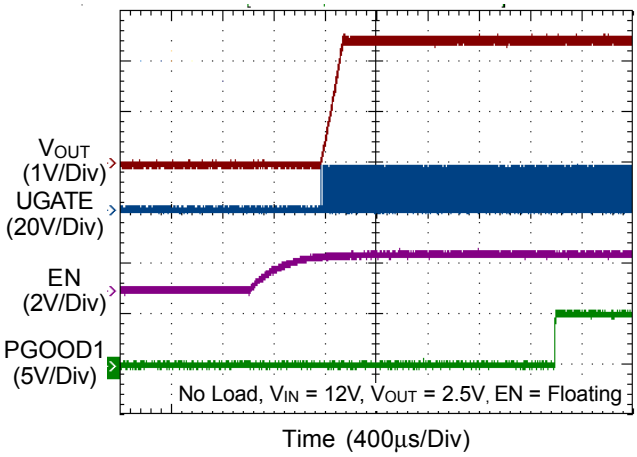


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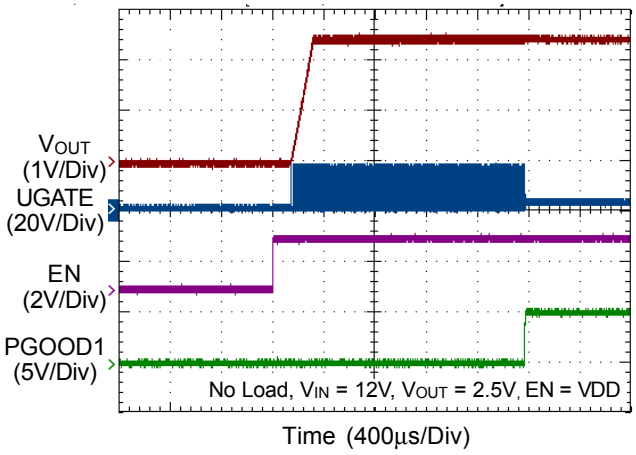
Shutdown Input Current vs. Input Voltage



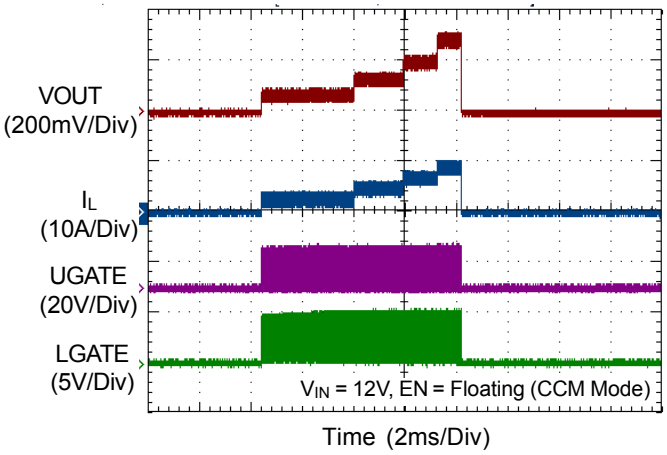
Power On from EN (CCM Mode)



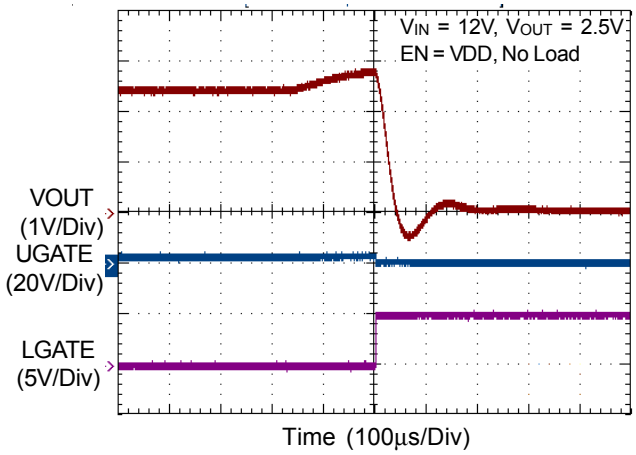
Power On from EN (DEM Mode)



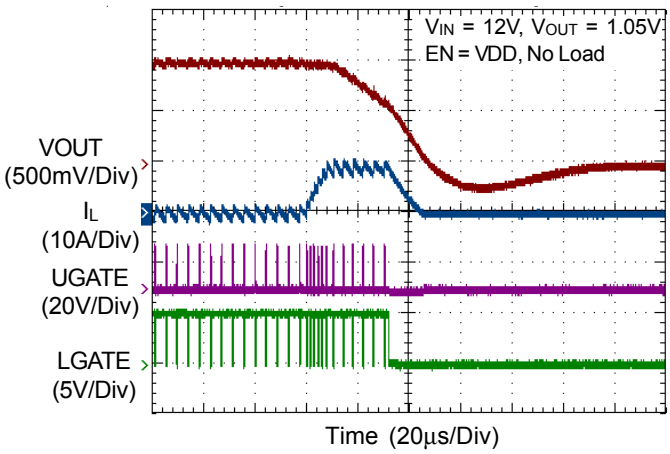
Power On in Short Circuit



OVP (DEM Mode)

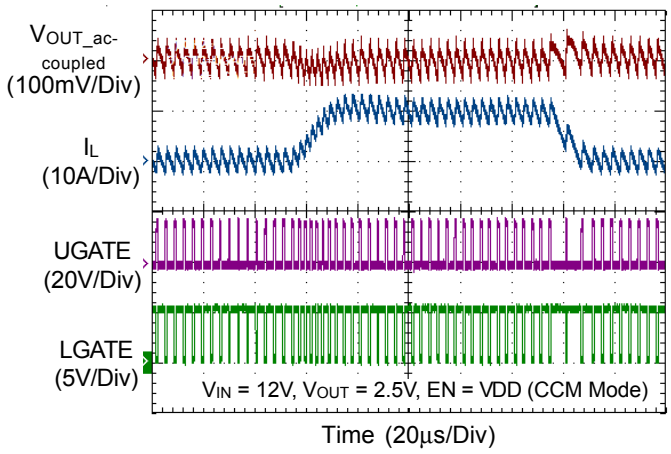


UVP (DEM Mode)

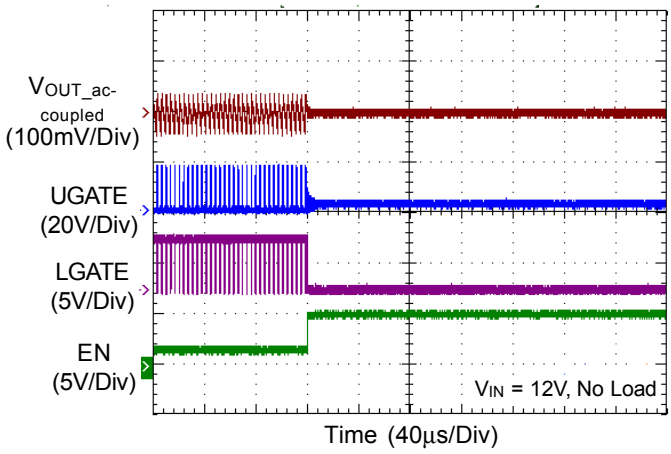


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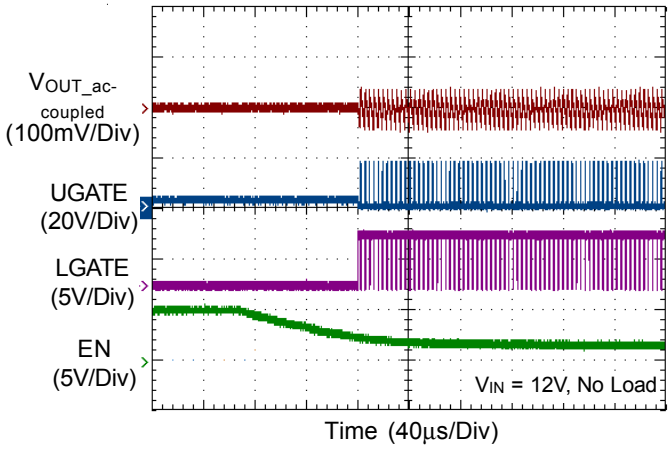
2.5V Load Transient Response



Mode Transition CCM to DEM



Mode Transition DEM to CCM



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Application Information

The RT8209A/B/C PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers. Richtek Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load transient timing problems of fixed-frequency current-mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current sense resistor, so the output ripple voltage provides the PWM ramp signal. Refer to the function block diagram, the synchronous UGATE driver will be turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver will be turned off. The pulse width of this one shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

On-Time Control

The on-time one-shot comparator has two inputs. One input monitors the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{OUT}, thereby making the on-time of the high side switch directly proportional to output voltage and inversely proportional to input voltage. The implementation results in a nearly constant switching frequency without the need a clock generator.

t_{ON} = 9.6p x R_{TON} x (V_{OUT} + 0.1) / (V_{IN} – 0.3) + 50ns

Although this equation provides a good approximation to start with, the accuracy depends on each design and selection of the high side MOSFET.

And then the switching frequency is:

$$f = \frac{V_{OUT}}{V_{IN} \times t_{ON}}$$

R_{TON} is the external resistor connected from the PHASE to TON pin.

Mode Selection (EN/DEM) Operation

The EN/DEM pin enables the supply. When EN/DEM is tied to VDD, the controller is enabled and operates in diode-emulation mode. When the EN/DEM pin is floating, the RT8209A/B/C will operate in forced-CCM mode.

Diode-Emulation Mode (EN/DEM = High)

In diode-emulation mode, the RT8209A/B/C automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increasing VOUT ripple or load regulation. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial of negative current when the inductor freewheeling current reach negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level than requires the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light-load operation can be calculated as follows (Figure 1) :

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is On-time.

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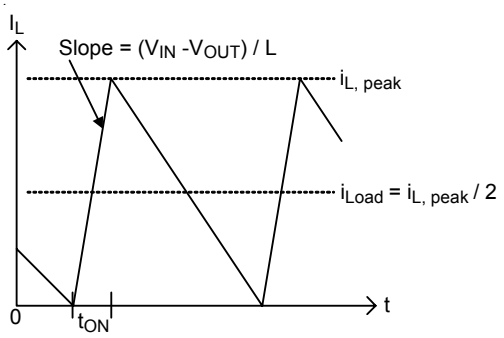


Figure 1. Boundary Condition of CCM/DEM

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degrade load transient response (especially at low input-voltage levels).

Forced-CCM Mode (EN/DEM = Floating)

The low noise, forced-CCM mode (EN/DEM = floating) disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low side gate drive waveform to become the complement of the high side gate-drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio VOUT/VIN. The benefit of forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost. The no-load battery current can be up to 10mA to 40mA, depending on the external MOSFETs.

Current Limit Setting (OCP)

RT8209A/B/C has cycle-by-cycle current limiting control. The current limit circuit employs a unique “valley” current sensing algorithm. If PHASE voltage plus the current limit threshold is below zero, the PWM is not allowed to initiate a new cycle (Figure 2). In order to provide both good accuracy and a cost effective solution, the RT8209A/B/C supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The CS pin should be connected to GND through the trip voltage setting resistor, R_{CS}. The CS terminal source 10μA I_{CS} current, and the trip level is set to the CS trip voltage, V_{CS} can be calculated as following equation.

V_{CS} (mV) = R_{CS} (kΩ) x 10 (μA)

Inductor current is monitored by the voltage between the PGND pin and the PHASE pin, so the PHASE pin should be connected to the drain terminal of the low side MOSFET. I_{CS} has positive temperature coefficient to compensate the temperature dependency of the $R_{DS(ON)}$. PGND is used as the positive current sensing node so PGND should be connected to the source terminal of the bottom MOSFET.

As the comparison is done during the OFF state, V_{CS} sets the valley level of the inductor current. Thus, the load current at over current threshold, I_{LOAD_OC}, can be calculated as follows.

$$I_{LOAD_OC} = \frac{VCS}{RDS(ON)} + \frac{IRipple}{2}$$

$$= \frac{V_{CS}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

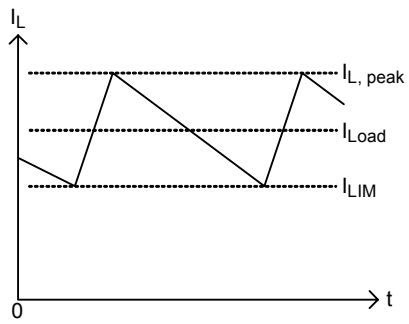


Figure 2. Valley Current Limit

MOSFET Gate Driver (UGATE, LGATE)

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from VDDP supply. The average drive current is proportional to the gate charge at VGS = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOT and PHASE pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on. The low side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s).

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The internal pull-down transistor that drives LGATE low is robust, with a 0.5Ω typical on resistance. A 5V bias voltage is delivered from VDDP supply. The instantaneous drive current is supplied by the flying capacitor between VDDP and PGND.

For high current applications, some combinations of high and low side MOSFETs might be encountered that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high side MOSFET without degrading the turn-off time (Figure 3).

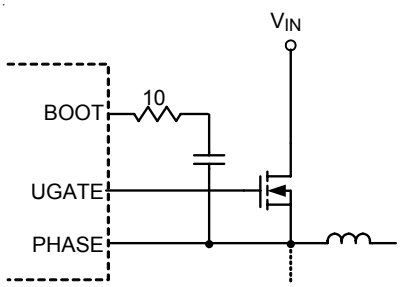


Figure 3. Reducing the UGATE Rise Time

Power Good Output (PGOOD)

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 25% above or 10% below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. In soft-start, PGOOD is actively held low and is allowed to transition high until soft-start is over and the output reaches 93% of its set voltage. There is a 2.5μs delay built into PGOOD circuitry to prevent false transitions.

POR, UVLO and Soft-Start

Power On Reset (POR) occurs when VDD rises above to approximately 4.3V, the RT8209A/B/C will reset the fault latch and preparing the PWM for operation. Below 4.1 $V_{(MIN)}$, the VDD under voltage-lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low. A built-in soft-start is used to prevent surge current from power supply input after EN/DEM is enabled. The maximum allowed current limit is segmented in 4 steps: 25%, 50%, 75% and 100% during this period, each step is 128 UGATE clks. The current limit steps can eliminate the V_{OUT} folded-back in the soft-start duration.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage protection. When the output voltage exceeds 25% of the set voltage threshold, over voltage protection is triggered and the low side MOSFET is latched on. This activates the low side MOSFET to discharge the output capacitor. The RT8209A/B/C is latched once OVP is triggered and can only be released by VDD or EN/DEM power on reset. There is a 20μs delay built into the over voltage protection circuit to prevent false transitions.

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When the output voltage is less than 70% of the set voltage threshold, under voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. There is a 2.5μs delay built into the under voltage protection circuit to prevent false transitions. During soft-start, the UVP blanking time is 512 UGATE clks.

Output Voltage Setting (FB)

The output voltage can be adjusted from 0.75V to 3.3V by setting the feedback resistor R1 and R2 (Figure 4). Choose R2 to be approximately 10kΩ, and solve for R1 using the equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is 0.75V.(typ.)

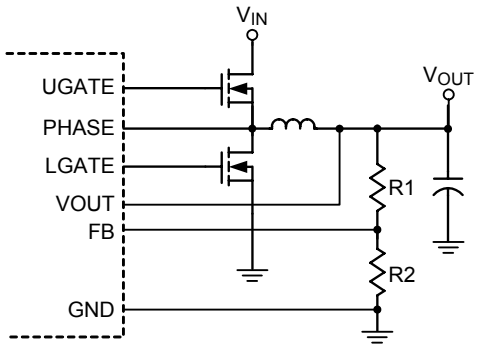


Figure 4. Setting VOUT with a Resistor Divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows :

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{L_{IR} \times I_{LOAD(MAX)}}$$

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Where L_{IR} is the ratio of peak-of-peak ripple current to the maximum average inductor current. Find a low pass inductor having the lowest possible DC resistance that fits in the allowed dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough and not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left[\left(\frac{L_{IR}}{2}\right) \times I_{LOAD(MAX)}\right]$$

Output Capacitor Selection

The output filter capacitor must have low enough Equivalent Series Resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must also be high enough to absorb the inductor energy while transiting from full-load to no-load conditions without tripping the overvoltage fault latch.

Although Mach Response™ DRV™ dual ramp valley mode provides many advantages such as ease-of-use, minimum external component configuration, and extremely short response time, due to not employing an error amplifier in the loop, a sufficient feedback signal needs to be provided by an external circuit to reduce the jitter level. The required signal level is approximately 15mV at the comparing point. This generates $V_{Ripple} = (V_{OUT} / 0.75) \times 15mV$ at the output node. The output capacitor ESR should meet this requirement.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic and unstable operation. However, it is easy to add sufficient series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting VOUT or FB divider close to the inductor. There are two related but distinct ways including double-pulsing and feedback loop instability to identify the unstable operation. Double-pulsing occurs due to noise on the output or because the ESR is too low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after a 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillation at the output after line or load perturbations that can trip the over voltage protection latch or cause the output voltage to fall below the tolerance limit. The easiest method for stability checking is to apply a very zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with AC probe. Do not allow more than one ringing cycle after the initial step-response under- or over-shoot.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8209A/B/C, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-16L 3x3 packages, the thermal resistance θ_{JA} is 68°C/W on the standard JEDEC 51-7 four layers thermal test board. For WQFN-14L 3.5x3.5 packages, the thermal resistance θ_{JA} is 60°C/W on the standard JEDEC 51-7 four layers thermal test board. For TSSOP-14 packages, the thermal resistance θ_{JA} is 135°C/W on the standard JEDEC 51-7

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four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (68°C/W) = 1.471W for

WQFN-16L 3x3 packages

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for

WQFN-14L 3.5x3.5 packages

$P_{D(MAX)}$ = (125°C – 25°C) / (135°C/W) = 0.741W for TSSOP-14 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8209A/B/C packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

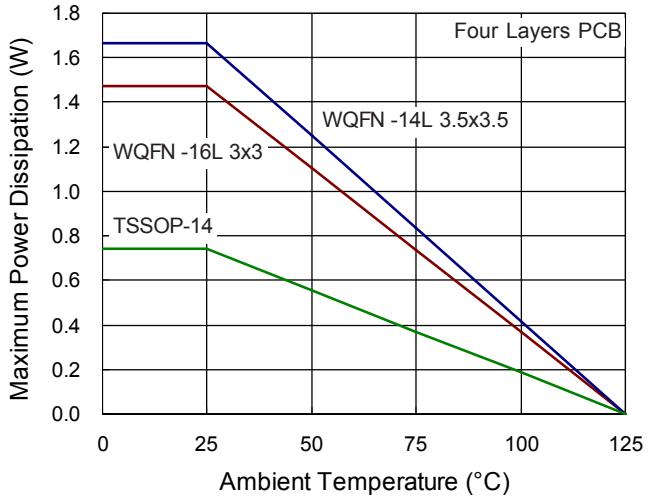


Figure 5. Derating Curves for RT8209A/B/C Packages

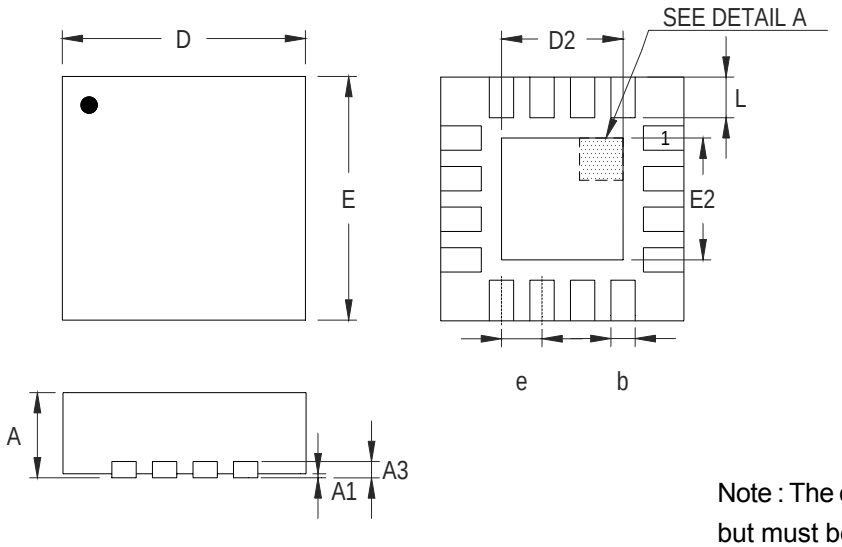
Layout Considerations

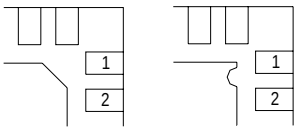
Layout is very important in high frequency switching converter design. If the layout is designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. The following points must be followed for a proper layout of RT8209A/B/C.

- Connect an RC low-pass filter from VDDP to VDD, 1μF and 10Ω are recommended. Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VOUT, FB, GND, EN/DEM, PGOOD, CS, VDD, and TON should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

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Outline Dimension





DETAIL A

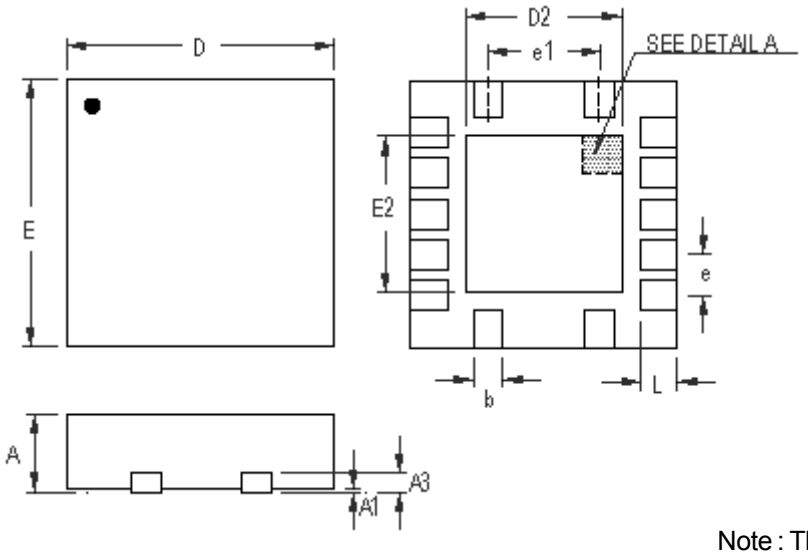
Pin #1 ID and Tie Bar Mark Options

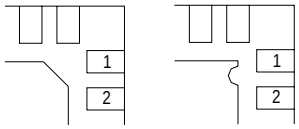
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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DETAIL A

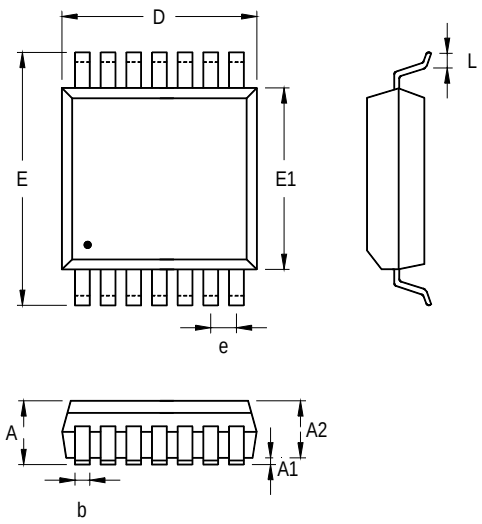
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.400	3.600	0.134	0.142
D2	1.950	2.150	0.077	0.085
E	3.400	3.600	0.134	0.142
E2	1.950	2.150	0.077	0.085
e	0.500		0.020	
e1	1.500		0.060	
L	0.300	0.500	0.012	0.020

W-Type 14L QFN 3.5x3.5 Package

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Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.200	0.039	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030

14-Lead TSSOP Plastic Package

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Tel: (8863)5526789

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