Ultra Low Noise 300mA Dual LDO Regulator with POR, NMOS Driver and Requiring No Bypass Capacitor

General Description

RT9014/A is a dual channel, low noise, and low dropout with the sourcing ability up to 300mA, an open drain driver and power-on reset function. The open-drain output is capable of sinking 150mA for LED backlighting applications.

The range of output voltage is from 1.2V to 3.6V by operating from 2.5V to 5.5V input.

RT9014/A offers 2% accuracy, extremely low dropout voltage (240mV @ 300mA), and extremely low ground current, only 27μA per LDO. The shutdown current is near zero current which is suitable for battery-power devices. Other features include current limiting, over temperature, output short circuit protection.

RT9014/A is short circuit thermal folded back protected. RT9014/A lowers its OTP trip point from 165°C to 110°C when output short circuit occurs (V_{OUT} < 0.4V) providing maximum safety to end users.

RT9014/A can operate stably with very small ceramic output capacitors, reducing required board space and component cost. RT9014/A is available in fixed output voltages in the WDFN-10L 3x3 package.

Ordering Information

RT9014/A-□□□□

- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
- Output Voltage : VOUT1/VOUT2
  FM : 1.50V/2.80V, FP : 1.50V/3.00V
  GK : 1.80V/2.60V, GM : 1.80V/2.80V
  GP : 1.80V/3.00V, JG : 2.50V/1.80V
  JM : 2.50V/2.80V, JP : 2.50V/3.00V
  JN : 2.50V/2.85V, PP : 3.00V/3.00V
- EN Function Independent
- EN Function Dependent

Note :

RichTek Pb-free products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

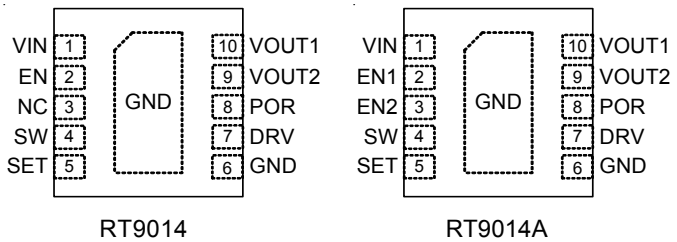
- **Wide Operating Voltage Ranges : 2.5V to 5.5V**
- **Low-Noise for RF Application**
- **No Noise Bypass Capacitor Required**
- **Fast Response in Line/Load Transient**
- **TTL-Logic-Controlled Shutdown Input**
- **Low Temperature Coefficient**
- **Dual LDO Outputs (300mA/300mA)**
- **1 Open-Drain Driver**
- **Ultra-low Quiescent Current 27μA/LDO**
- **High Output Accuracy 2%**
- **Short Circuit Protection**
- **Thermal Shutdown Protection**
- **Current Limit Protection**
- **Short Circuit Thermal Folded Back Protection**
- **Tiny 10-Lead WDFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- CDMA/GSM Cellular Handsets
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- Portable Information Appliances

Pin Configurations

(TOP VIEW)

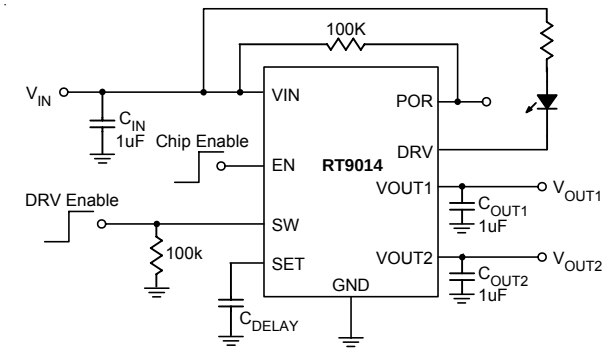


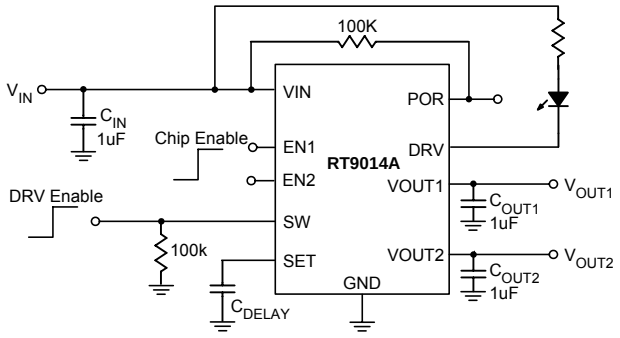
WDFN-10L 3x3

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

Typical Application Circuit





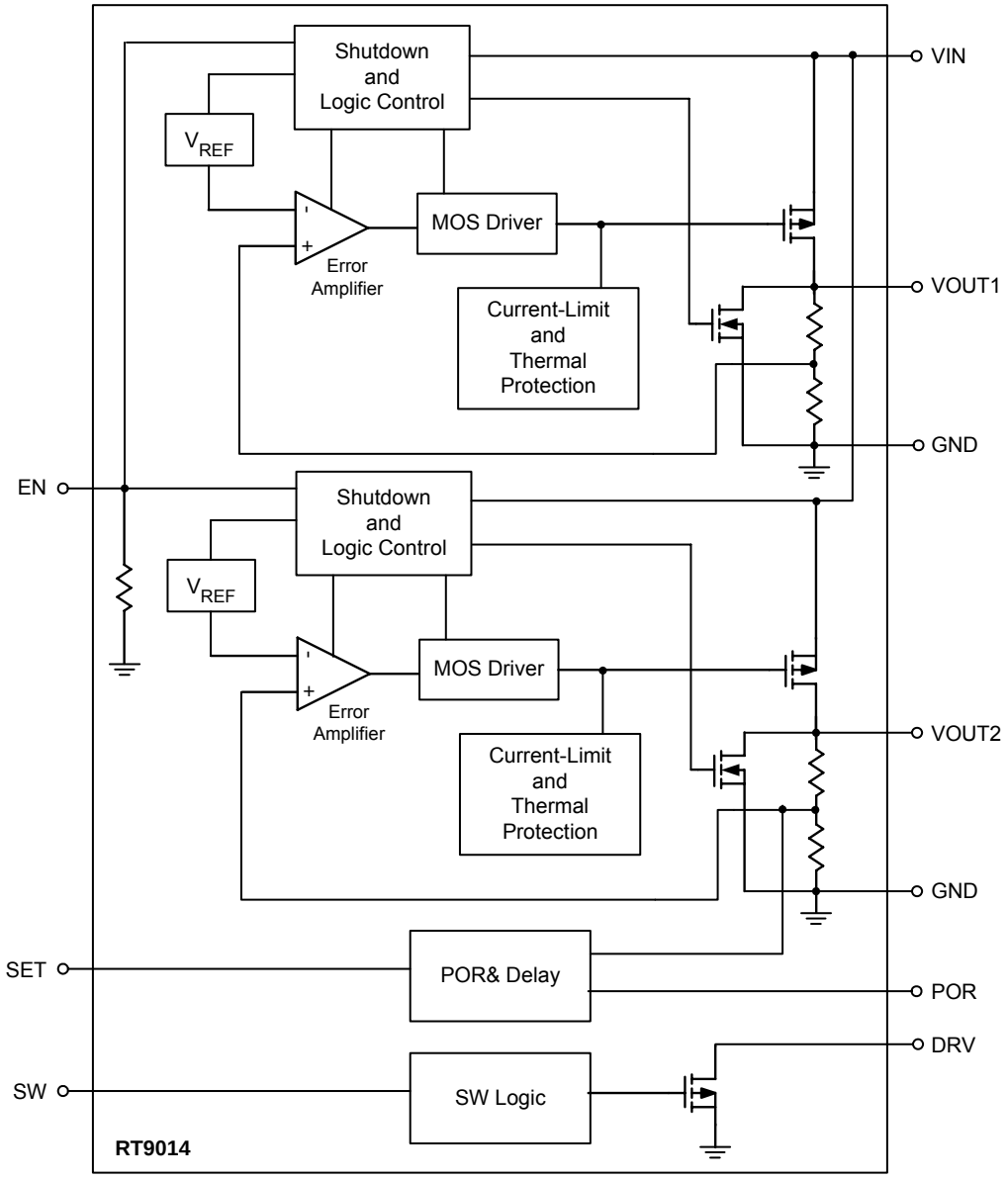
Functional Pin Description

Pin No.		Pin Name	Pin Function
RT9014-□□PQW	RT9014A-□□PQW		
1	1	VIN	Supply Input
2	--	EN	Chip Enable (Active High)
--	2	EN1	Chip Enable 1 (Active High)
--	3	EN2	Chip Enable 2 (Active High)
3	--	NC	No Internal Connection Pin.
4	4	SW	Active high signal drives open-drain N-Channel MOSFET. Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
5	5	SET	Delay Set Input: Connect external capacitor to GND to set the internal delay for the POR output. When left open, there is no delay. This pin cannot be grounded.
6	6	GND	Common Ground
7	7	DRV	Open-Drain Output: Capable of sinking 150mA.
8	8	POR	Power-On Reset Output: Open-drain output. Active low indicates an output under-voltage condition on regulator 2.
9	9	VOUT2	Channel 2 Output Voltage
10	10	VOUT1	Channel 1 Output Voltage
Exposed Pad	Exposed Pad	GND	Exposed pad should be soldered to PCB board and connected to GND.

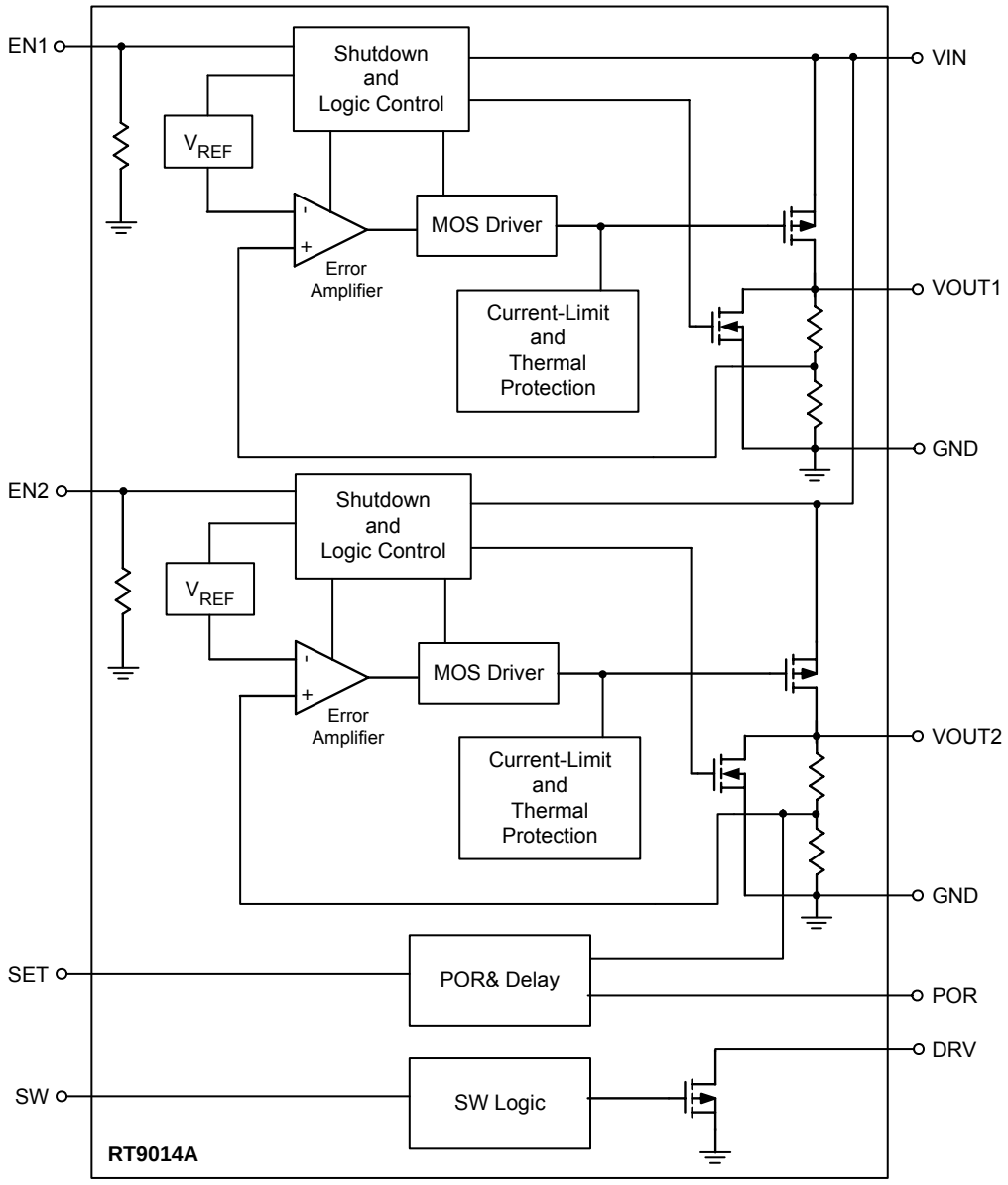
Available Voltage Version

Voltage	C	F	W	G	D	Y	H	E	J	K	T
Code	1.2	1.5	1.6	1.8	1.85	1.9	2	2.1	2.5	2.6	2.65
Voltage	L	M	N	V	P	Q	R	S	--	--	--
Code	2.7	2.8	2.85	2.9	3	3.1	3.2	3.3	--	--	--

Function Block Diagram



To be continued


EN1
Shutdown and Logic Control
VIN
VREF
MOS Driver
Error Amplifier
VOUT1
Current-Limit and Thermal Protection
GND
EN2
Shutdown and Logic Control
VREF
MOS Driver
Error Amplifier
VOUT2
Current-Limit and Thermal Protection
GND
SET
POR& Delay
POR
DRV
SW
SW Logic
RT9014A

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6V
- Other I/O Pin Voltages ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10L 3x3 ---------- 0.926W
- Package Thermal Resistance (Note 4)
  WDFN-10L 3x3, θ_{JA} ---------- 108°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 2.5V to 5.5V
- Enable Input Voltage ---------- 0V to 5.5V
- Operation Junction Temperature Range ---------- –40°C to 125°C
- Operation Ambient Temperature Range ---------- 0°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1µF, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}	V_{IN} = 2.5V to 5.5V	2.5	--	5.5	V
Dropout Voltage (Note 5)	V_{DROP}	I_{OUT} = 150mA	--	120	--	mV
		I_{OUT} = 300mA	--	240	--	mV
Output voltage range	V_{OUT}		1.2	--	3.6	V
V_{OUT} Accuracy	ΔV	I_{OUT} = 1mA	-2	--	+2	%
Line Regulation	ΔV_{LINE}	V_{IN} = (V_{OUT} + 0.3V) to 5.5V or V_{IN} > 2.5V, whichever is larger	--	--	0.2	%/V
Load Regulation	ΔV_{LOAD}	1mA < I_{OUT}< 300mA	--	--	0.6	%
Current Limit		R_{LOAD} = 1Ω	330	450	700	mA
Quiescent Current	I_Q	V_{EN} > 1.5V	--	58	80	uA
Shutdown Current	I_{Q_SD}	V_{EN} < 0.4V	--	--	1	uA
EN Threshold	V_{IH}	V_{IN} = 2.5V to 5.5V, Power On	1.5	--	--	V
	V_{IL}	V_{IN} = 2.5V to 5.5V, Shutdown	--	--	0.4	
Output Voltage TC			--	100	--	ppm/°C
Thermal Shutdown	T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	40	--	°C

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PSRR I_{LOAD} = 10mA	PSRR	f =100Hz	--	65	--	dB
		f =1kHz	--	60	--	dB
		f =10kHz	--	50	--	dB
PSRR I_{LOAD} = 150mA	PSRR	f =100Hz	--	65	--	dB
		f =1kHz	--	50	--	dB
		f =10kHz	--	50	--	dB
Power Good						
Reset Threshold	V_{THL}	Low Threshold, % of nominal V_{OUT2} (Flag On)	90	--	--	%
	V_{THH}	High Threshold, % of nominal V_{OUT2} (Flag Off)	--	--	96	%
POR Output Logic Low Voltage	V_{OL}	I_{LOW} = 250uA	--	0.02	0.1	V
POR Leakage Current	I_{POR}	Flag Off	-1	0.01	1	μA
Set pin current source		V_{SET} = 0	0.60	1.25	1.70	μA
Set pin threshold		POR = high	--	1.4	--	V
DRV output						
Voltage Low		I_{DRV} = 150mA	--	0.2	0.5	V
Leakage current		I_{DRV} = 0mA, V_{DRV} = 5V, SW = 0V	-1	0.01	1	μA
SW input current		V_{IL} < 0.6V(DRV Shutdown)	-1	0.01	1	μA
		V_{IH} > 2.5V(DRV Enable)	-1	0.01	1	μA
SW input voltage	V_{IL}	Logic Low	--	--	0.4	V
	V_{IH}	Logic High	1.5	--	--	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

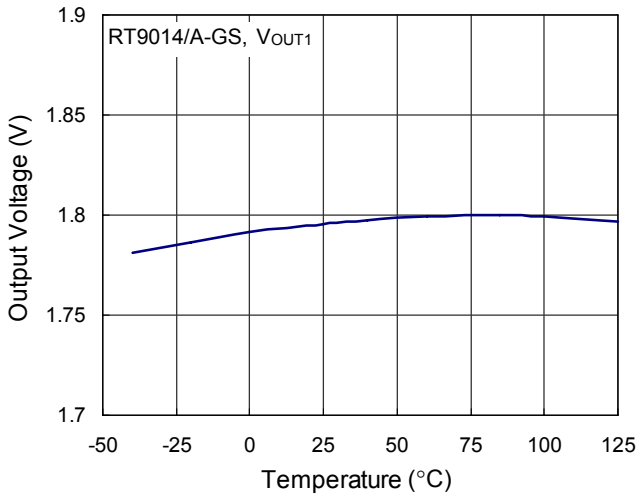
Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

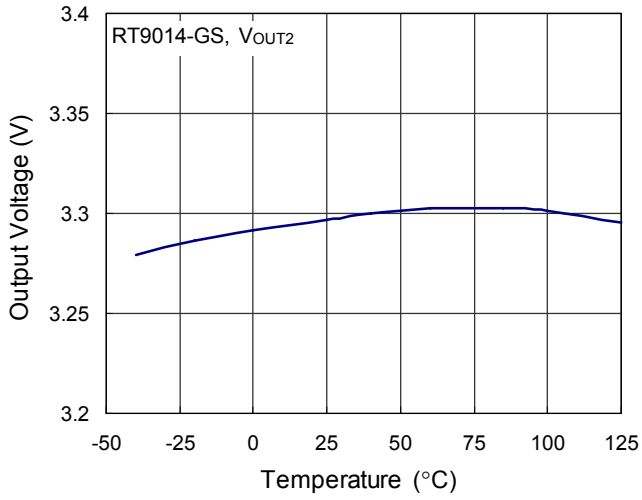
Note 5. The dropout voltage is defined as V_{IN} -V_{OUT}, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ − 100mV.

Typical Operating Characteristics

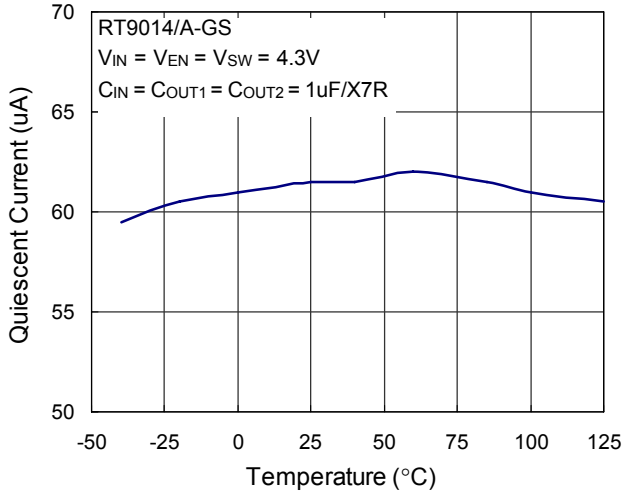
Output Voltage vs. Temperature



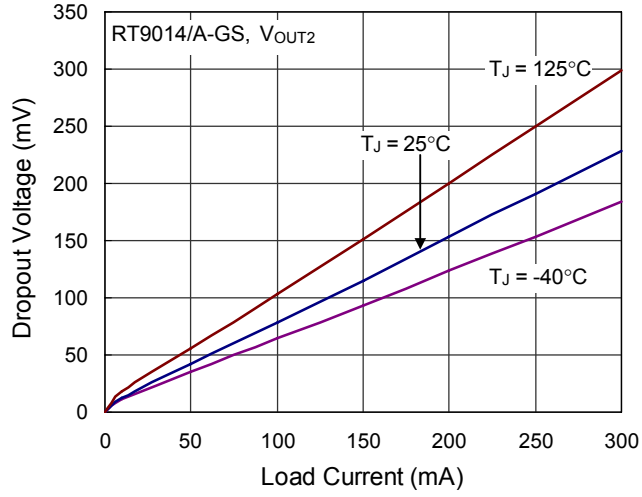
Output Voltage vs. Temperature



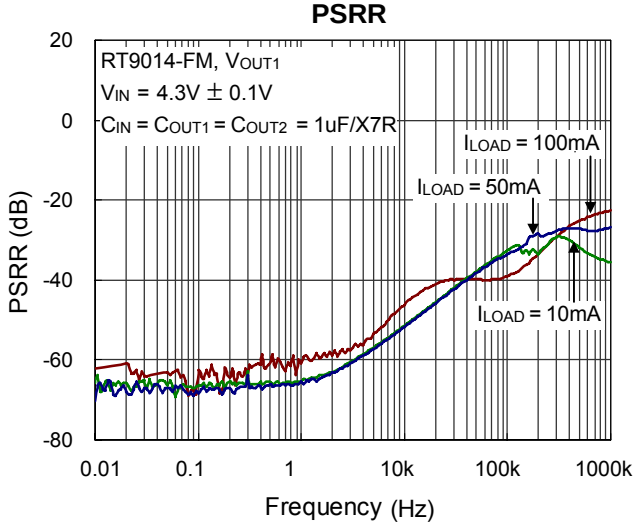
Quiescent Current vs. Temperature



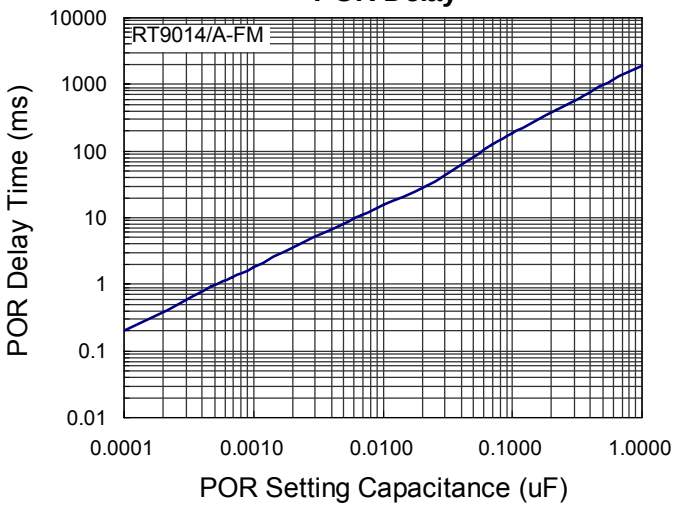
Dropout Voltage vs. Load Current



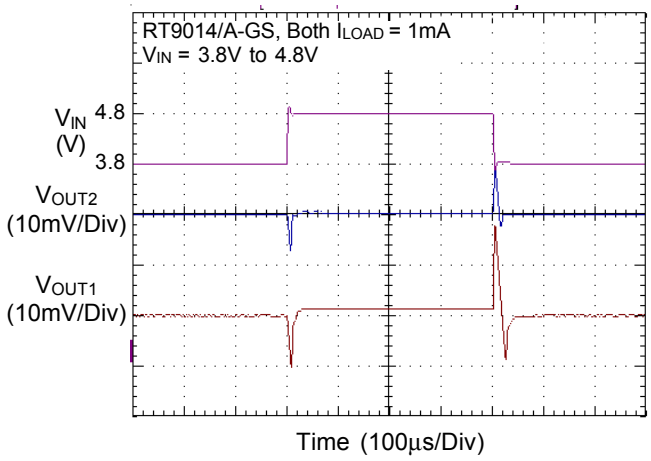
PSRR



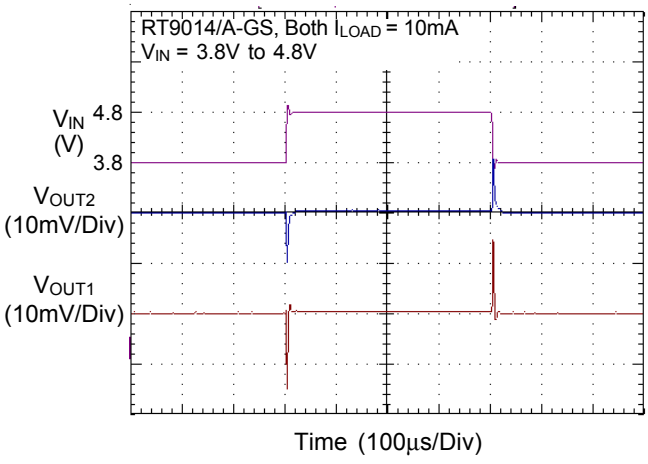
POR Delay



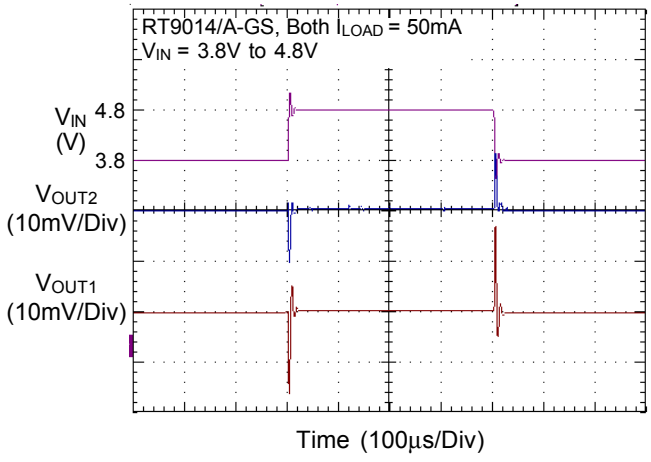
Line Transient Response



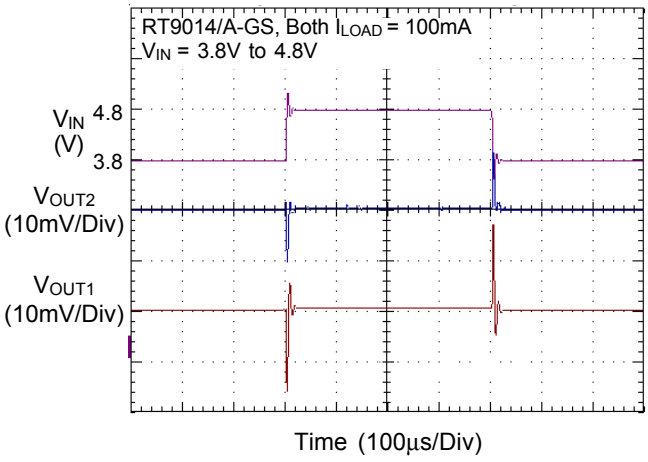
Line Transient Response



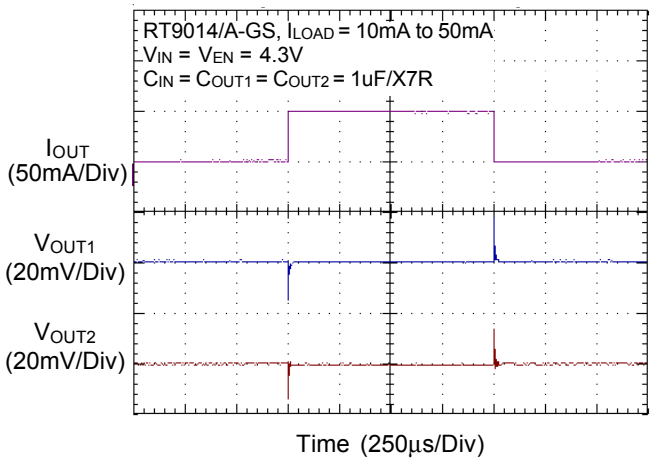
Line Transient Response



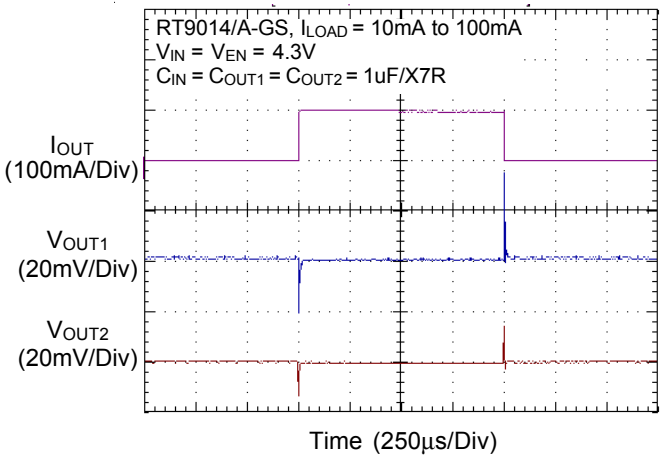
Line Transient Response



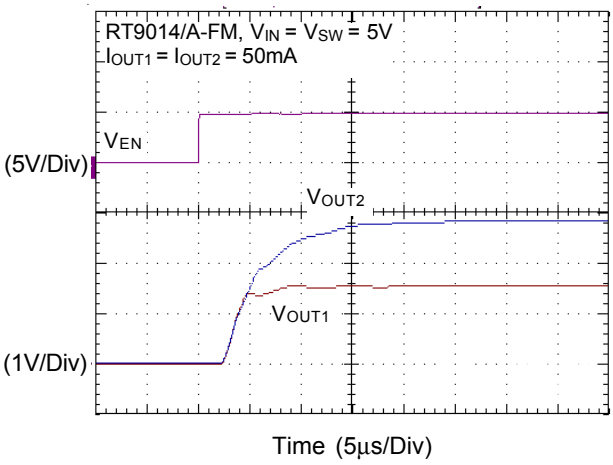
Load Transient Response



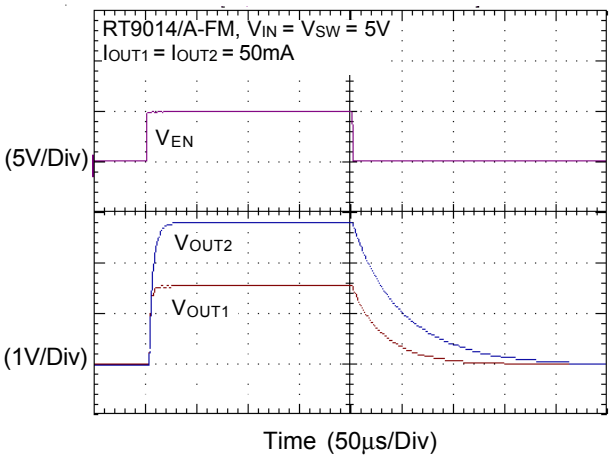
Load Transient Response



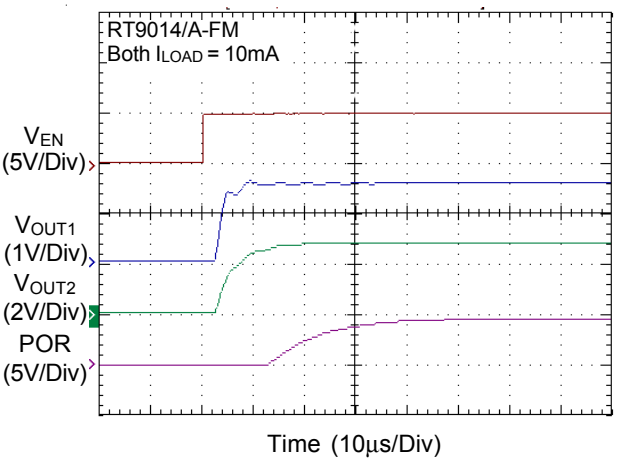
Start Up



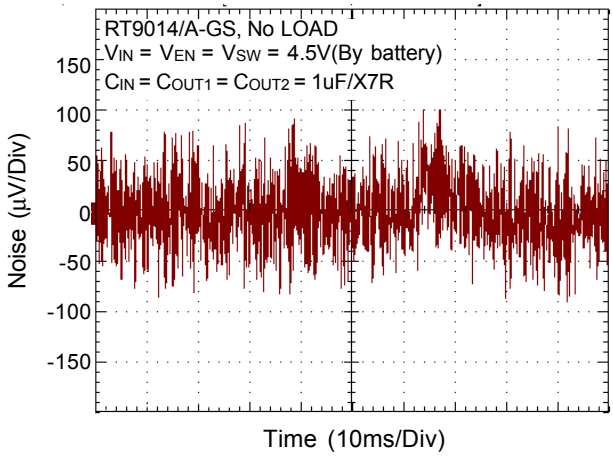
EN Pin Shutdown Response



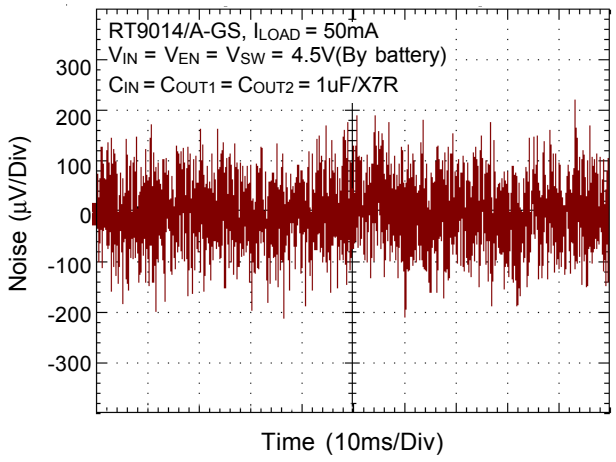
Power-On



Noise



Noise



Applications Information

Like any low-dropout regulator, the external capacitors used with the RT9014/A must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the RT9014/A input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9014/A is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 20mΩ on the RT9014/A output ensures stability. The RT9014/A still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9014/A and returned to a clean analog ground.

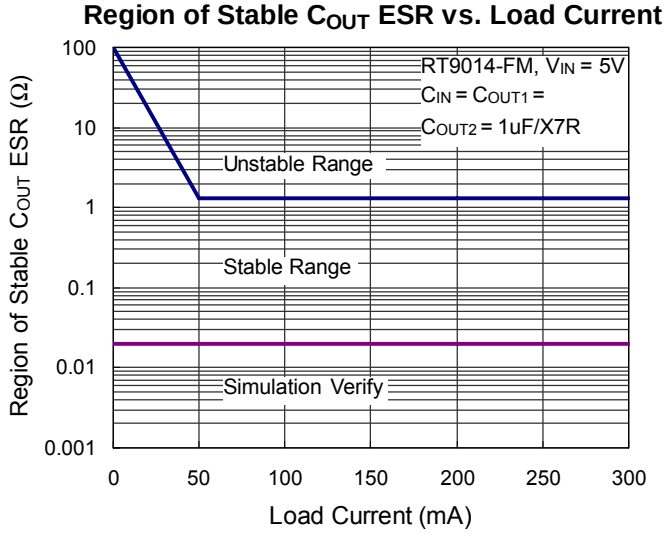


Figure 1. Stable Cout ESR Range

Thermal Considerations

Thermal protection limits power dissipation in RT9014/A. When the operation junction temperature exceeds 170°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 40°C. RT9014/A lowers its OTP trip level from 170°C to 110°C when output short circuit occurs (V_{OUT} < 0.4V) as shown in Figure 2. It limits IC case temperature under 100°C and provides maximum safety to customer while output short circuit occurring.

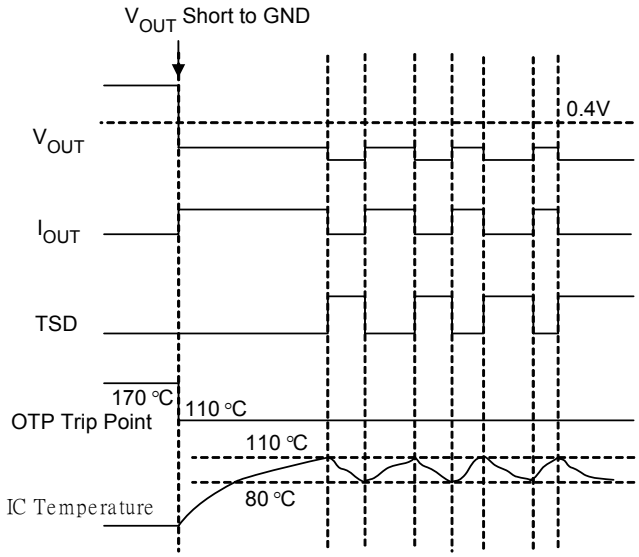


Figure 2. Short Circuit Thermal Folded Back Protection when Output Short Circuit Occurs (Patent)

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9014/A, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the operated ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for WDFN-10L 3x3 package is 108°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / 108 = 0.926W for WDFN-10L 3x3 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9014/A packages, the Figure 3 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

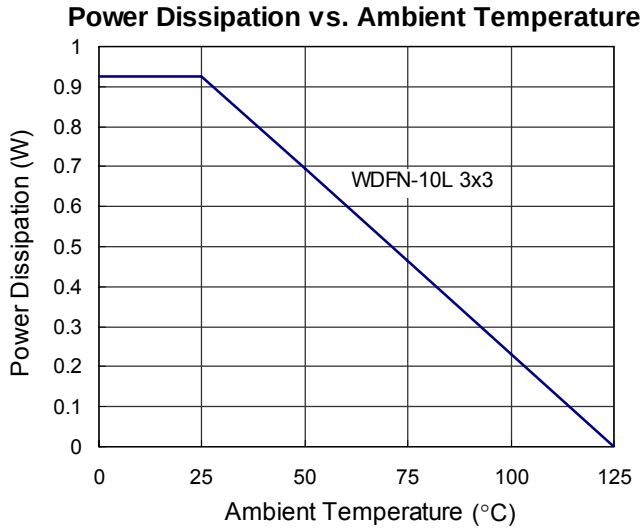
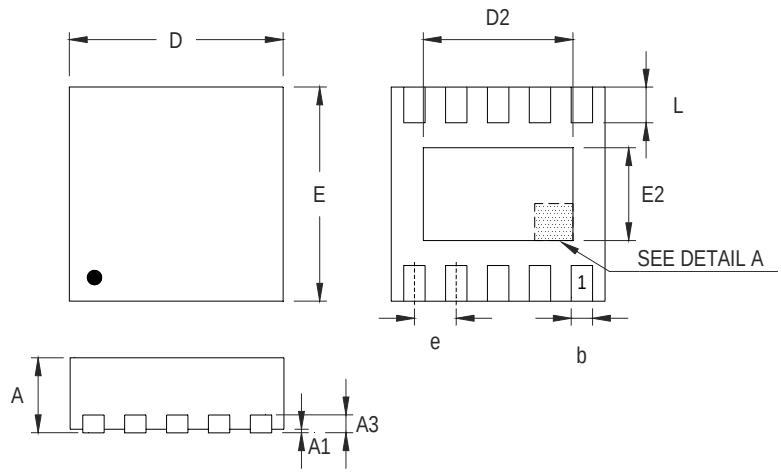
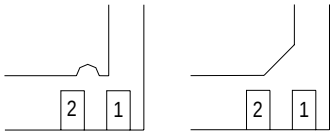


Figure 3. Derating Curves for RT9014/A Packages

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

RICHTEK TECHNOLOGY CORP.

Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

RICHTEK TECHNOLOGY CORP.

Taipei Office (Marketing)
8F-1, No. 137, Lane 235, Paochiao Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)89191466 Fax: (8862)89191465
Email: marketing@richtek.com