Low-cost Green-Mode PWM Controller for Flyback Converters **SG6848x1**

FEATURES

- Green-mode PWM Controller
- Low Start-up Current (5uA)
- Low Operating Current (3mA)
- Programmable PWM Frequency
- Peak-current-mode Operation
- Leading-edge Blanking
- Built-in Synchronized Slope Compensation
- Cycle-by-cycle Current Limiting
- Constant Output Power Limit
- Gate Output Voltage Clamped at 15V
- Small SOT-26 Package Available

APPLICATIONS

General-purpose switching mode power supplies and flyback power converters, such as

- Battery chargers
- Power adapters
- Open-frame SMPS
- Replacements for linear transformers and RCC
- 5V standby power for PC power supply.

DESCRIPTION

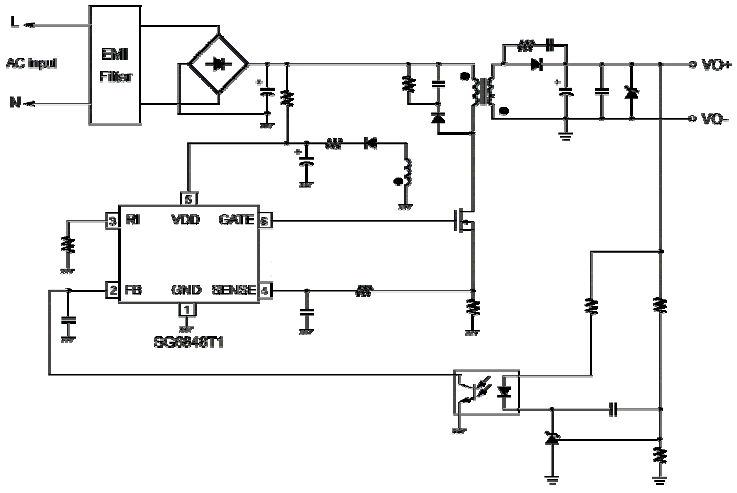
This highly integrated PWM controller provides several special enhancements designed to meet the low

standby-power needs of low-power SMPS. To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to continuously decrease PWM frequency under light-load conditions. This green-mode function enables the power supply to easily meet even the strictest power conservation requirements.

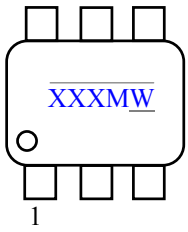
The BiCMOS fabrication process enables reducing the start-up current to 5uA, and the operating current to 3mA. As a result, a large start-up resistance can be used. Built-in synchronized slope compensation ensures the stability of peak-current-mode control. Proprietary internal compensation provides a constant output power limit over a universal AC input range (90VAC to 264VAC). Cycle-by-cycle current limiting ensures safe operation during short-circuits.

To protect the external power MOSFET from being damaged by supply over voltage, the SG6848x1's output driver is clamped at 15V. The SG6848x1's controllers can be used to improve the performance and reduce the production cost of power supplies. The SG6848x1 is the best choice for replacing linear and RCC power supplies. It is available in DIP-8 and SOT-26 packages.

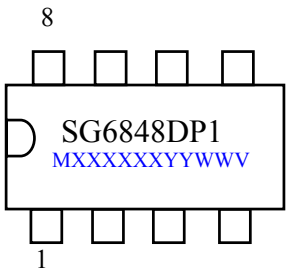
TYPICAL APPLICATION



MARKING DIAGRAMS

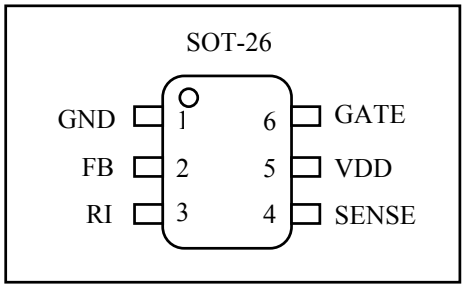


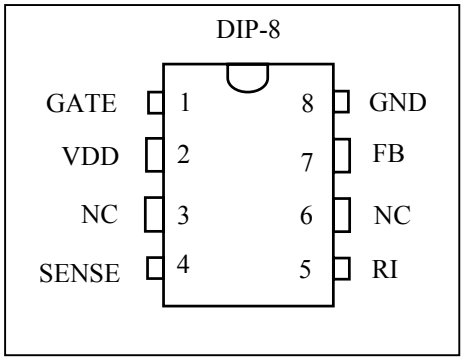
XXX:AAH =SG6848T1
XXX:AAH =SG6848TZ1
M: Mask Version
W: Week code A~Z=W1~W26
A~Z=W27~W52
_____ :Lead free package



D: D = DIP
P : Z = Lead Free
Null = Regular Package
M: Mask Version
XXXXXX: Wafer Lot
YY: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION





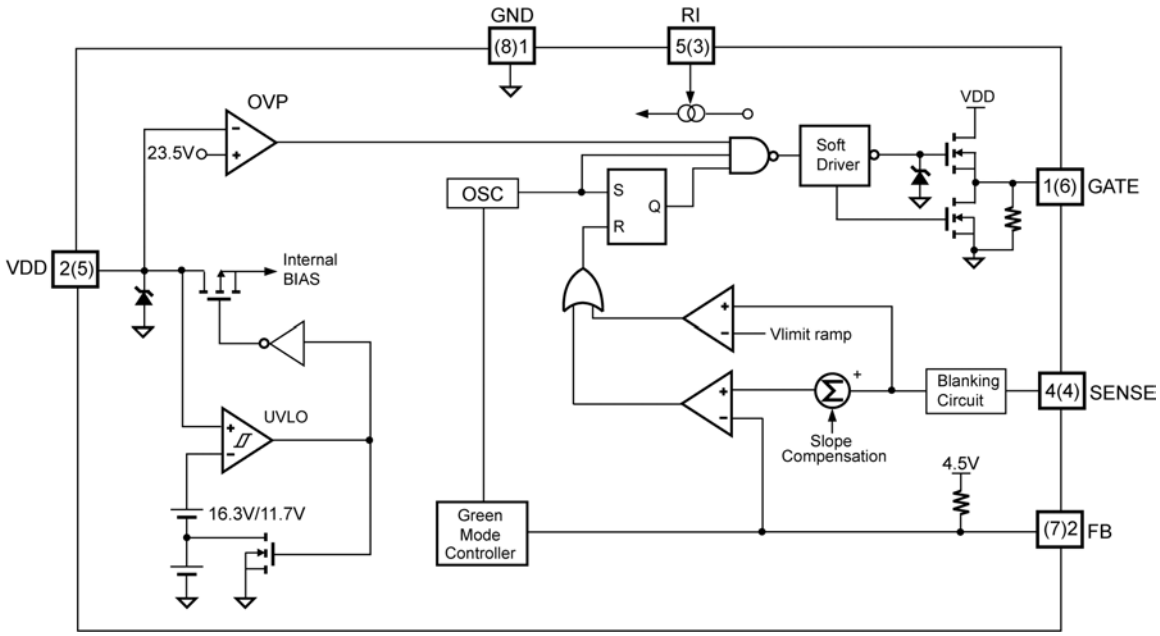
ORDERING INFORMATION

Part Number	Package
SG6848T1	SOT-26
SG6848D1	DIP-8
SG6848TZ1	SOT-26 (Lead Free)
SG6848DZ1	DIP-8 (Lead Free)

PIN DESCRIPTIONS

Name	Pin No. DIP-8 / (SOT-26)	Type	Function
GATE	1 / (6)	Driver Output	The totem-pole output driver for driving the power MOSFET.
VDD	2 / (5)	Supply	Power supply.
NC	3		No connection.
SENSE	4 / (4)	Analog Input	Current sense. This pin senses the voltage across a resistor for peak-current-mode control. If the voltage reaches the internal threshold, PWM output is disabled. This activates cycle-by-cycle current limiting.
RI	5 / (3)	Analog Input/Output	A resistor connected from the RI pin to GND pin will generate a constant current source for the controller. This current is used to determine PWM frequency. Increasing the resistance will reduce PWM frequency. A 95kΩ resistor results in a 70kHz PWM frequency.
NC	6		No connection.
FB	7 / (2)	Analog Input	Feedback. The FB pin accepts the output voltage regulation signal. It provides feedback to the internal PWM comparator to adjust the duty cycle.
GND	8 / (1)	Supply	Ground.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	DC Supply Voltage		25	V
V_{FB}	Input Voltage to FB Pin		-0.3 to 6 V	V
V_{SENSE}	Input Voltage to Sense Pin		-0.3 to 6V	V
P_D	Power Dissipation		300	mW
$R_{\theta JA}$	Thermal Resistance (Junction to Air)	SOT-26	208.4	°C/W
		DIP-8	82.5	°C/W
T_J	Operating Junction Temperature		-40 to +125	°C
T_{STG}	Storage Temperature Range		-55 to +150	°C
T_R	Peak Reflow Temperature	Pb free	260(+5/-0)	°C
		Pb	230(+5/-0)	

* All voltage values, except differential voltages, are given with respect to GND pin.

* Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

RECOMMENDED OPERATING JUNCTION TEMPERATURE: -30°C ~ 105°C*

*For proper operation

ELECTRICAL CHARACTERISTICS (V_{DD}=15V, T_A = 25°C, unless noted)

VDD Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OP}	Continuously Operating Voltage				20	V
$V_{TH(ON)}$	Start-up Threshold Voltage		15.3	16.3	17.3	V
$V_{DD(MIN)}$	Min. Operating Voltage		10.9	11.7	12.5	V
$I_{DD\ ST}$	Start-up Current			5	30	uA
$I_{DD\ OP}$	Operating Supply Current	GATE = 1nF		3	5	mA
V_{DD-OVP}	Over Voltage Protection		22	23.5	25	V

Feedback Input Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_{FB}	Input Impedance			2		kΩ
I_{OZ}	Zero-duty-cycle Input Current			1.3	2.0	mA
V_{OP}	Open Loop Voltage			4.5		V

Oscillator Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{OSC}	PWM Frequency	RI = 95kΩ	65	70	75	kHz
$F_{OSC-GREEN}$	Green-mode Min. Frequency	RI = 95kΩ		15		kHz
F_{DY}	Frequency Variation versus V_{DD} Deviation	V_{DD} = 14 to 20V			2	%
F_{DT}	Frequency Variation versus Temp. Deviation	T_A = -30 to 105 ℃			2	%
I_N	Green-mode Start Threshold FB Input Current			1		mA
I_G	Green-mode Min. Freq. FB Input Current			1.16		mA
S_G	Green-mode Modulation Slope	RI = 95kΩ		300		Hz/uA
R_I	RI pin resistance		66.5		150	kΩ

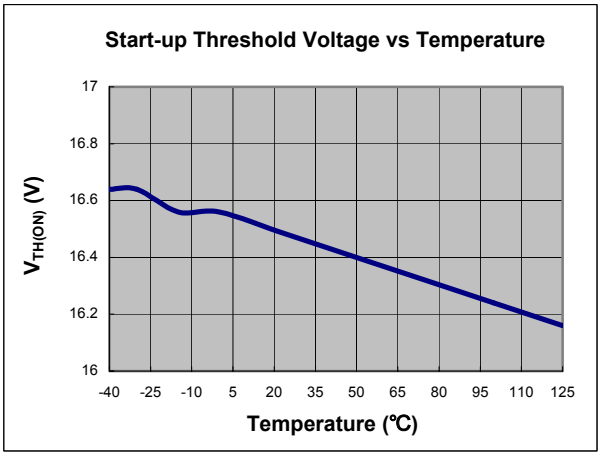
Current Sense Section

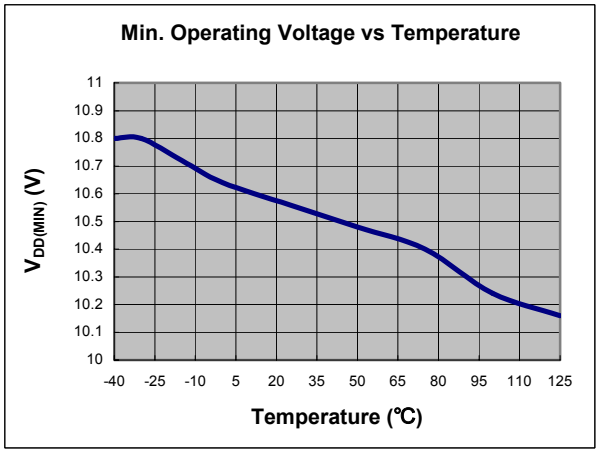
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_{CS}	Input Impedance			10		kΩ
T_{PD}	Delay to Output			100		nsec
$V_{TH,FLT}$	Current Limit Flatten Threshold Voltage			0.96		V
$V_{TH,VALLEY}$	Current Limit Valley Threshold Voltage			0.81		V
DC_{SAW}	Duty Cycle of SAW Limit			45		%

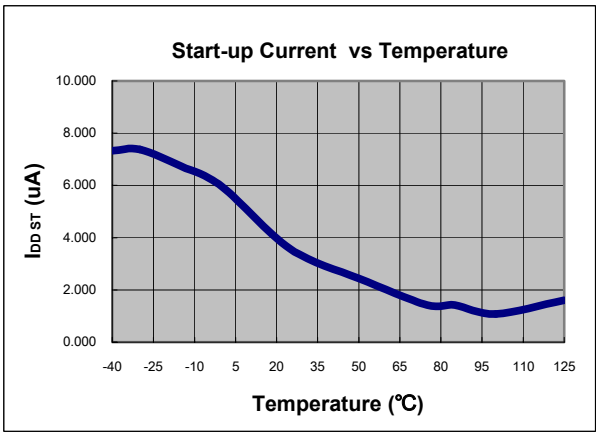
Gate Section

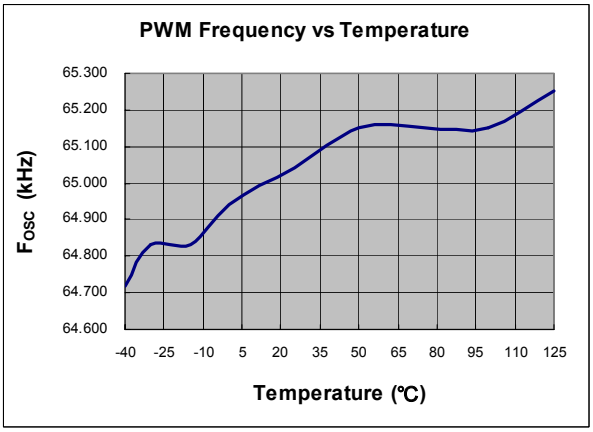
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$DC_{(MAX)}$	Maximum Duty Cycle		70	75	80	%
$DC_{(MIN)}$	Minimum Duty Cycle			0		%
B_{NK}	Leading-edge Blanking Time			200		nsec
V_{OL}	Output Voltage Low	Sink current = 20mA			1.5	V
V_{OH}	Output Voltage High	Source current = 20mA	8			V
T_R	Rising Time	GATE = 1nF		250		nsec
T_F	Falling Time	GATE = 1nF		80		nsec
V_{CLAMP}	Output Clamp Voltage	V_{DD} = 20V		15	17	V

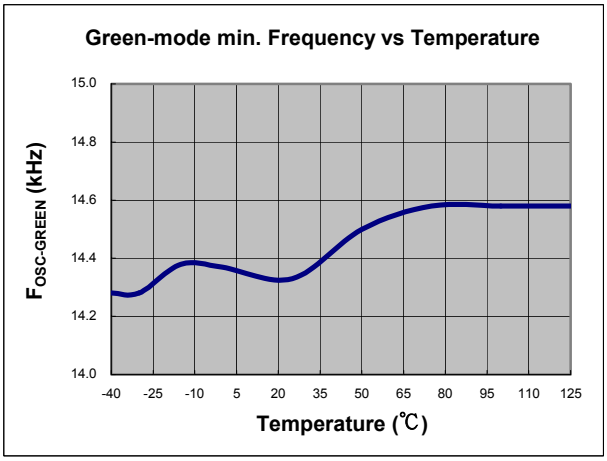
TYPICAL CHARACTERISTICS

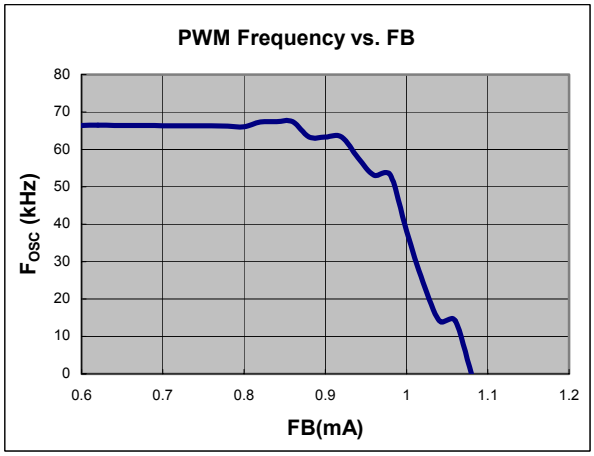












OPERATION DESCRIPTION

The SG6848x1 devices integrate many useful functions into one controller for low-power switching mode power supplies. The following descriptions highlight some of the features of the SG6848D1.

Start-up Circuitry

When the power is turned on, the input rectified voltage, Vdc, charges the hold-up capacitor C1 via a start-up resistor R_{IN}. As the voltage of VDD pin reaches the start threshold voltage $V_{TH(ON)}$, the SG6848x1 activates the entire power supply.

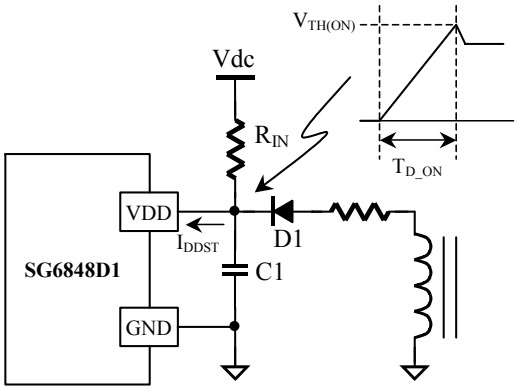


Figure 1. Power Circuit

The maximum power-on delay time is determined as follows,

$$V_{TH(ON)} = (V_{dc} - I_{DDST} \cdot R_{IN})\left[1 - e^{-\frac{T_{D_ON}}{R_{IN} \cdot C1}}\right] \quad (1)$$

where

I_{DDST} is the start-up current of SG6848x1;

T_{D_ON} is the power-on delay time of the power supply.

Due to the low start-up current, a large R_{IN} such as 1.5Mohm can be used. Also with a hold-up capacitor of 10uF/50V, the power-on delay T_{D_ON} is less than 2.8S for 90VAC input.

The FB input

This pin is designed for feedback control and to activate the green-mode function. Figure 2 is a typical feedback circuit mainly consisting of a shunt regulator and an opto-coupler. R_1 and R2 form a voltage divider for the output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47ohm, C_{FB}= 1nF) placed from the FB pin to GND can increase stability. The maximum source current on the FB pin is 2mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. Thus, the value of the biasing resistor Rb is determined as follows,

$$\frac{V_o - V_D - V_Z}{Rb} \cdot K \geq 2mA \quad (2)$$

where V_D is the drop voltage of a photodiode, about 1.2V;

V_Z is the minimum operating voltage of the shunt regulator. Typical value is 2.5V;

K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage Vo=5V, with CTR=100%, the maximum value of Rb is 650ohm.

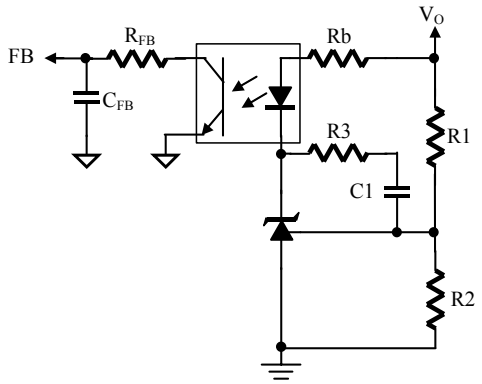


Figure 2. Feedback circuit.

Oscillator & Green Mode Operation

One external resistor, R_{Ii}, connected between RI and GND pins is used to program the PWM frequency of the SG6848x1. The approximated formula is:

$$F_{OSC}(KHz) = \frac{6650}{R_I(Kohm)} \qquad (3)$$

The recommended F_{OSC} is from 50 to 100KHz.

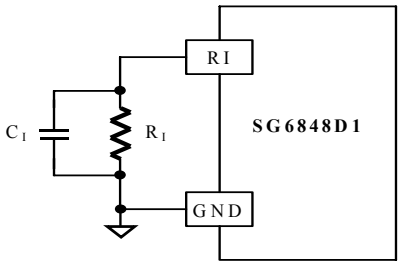


Figure 3. Setting PWM frequency

The patented green-mode function provides off-time modulation to reduce the PWM frequency at light-load and no-load conditions. The sink current of the FB pin determines the green mode operation as shown in Figure 4. At light load, the sink current of the FB pin will increase. When the sink current is larger than 1mA, the PWM frequency decreases in order to reduce the power consumption of the power supply at light-load and in no-load conditions.

For lightning surge tests, a small capacitor (not over 50pF) connected from the RI pin to GND is recommended. This added capacitor also improves stability, especially at light load and high input line voltage conditions.

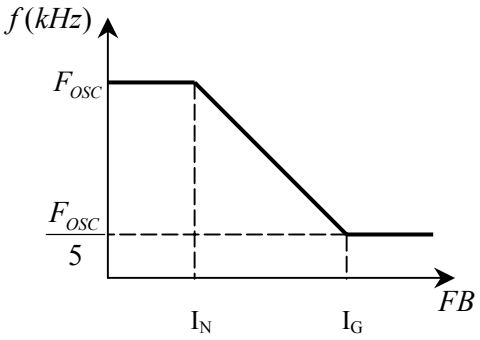


Figure 4. PWM frequency vs. FB current.

Built-in Slope Compensation

A flyback converter can be operated in either discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages to operating the converter in CCM. With the same output power, a converter in CCM exhibits smaller peak inductor currents than one in DCM. Therefore, a small-sized transformer and a low-rated MOSFET can be applied. On the secondary side of the transformer, the rms output current of DCM can be up to twice that of CCM. Larger wire gauge and output capacitors with larger ripple current ratings are required. DCM operation also results in higher output voltage spikes. A large LC filter must also be added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of operating in CCM, there is one concern–stability. Operating in CCM, the output power is proportional to the average inductor current, while the peak current is controlled. This causes the well-known sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent this oscillation. The SG6848x1 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. The sensed voltage together with this slope compensation signal (V_{SLOPE}) is fed into the non-inverting input of the PWM comparator. The resulting voltage is compared with the FB signal to adjust the PWM duty cycle, such that the output voltage is regulated. Therefore, users can use the SG6848x1 to design a cost-effective, highly efficient and compact sized flyback power supply operating in CCM without adding any external components.

The positive ramp added is,

$$V_{SLOPE} = V_{SL} \cdot D \qquad (4)$$

where
V_{SL} = 0.33V;

D = Duty cycle

Constant Output Power Limit

The maximum output power of a flyback converter can generally be determined from the current-sense resistor R_S. When the load increases, the peak inductor current increases accordingly. When the output current arrives at the protection value, the OCP comparator dominates the current control loop. OCP occurs when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay, td. The delay time results in unequal power-limit level under universal input. In the SG6848x1, a saw-tooth power-limiter is designed to solve the unequal power-limit problem. As shown in Figure 5, the power limiter is designed as a positive ramp signal and is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs. However, with fixed propagation delay, td, the peak primary current would be the same for various line input voltages. Therefore the maximum output power can practically be limited to a constant value within a wide input voltage range without adding any external circuitry.

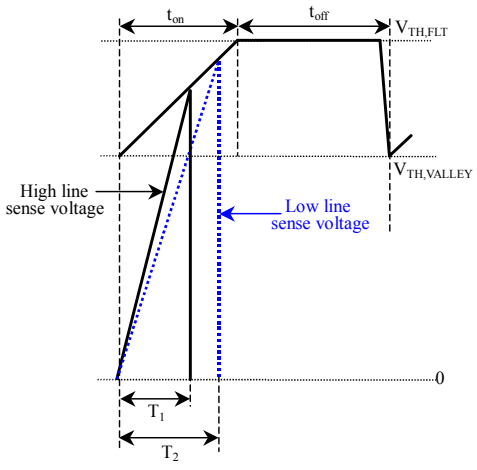


Figure 5. Constant power limit compensation

Short Circuit Protection

When the output of a flyback power supply is shorted, the primary VDD will decrease due to the coupling polarity between the aux winding and the secondary winding of a transformer. When V_{DD} drops below the UVLO level of the SG6848x1, the power supply will enter hiccup operation mode and hence limit the output power. However, it is possible that the V_{DD} voltage remains higher than the UVLO level even if the output is shorted. This happens when the coupling between the aux and the primary winding is too good. Therefore, the construction of the transformer becomes a dominant factor. The recommended construction layout is to increase the insulation thickness for the aux winding and place the primary aux winding in one side of the bobbin. For low output voltage applications, using a low dropout voltage diode and a larger secondary winding also helps.

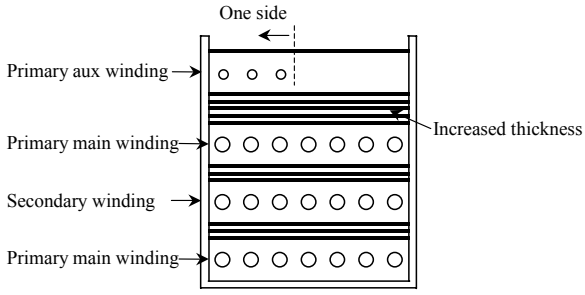


Figure 6. Transformer construction

Leading-Edge Blanking

A voltage signal proportional to the MOSFET current develops on the current-sensing resistor, R_S. Each time the MOSFET is turned on, a spike, which is induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, inevitably appears on the sensed signal. Inside the SG6848x1, a leading-edge blanking time of about 200 nsec. is introduced to avoid premature termination of the MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100ohm + 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the R_S is recommended.

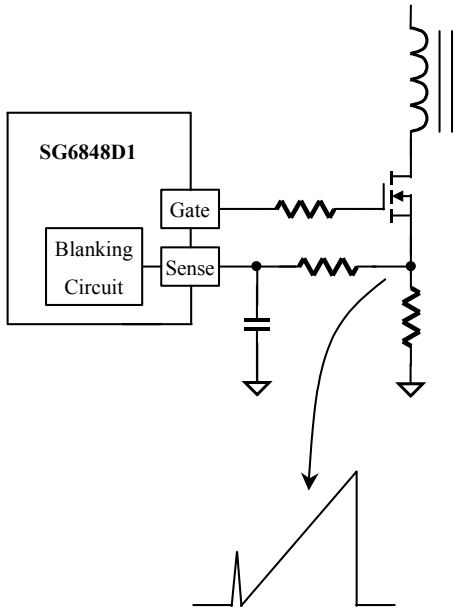


Figure 7. Turn on spike

Gate Drive

The SG6848x1's output stage is a fast totem pole driver that can drive a MOSFET gate directly. It is also equipped with a voltage clamping Zener diode to protect the MOSFET from damage caused by undesirable over-drive voltage. The output voltage is clamped at 15V. An internal pull-down resistor is used to avoid a floating state of the gate before startup. A gate drive resistor in the range of 47 to 100ohm is recommended. This resistor limits the peak gate drive current and provides damping to prevent oscillations at the MOSFET gate terminal.

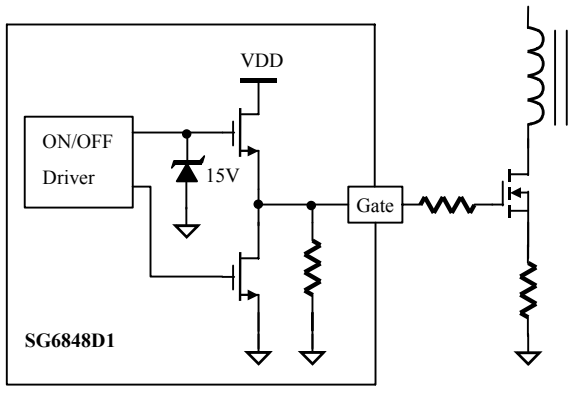


Figure 8. Gate drive

Lab Note

Before reworking or soldering/de-soldering on the power supply, it is suggested to discharge the primary capacitors by an external bleeding resistor. Otherwise the PWM IC may be destroyed by external high voltage during soldering or de-soldering.

This device is sensitive to ESD discharge. To improve the production yield, the production line should be ESD protected in accordance to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board (PCB) Layout

High frequency switching current/voltage makes PCB layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests. Here, we give some common guidelines:

In order to get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, and then to the switching circuits.

The high frequency current loop is in **C1 – Transformer – MOSFET – R_S – C1**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→**1**) short, direct, and wide. High voltage traces related to the drain of the MOSFET and the RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, it's better to connect this heatsink to a ground.

As indicated by **3**, the ground of control circuits should be connected first before any other circuitry.

As indicated by **2**, the area enclosed by the **transformer aux winding, D1, and C2** should also be kept small. Place C2 close to the SG6848x1 for good decoupling.

Two suggestions for ground connections, with different pro and cons, are offered.

GND3 → 2 → 4 → 1: This should avoid common impedance interference for the sense signal.

GND3→2→1→4: This should be better for ESD tests, where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary through the transformer's stray capacitance to GND2 first. Then the charge goes from GND2 to GND1 and back to the mains. It should be noted that control circuits should not be placed in the discharge path. Point discharges for common choke can decrease the high frequency impedance and help increase ESD immunity.

Should a Y-cap between primary and secondary be required, it is suggested to connect this Y-cap to the **positive terminal of C1 (Vdc)**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. The Point discharge of this Y-cap also helps with ESD. However, the distance between these two points should be at least 5mm according to safety requirements.

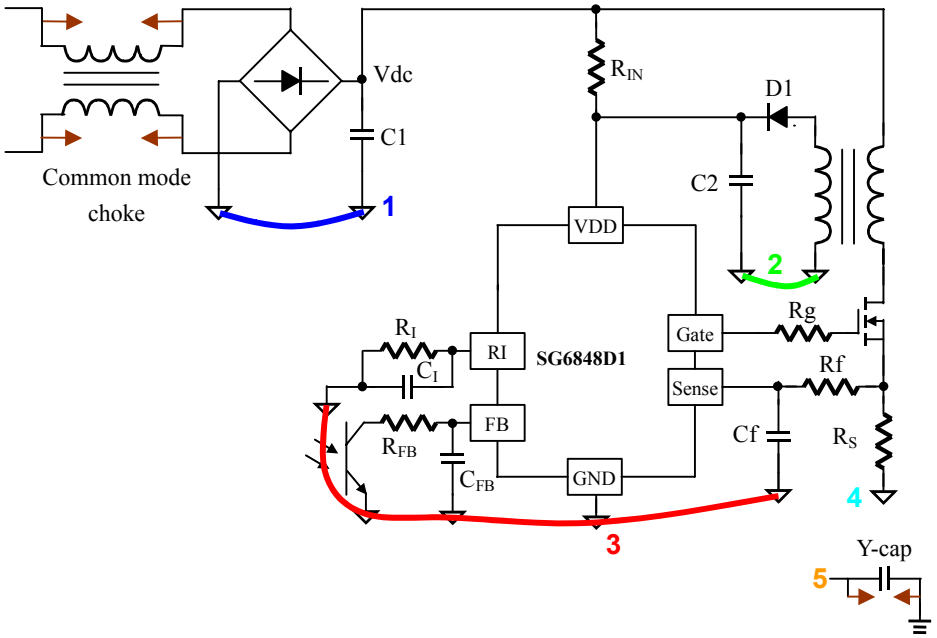
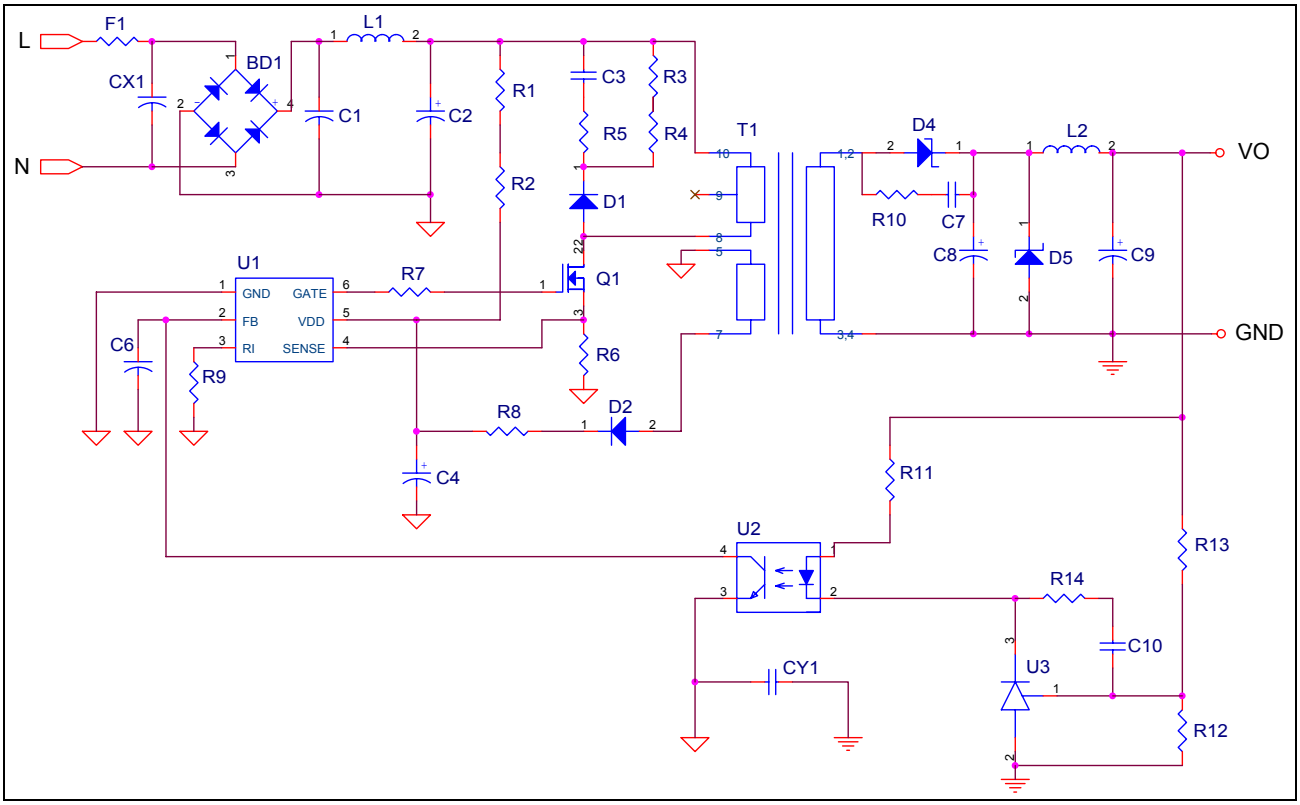


Figure 9. Layout considerations

REFERENCE CIRCUIT

Circuit 5V/1A

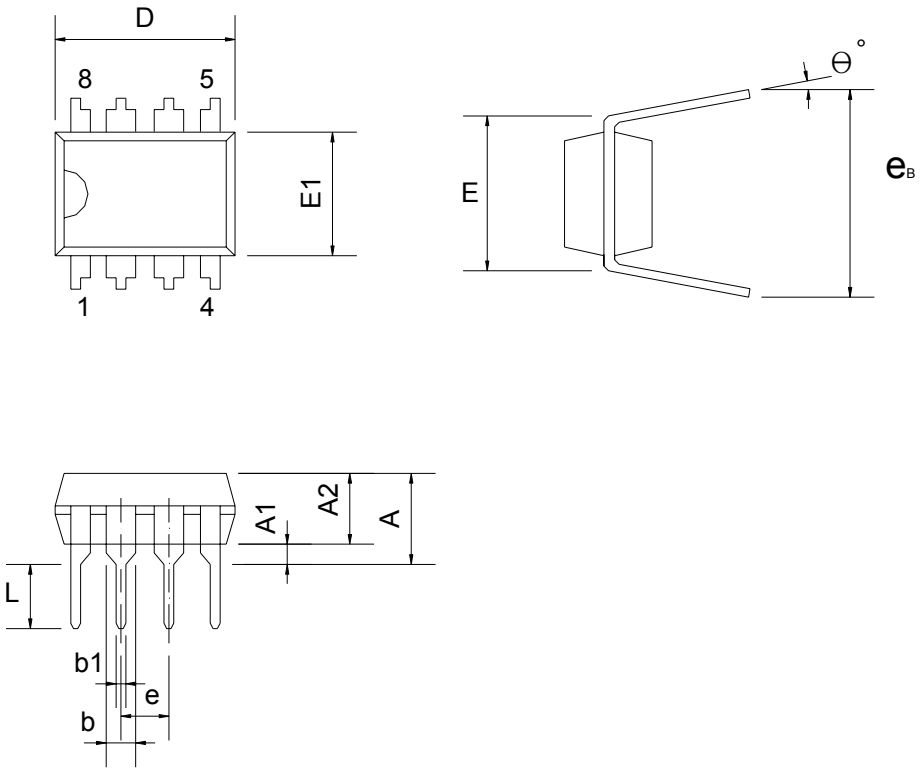


BOM

Reference	Component	Reference	Component
BD1	BD 1A/500V	L2	10uH 6mm
CX1 (Optional)	XC 0.1uF	Q1	MOSFET 1A/600V
CY1 (Optional)	YC 102P/400V (Y1)	R1, R2	R 750KΩ 1206
C2	EC 10uF/400V 105℃	R4, R3	R 47KΩ 1206
C1	CC 103P/500V	R5	R 47Ω 1206
C3	CC 102P/500V	R6	R 4.7Ω 1206
C4	EC 10u/50V	R7	R 100Ω 0805
C6	CC 472P 0805	R8	R 10Ω 1206
C7 (Optional)	CC 102P/100V 1206	R10 (Optional)	R 10Ω 1206
C8	EC 470u/10V 105℃	R9	R 100KΩ 0805
C9	EC 220u/10V 105℃	R11	R 100Ω 1/8W
C10	CC 222P 0805	R12	R 33KΩ 0805
D1	Diode FRI07	R13	R 33KΩ 1/8W
D2	Diode FR102	R14	R 4.7KΩ 0805
D4	Diode SB360	T1	EE-16
D5 (Optional)	ZD 6.8V 0.5W	U1	IC SG6848D1
F1	R 1Ω/0.5W	U2	PC817
L1	20mH 6*8mm	U3	TL431

PACKAGE INFORMATION

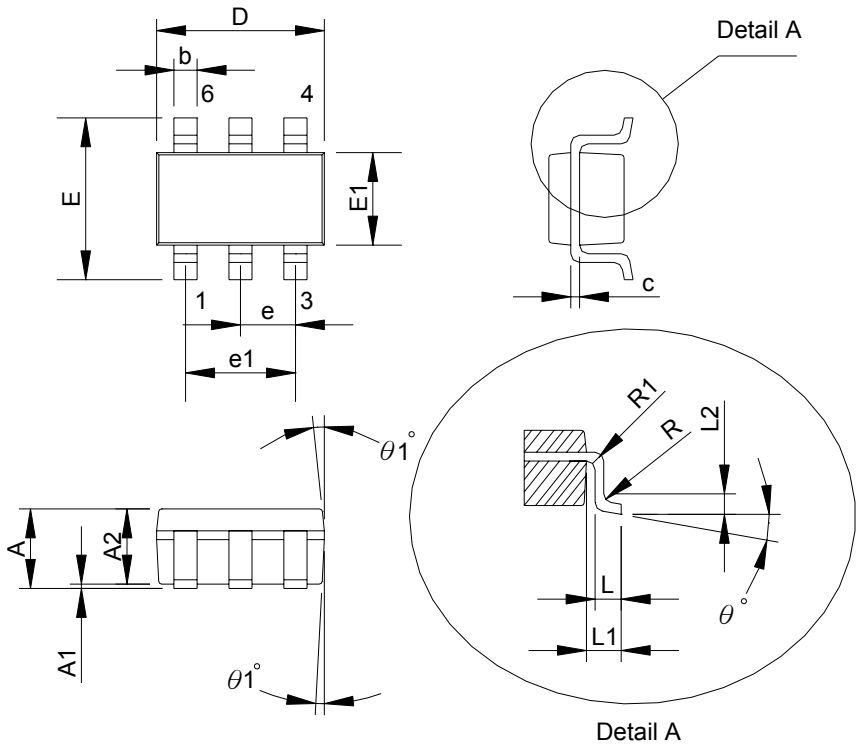
8 PINS - DIP (D)



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
e_B	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

6PINS - SOT (T)



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1			0.15			0.006
A2	0.90	1.15	1.30	0.036	0.045	0.051
b	0.30		0.50	0.011		0.020
c	0.08		0.22	0.003		0.009
D		2.90			0.114	
E		2.80			0.110	
E1		1.60			0.063	
e		0.95			0.037	
e1		1.90			0.075	
L	0.30	0.45	0.60	0.020	0.018	0.024
L1		0.60			0.024	
L2		0.25			0.010	
R	0.10			0.004		
R1	0.10		0.25	0.004		0.010
θ°	0°	4°	8°	0°	4°	8°
θ1°	5°	10°	15°	5°	10°	15°

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