Low Cost Green-Mode PWM Controller for Flyback Converters **SG6859**

FEATURES

- Green-Mode PWM
- Supports the "Blue Angel" Standard
- Low Start-up Current (9uA)
- Low Operating Current (3mA)
- Leading-Edge Blanking
- Constant Output Power Limit
- Universal Input
- Built-in Synchronized Slope Compensation
- Current Mode Operation
- Cycle-by-cycle Current Limiting
- Under Voltage Lockout (UVLO)
- Programmable PWM Frequency with Frequency Hopping
- V_{DD} Over Voltage Protection (Auto Restart)
- Gate Output Voltage Clamped at 17V
- Low Cost
- Few External Components Required
- Small SOT-26 and Dip 8 Packages

APPLICATIONS

General-purpose switching mode power supplies and flyback power converters, such as

- Battery chargers for cellular phones, cordless phones, PDAs, digital cameras, and power tools
- Power adapters for ink jet printers, video game consoles, and portable audio players
- Open-frame SMPS for TV/DVD standby and other auxiliary supplies, home appliances, and consumer electronics
- Replacements for linear transformers and RCC SMPS
- PC 5V standby power.

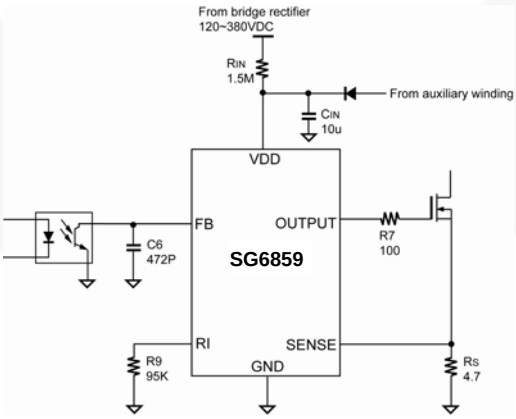
DESCRIPTION

This highly integrated PWM controller provides several special enhancements designed to meet the low standby-power needs of low-power SMPS. To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. This green-mode function enables the power supply to easily meet even the strictest power conservation requirements.

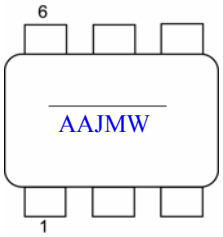
The BiCMOS fabrication process enables reducing the start-up current to 9uA, and the operating current to 3mA. To further improve power conservation, a large start-up resistance can be used. Built-in synchronized slope compensation ensures the stability of peak current mode control. Proprietary internal compensation provides a constant output power limit over a universal AC input range ($90V_{AC}$ to $264V_{AC}$). Pulse-by-pulse current limiting ensures safe operation even during short-circuits.

To protect the external power MOSFET from being damaged by supply over voltage, the SG6859's output driver is clamped at 17V. SG6859 controllers can be used to improve the performance and reduce the production cost of power supplies. The SG6859 is the best choice for replacing linear and RCC-mode power adapters. It is available in 8-pin DIP and 6-pin SOT-26 packages.

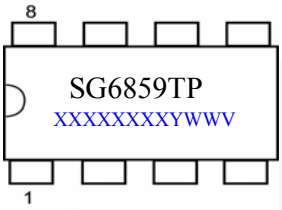
TYPICAL APPLICATION



MARKING DIAGRAMS



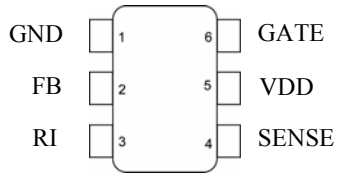
AAJ: SG6859
M: Mask Version
W: Week code A~Z=W1~W26
A~Z=W27~W52
—— : Lead Free Package



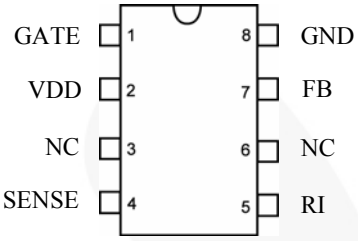
T: D=DIP
P: Z =Lead Free
Null=Regular Package
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION

SOT-26



DIP-8



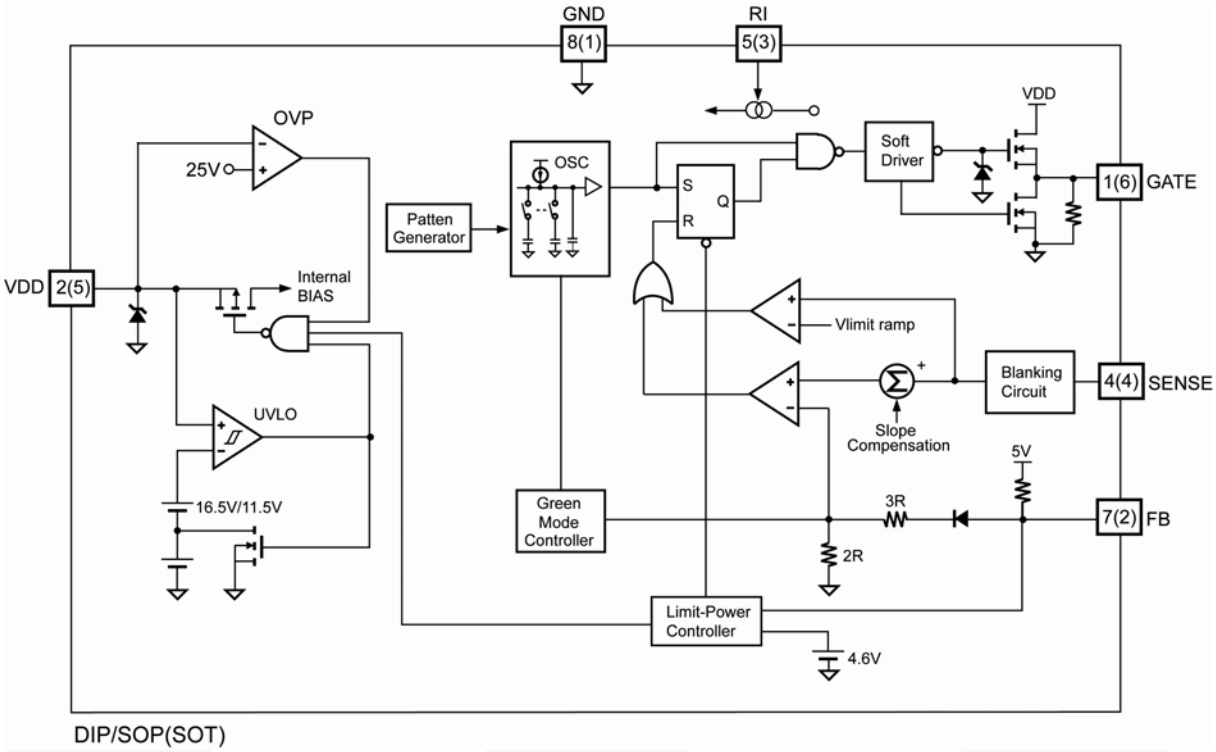
ORDERING INFORMATION

Part Number	Pb-Free	Package
SG6859TZ		6-Pin SOT-26
SG6859DZ		8-Pin DIP-8

PIN DESCRIPTIONS

Name	Pin No. DIP-8(SOT-26)	Type	Function
GATE	1 / (6)	Driver Output	The totem-pole output driver for driving the power MOSFET.
VDD	2 / (5)	Supply	Power supply.
NC	3		NC pin.
SENSE	4 / (4)	Analog Input	Current sense. This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled. This activates over-current protection. This pin also provides current amplitude information for current-mode control.
RI	5 / (3)	Analog Input/Output	A resistor connected from the RI pin to ground will generate a constant current source for the SG6859. This current is used to charge an internal capacitor, to determine the switching frequency. Increasing the resistance will reduce the amplitude of the current source and reduce the switching frequency. A 95kΩ resistor R_i results in a 50uA constant current I_i and a 70kHz switching frequency.
NC	6		NC pin.
FB	7 / (2)	Analog Input	Feedback. The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator, so that the PWM comparator can control the duty cycle.
GND	8 / (1)	Supply	Ground.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_{VDD}	DC Supply Voltage *	30		V
V_{FB}	Input Voltage to FB Pin	-0.3 to 7		V
V_{SENCE}	Input Voltage to Sense Pin	-0.3 to 7		V
T_J	Operating Junction Temperature	150		°C
$R_{\theta JA}$	Thermal Resistance (Junction to Air)	SOT	208.4	°C/W
		DIP	82.5	°C/W
T_{STG}	Storage Temperature Range	-55 to +150		°C
T_L	Lead Temperature (Wave soldering or IR, 10 seconds)	260		°C
$V_{ESD-HBM}$	ESD Capability, HBM Model	3.5		kV
V_{ESD-MM}	ESD Capability, Machine Model	200		V

* All voltage values, except differential voltages, are given with respect to GND pin.

* Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	≦22	V
T_A	Operating Ambient Temperature	-20 to +85	°C

* For proper operation.

ELECTRICAL CHARACTERISTICS (V_{DD} = 15V; T_A = 25°C)

VDD Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD-OP}	Continuously Operation Voltage				22	V
V_{DD-ON}	Turn-On Threshold Voltage		15.5	16.5	17.5	V
V_{DD-OFF}	Turn-Off Threshold Voltage		10.5	11.5	12.5	V
I_{DD-ST}	Startup Current	$V_{DD}=V_{DD-ON}$ – 0.1V		9	15	μA
I_{DD-OP}	Operating Supply Current	V_{DD}=15V, GATE with 1nF to GND		3	3.5	mA
V_{DD-OVP}	VDD Over-voltage-protection level	(Auto Restart)	24	25	26	V
$t_{D-VDDOVP}$	VDD Over-voltage-protection Debounce	(Auto Restart)		125		μs
$V_{DD-G\ OFF}$	V_{DD} Low-threshold Voltage to Exit Green-off Mode			V_{DD-OFF} + 1		V

Feedback Input Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_{FB}	Input Impedance			5		KΩ
$V_{FB-OPEN}$	FB Output High Voltage		5			V
V_{FB-OL}	FB Open-loop Trigger Level		4.3	4.6	4.9	V
t_{D-OLP}	The delay time of FB pin Open Loop Protection			56		ms
V_{FB-N}	Green-Mode Entry FB Voltage		2.6	2.85	3.1	V
V_{FB-G}	Green-Mode Ending FB Voltage			2.20		V
S_G	Green-Mode Modulation Slope	R_I=95KΩ	40	75	100	Hz/mV

Current Sense Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_{SENSE}	Input Impedance		10			KΩ
t_{PD}	Delay to Output		40	55	100	ns
V_{STHFL}	Flat Threshold Voltage for Current Limit		0.91	0.96	1.01	V
V_{STHVA}	Valley Threshold Voltage for Current Limit		0.75	0.80	0.85	V
t_{LEB}	Leading-Edge Blanking Time		250	300	350	ns
DCY_{SAW}	Duty Cycle of SAW Limit			40		%

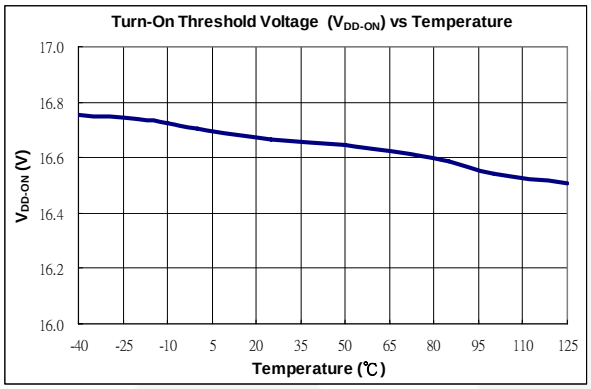
Oscillator Section

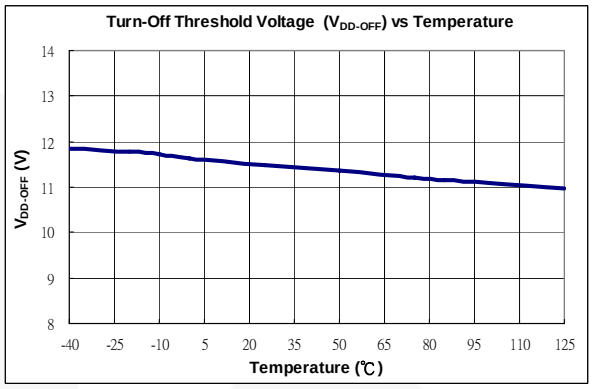
Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
F_{OSC}	Normal PWM Frequency	Center Frequency	R_I=95KΩ	65	70	75	KHz
		Hopping Range			±4.9		
T_{HOP}	Hopping Period		R_I=95KΩ		3.7		ms
F_{OSC-G}	Green-Mode Frequency		R_I=95KΩ		22		KHz
F_{DV}	Frequency Variation versus V_{DD} Deviation		V_{DD}=13.5 to 22V	0	0.02	2	%
F_{DT}	Frequency Variation versus Temp. Deviation		T_A=-20 to 85°C			2	%

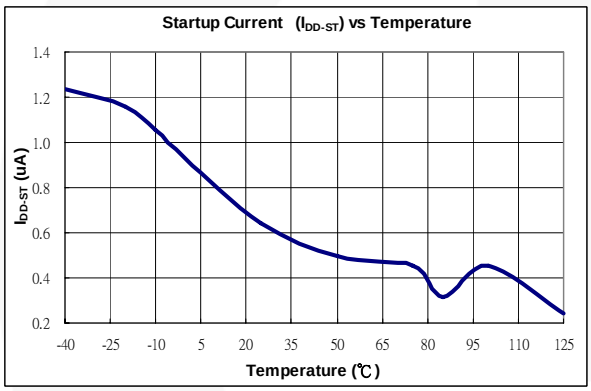
Output Section

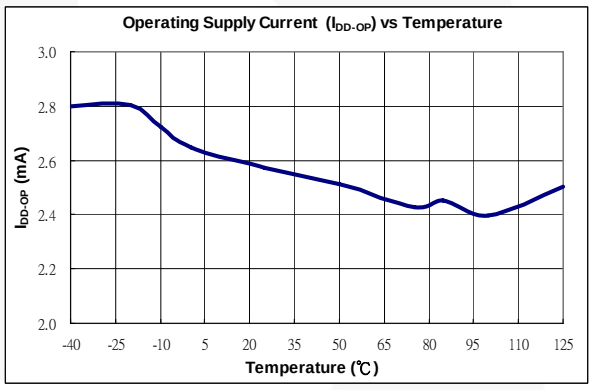
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DCY_{MAX}	Maximum Duty Cycle		70	75	80	%
V_{GATE-L}	Output Voltage Low	V_{DD}=15V, I_o=20mA			1.5	V
V_{GATE-H}	Output Voltage High	V_{DD}=13.5V, I_o=20mA	8			V
tr	Rising Time	V_{DD}=15V, C_L=1nF		150		ns
tf	Falling Time	V_{DD}=15V, C_L=1nF		55		ns
$V_{GATE-CLAMP}$	Output Clamp Voltage	V_{DD}=22V	16	17	18	V

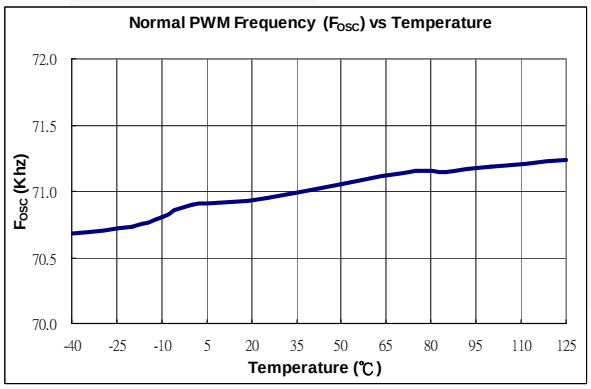
TYPICAL CHARACTERISTICS

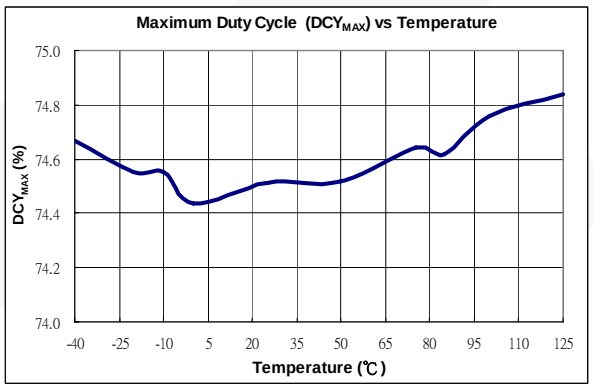


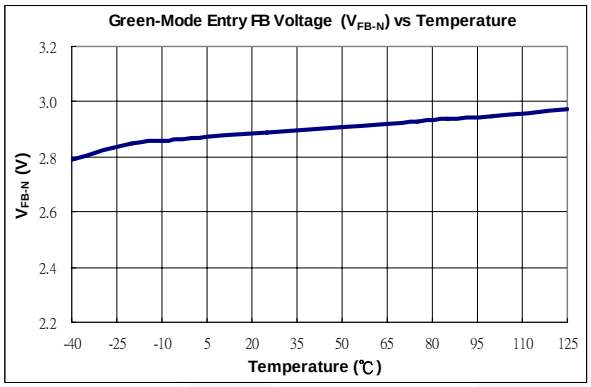


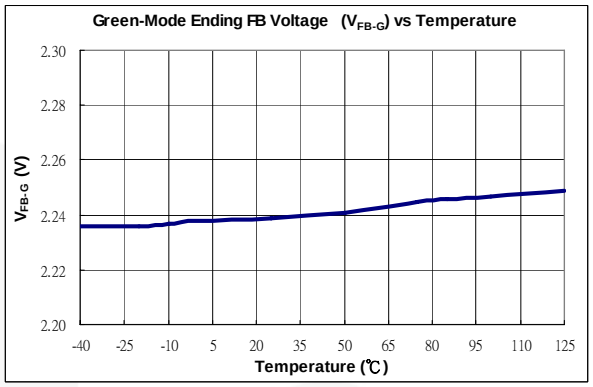


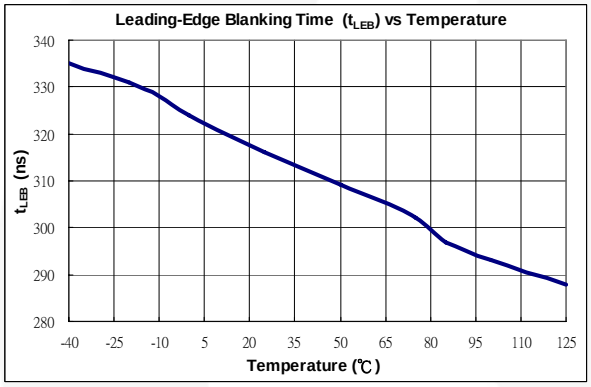


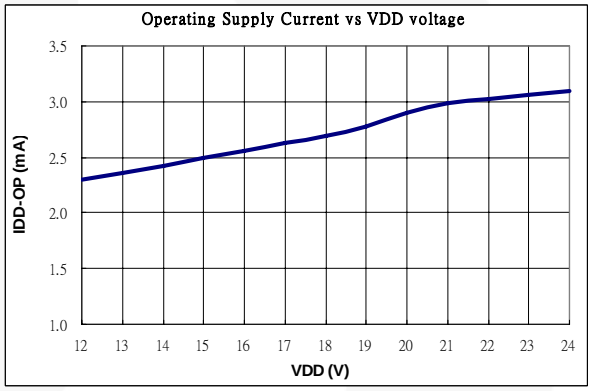





Green-Mode Entry FB Voltage (V_{FB-N}) vs Temperature
V_{FB-N} (V)
3.2
3.0
2.8
2.6
2.4
2.2
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Green-Mode Ending FB Voltage (V_{FB-G}) vs Temperature
V_{FB-G} (V)
2.30
2.28
2.26
2.24
2.22
2.20
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Leading-Edge Blanking Time (t_{LEB}) vs Temperature
t_{LEB} (ns)
340
330
320
310
300
290
280
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Operating Supply Current vs VDD voltage
IDD-OP (mA)
3.5
3.0
2.5
2.0
1.5
1.0
12 13 14 15 16 17 18 19 20 21 22 23 24
VDD (V)

OPERATION DESCRIPTION

SG6859 devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the SG6859 series.

Start-up Current

The start-up current is only 9uA. Low start-up current allows a start-up resistor with a high resistance and a low-wattage to supply the start-up power for the controller. A 1.5 MΩ, 0.25W, start-up resistor and a 10uF/25V V_{DD} hold-up capacitor would be sufficient for an AC-to-DC power adapter with a wide input range ($100V_{AC}$ to $240V_{AC}$).

Operating Current

The operating current has been reduced to 3mA. The low operating current results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. On-time is limited to provide stronger protection against brownouts and other abnormal conditions. The feedback current, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback current exceeds the threshold current, the switching frequency starts to decrease. This green-mode function dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using the SG6859 can easily meet even the strictest regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to ground will generate a constant current source for the SG6859. This current is used to charge an internal capacitor. The charge-time determines the internal clock speed and the switching frequency. Increasing the resistance will reduce the amplitude of the input current and reduce the switching frequency. A 95kΩ resistor R_i results in a 50uA constant current I_i and a 70kHz switching frequency. The relationship between R_i and the switching frequency is:

$$f_{PWM} = \frac{6650}{R_I\,(k\Omega)}\,(kHz)$$

Leading-Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a 320nsec leading edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Constant Output Power Limit

When the SENSE voltage across the sense resistor R_s reaches the threshold voltage (around 0.96V), the output GATE drive will be turned off following a short propagation delay t_{PD}.

This propagation delay will introduce an additional current proportional to $t_{PD}*V_{in}/L_p$. The propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltages will result in larger additional currents. At high input line voltages, the output power limit will be higher than at low input line voltages.

To compensate for this output power limit variation across a wide AC input range, the threshold voltage is adjusted by adding a positive ramp.

This ramp signal rises from 0.80V to 0.96V, and then flattens out at 0.96V. A smaller threshold voltage forces the output GATE drive to terminate earlier.

This reduces the total PWM turn-on time and makes the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for a wide AC input voltage range (90VAC to 264VAC).

Under Voltage Lockout (UVLO)

The turn-on and turn-off thresholds of the SG6859 are fixed internally at 16.5V/11.5V. During start-up, the hold-up capacitor must be charged to 16.5V through the start-up resistor, so that the SG6859 will be enabled. The hold-up capacitor will continue to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 11.5V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor will be adequate to supply V_{DD} during start-up.

Gate Output

The SG6859 BiCMOS output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 17V Zener diode in order to protect power MOSFET transistors against undesired over-voltage gate signals.

Built-in Slope Compensation

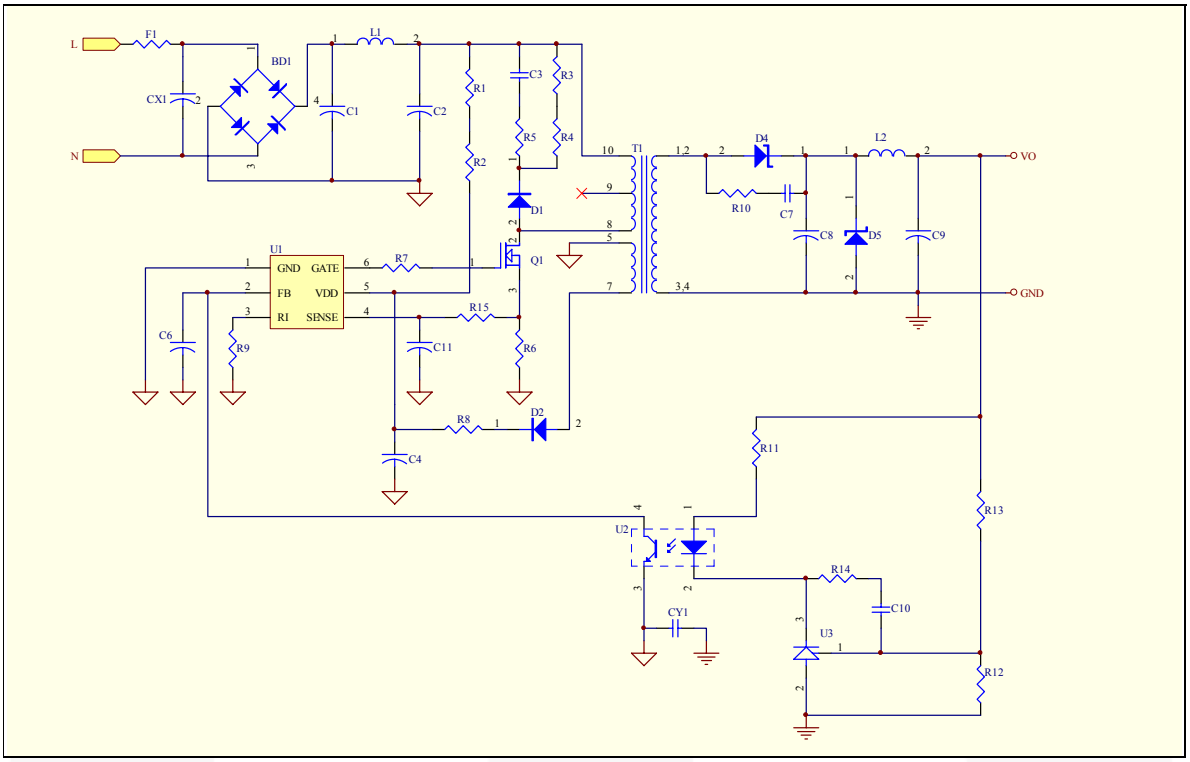
The sensed voltage across the current sense resistor is used for current mode control and pulse-by-pulse current limiting. Built-in slope compensation will improve stability and prevent sub-harmonic oscillations due to peak-current mode control. The SG6859 has a synchronized, positively-sloped ramp built-in at each switching cycle. The slope of the ramp is:

$$\frac{0.36 \times Duty}{Duty(\max.)}$$

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse width jitter, particularly in continuous-conduction mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the SG6859, and increasing the power MOS gate resistance is advised.

REFERENCE CIRCUIT

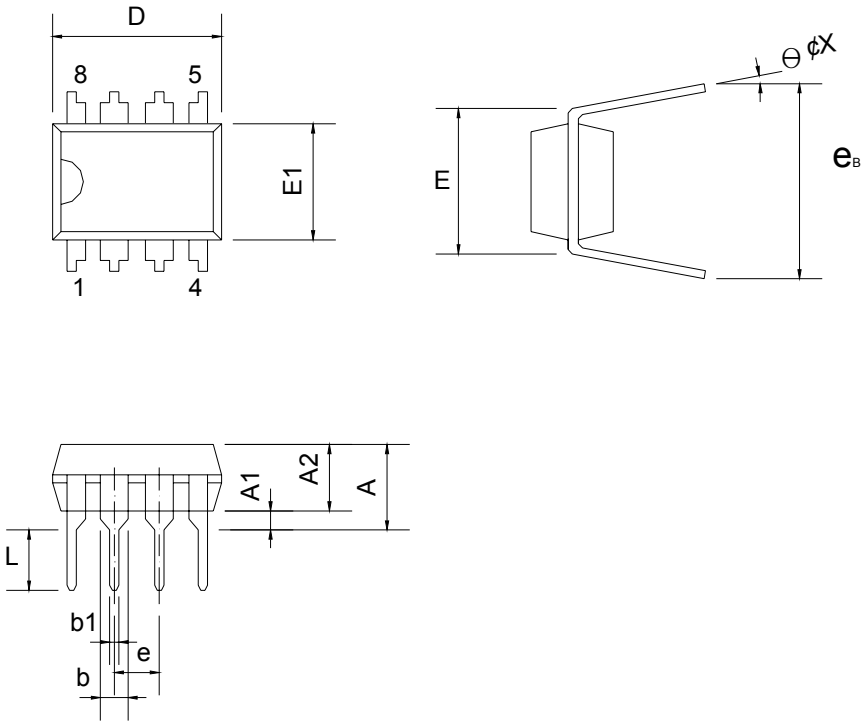


BOM

Reference	Component	Reference	Component
BD1	BD 1A/500V	L2	10uH 6mm
CX1 (Optional)	XC 0.1uF	Q1	MOSFET 1A/600V
CY1 (Optional)	YC 102P/400V (Y1)	R1,R2	R 750KΩ 1206
C1	CC 103P/500V	R3,R4	R 47KΩ 1206
C2	EC 10μF/400V 105°C	R5	R 47Ω 1206
C3	CC 102P/500V	R6	R 4.7Ω 1206
C4	EC 10μ/50V	R7	R 100Ω 0805
C6	CC 472P 0805	R8	R 10Ω 1206
C7 (Optional)	CC 102P/100V 1206	R9	R 100KΩ 0805
C8	EC 470μ/10V 105°C	R10 (Optional)	R 10Ω 1206
C9	EC 220μ/10V 105°C	R11	R 100Ω 1/8W
C10	CC 222P 0805	R12	R 33KΩ 0805
C11	N.C.	R13	R 33KΩ 1/8W
D1	Diode FRI07	R14	R 4.7KΩ 0805
D2	Diode FR102	R15	R 0Ω 0805
D4	Diode SB360	T1	EE-16
D5 (Optional)	ZD 6.8V 0.5W	U1	IC SG6859
F1	R 1Ω/0.5W	U2	PC817
L1	20mH 6*8mm	U3	TL431

PACKAGE INFORMATION

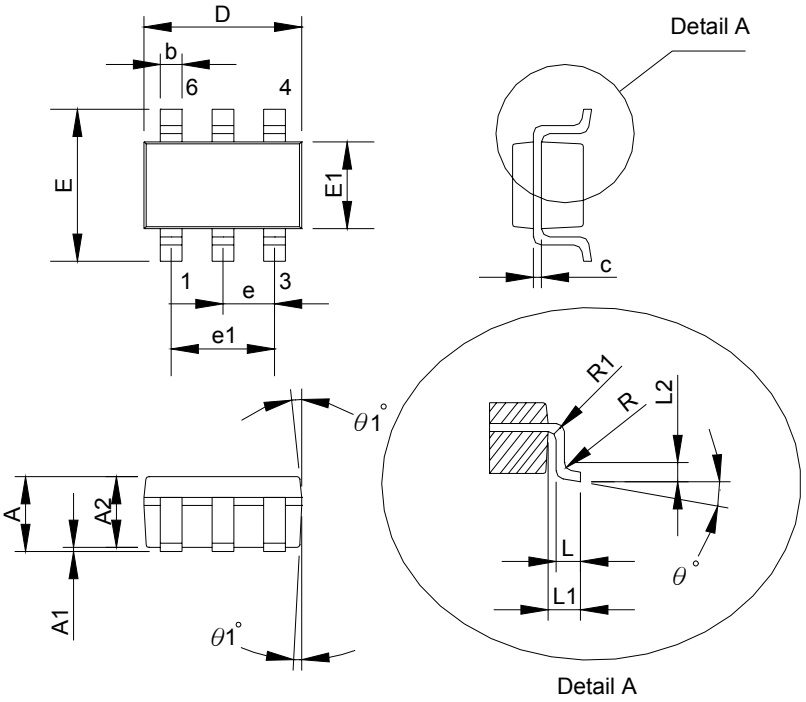
8 PINS - DIP (D)



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
e_B	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

6 PINS - SOT (T)



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1			0.15			0.006
A2	0.90	1.15	1.30	0.036	0.045	0.051
b	0.30		0.50	0.011		0.020
c	0.08		0.22	0.003		0.009
D		2.90			0.114	
E		2.80			0.110	
E1		1.60			0.063	
e		0.95			0.037	
e1		1.90			0.075	
L	0.30	0.45	0.60	0.020	0.018	0.024
L1		0.60			0.024	
L2		0.25			0.010	
R	0.10			0.004		
R1	0.10		0.25	0.004		0.010
θ°	0°	4°	8°	0°	4°	8°
θ1°	5°	10°	15°	5°	10°	15°

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Green FPS™ e-Series™
GTO™
i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
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Power220®
Power247®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
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QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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