DATA SHEET

SA57000-XX

CapFREE™ 150 mA, low-noise, low dropout regulator with thermal protection

Product data
Supersedes data of 2003 Apr 30

2003 Jul 30

Philips
Semiconductors

PHILIPS

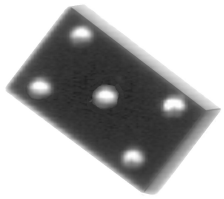
CapFREE™ 150 mA, low-noise, low dropout regulator with thermal protection

SA57000-XX

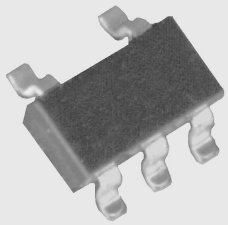
GENERAL DESCRIPTION

The CapFREE™ SA57000 is the first in a new family of unique low dropout regulators. It needs no external capacitors, offers a low output noise voltage of 30 μV_{RMS}, and an ultra-low dropout voltage of 55 mV @ 50 mA output current. To accommodate high density layouts, it is packaged in the small footprint 5 leaded SOT23-5 (SO5) and a 5-bump Wafer Level Chip-Scale package (WL-CSP5). It is ideal for all portable and cellular phone applications.

Additional features include power and thermal shutdown, output current limitation, power OK status, thermal warning, and external logic-controlled on-off via the PWRON pin.



WL-CSP5



SOT23-5

FEATURES

- CapFREE: No output capacitor needed, stable for all capacitive loads, regardless of ESR
- 5 leaded SOT23-5 (SO5) and Wafer Level Chip-Scale (WL-CSP5) packages
- Low 30 μV_{RMS} noise without noise bypass capacitor
- Preset output voltages to 2.5 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 3.3 V and 3.6 V; other voltages available upon request. 2% output voltage accuracy
- 150 mA maximum output current with current limitation
- Typical dropout voltage 55 mV @ 50 mA output current
- 85 µA typical ground current
- Shut-down (standby) current < 1 µA
- Thermal-overload and short-circuit protection
- PWROK pin: both power status and thermal warning indicator
- PWRON pin offers logic-controlled shutdown
- Maximum line regulation: 0.1%/V
- Maximum load regulation: 0.02%/mA.

APPLICATIONS

- Cordless and mobile phones
- Industrial and medical equipment
- Other battery-powered equipment.

SIMPLIFIED SYSTEM DIAGRAM

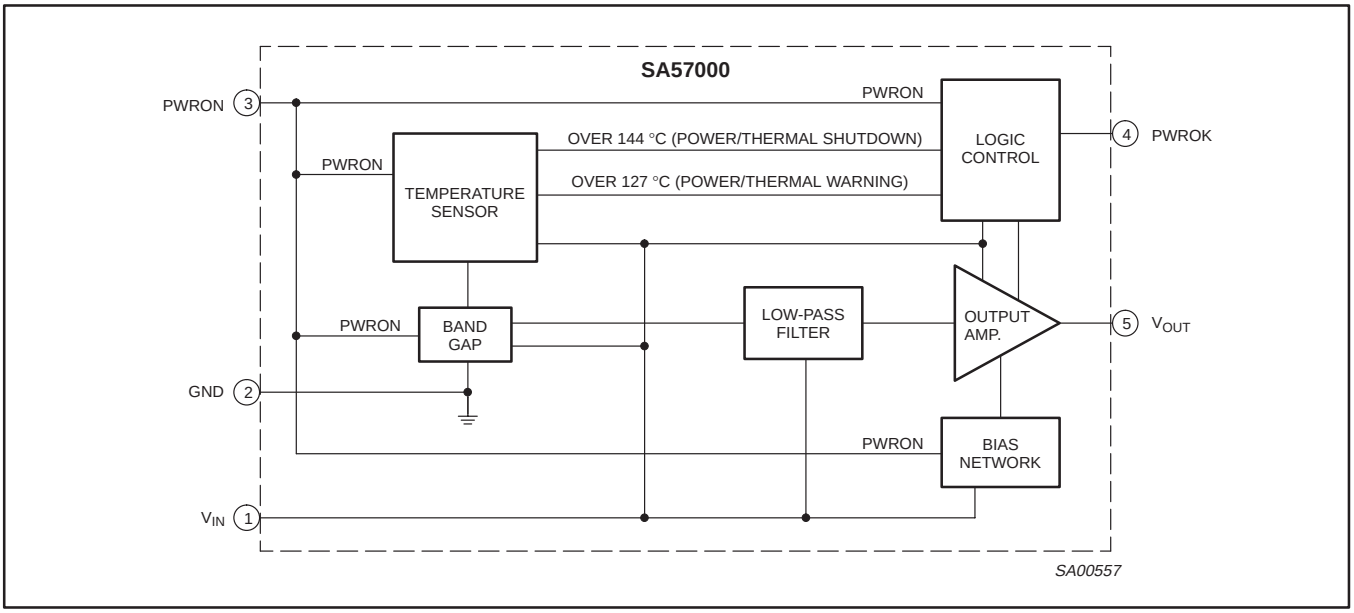


Figure 1. Simplified system diagram.

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE
	NAME	DESCRIPTION	VERSION	
SA57000-**XX**D	SOT23-5, SO5	plastic small outline package; 5 leads (see dimensional drawing)	SOT680-1	–40 to +85 °C
SA57000-**XX**UK	WL-CSP5	wafer level, chip-scale package; 5 bumps (see dimensional drawing)		–40 to +85 °C

NOTE:
The device has seven voltage output options, indicated by the **XX** on the Type Number.

XX	VOLTAGE (Typical)
25	2.5 V
28	2.8 V
29	2.9 V
30	3.0 V
31	3.1 V
33	3.3 V
36	3.6 V

Marking code

Each device is marked with a four letter code. The first three letters designate the product. The fourth, represented by an 'x', designates the date tracking code.

Part	Marking
SA57000-25UK, SA57000-25D	ABKx
SA57000-28UK, SA57000-28D	ABLx
SA57000-29UK, SA57000-29D	ABXx
SA57000-30UK, SA57000-30D	ABMx
SA57000-31UK, SA57000-31D	ABYx
SA57000-33UK, SA57000-33D	ABNx
SA57000-36UK, SA57000-36D	ABPx

PIN CONFIGURATION

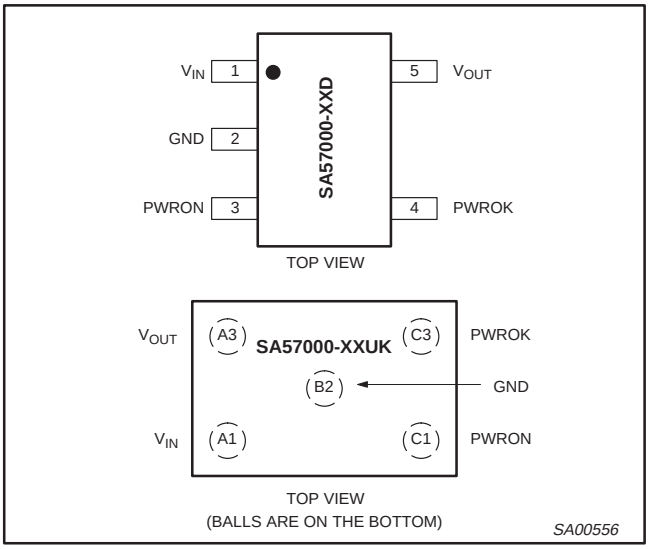


Figure 2. Pin configurations.

PIN DESCRIPTION

PIN	BALL	SYMBOL	DESCRIPTION
1	A1	V_{IN}	Regulator input. $V_{OUT(nom)}$ + 0.5 V to 6.5 V. No bypass capacitor required.
2	B2	GND	Ground.
3	C1	PWRON	Power-on input. Active-HIGH. A logic LOW powers down the regulator. The shutdown quiescent current is typically 50 nA. Connect to V_{IN} for manual operation.
4	C3	PWROK	Power OK indicator, including thermal warning. Connect a 10 kΩ resistor between PWROK and V_{OUT}. Active-LOW open-drain output indicates an out-of-regulation condition when power falls typically 6% below VOUT(nom), or thermal warning (trips at 127 °C ± 2 °C).
5	A3	V_{OUT}	Regulator output. Sources up to 150 mA. No bypass capacitors required.

MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{IN}	V_{IN} to GND voltage		–0.3	6.5	V_{DC}
V_{PWRON}	PWRON to GND voltage		–0.3	6.5	V_{DC}
V_{OUT}	OUT to GND voltage		–0.3	V_{IN} + 0.3	V_{DC}
T_{amb}	Operating ambient temperature		–40	+85	°C
T_j	Junction temperature		–	+125	°C
T_{stg}	Storage temperature		–65	+160	°C
P	Power dissipation (Derating factor above 25 °C)	T_{amb} = 25 °C	–	637	mW
$R_{th(j-a)}$	Thermal resistance from junction to ambient		–	140	°C/W

CHARACTERISTICS

$V_{IN} = V_{OUT(nom)} + 0.5$ V. (Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IN}	input voltage		$V_{OUT(nom)}$	–	6.5	V
	output voltage accuracy [2]	I_{OUT} = 1 mA T_{amb} = +25 °C –40 °C ≤ T_{amb} ≤ +85 °C	 – –2.0	 ±1 –	 – 2.0	 % %
I_{LIM}	current limit		160	300	–	mA
I_Q	ground pin current	I_{OUT} = 1 mA to 150 mA	–	85	150	µA
	dropout voltage [3]	I_{OUT} = 1 mA	–	1	–	mV
		I_{OUT} = 50 mA	–	55	120	mV
		I_{OUT} = 150 mA	–	165	–	mV
ΔV_{LNR}	line regulation	V_{IN} = (V_{OUT} + 0.1 V) to 5.5 V; I_{OUT} = 20 mA	–	–	0.1	%/V
ΔV_{LDR}	load regulation	I_{OUT} = 1 mA to 150 mA	–	0.01	0.02	%/mA
e_n	output voltage noise	f = 10 Hz to 100 kHz, C_{OUT} = 10 µF	–	30	–	μV_{RMS}
Shutdown						
V_{IH}	PWRON input threshold (HIGH ON-state)	$V_{IN} \rightarrow V_{OUT(nom)} \rightarrow 6.5$ V	$0.7 \times V_{IN}$	–	–	V
V_{IL}	PWRON input threshold (HIGH ON-state)	$V_{IN} \rightarrow V_{OUT(nom)} \rightarrow 6.5$ V	–	–	$0.3 \times V_{IN}$	V
I_{PWRON}	PWRON input bias current	$V_{PWRON} = V_{IN}$ T_{amb} = +25 °C T_{amb} = +85 °C	 – –	 0.01 0.05	 1 –	 µA µA
$I_{Q(SHDN)}$	shutdown supply current	V_{OUT} = 0 V T_{amb} = +25 °C T_{amb} = +85 °C	 – –	 0.05 0.2	 1 1	 µA µA
t_{PWRON}	power-on start-up time [4]	I_{OUT} = 1 mA, C_{OUT} = 100 nF T_{amb} = +25 °C T_{amb} = –40 to +85 °C	 – –	 25 35	 100 200	 µs µs
Thermal protection (Note 2)						
T_{SHDN}	thermal shut-down temperature		–	144	–	°C
ΔT_{SHDN}	thermal shut-down hysteresis		–	13	–	°C
PWROK output (power and temperature OK) (Note 2)						
	PWROK trip temperature		–	127	–	°C
	PWROK trip temperature hysteresis		–	12	–	°C
	PWROK trip as percentage of $V_{OUT(nom)}$		–3.5	–6	–8	%
	PWROK hysteresis as percentage of $V_{OUT(nom)}$		–	2	–	%
	PWROK output (when tripped)	I_{SINK} = 0.5 mA	–	0.1	0.4	V

NOTES:

1. Limits are production tested at T_{amb} = +25 °C. All devices are 100% production tested at 25 °C. Limits over the operating tempreature are guaranteed by design.
2. Accuracy ±2 °C over temperature range guaranteed by design and characterization.
3. The dropout voltage is defined as $V_{IN} - V_{OUT}$, where V_{OUT} is 100 mV below the value of V_{OUT} for $V_{IN} = V_{OUT} + 0.5$ V.
4. Time needed for V_{OUT} to reach 95% of $V_{OUT(nom)}$.

TYPCIAL PERFORMANCE CURVES

Measurements taken with the SA57000-33 (3.3 volt output).

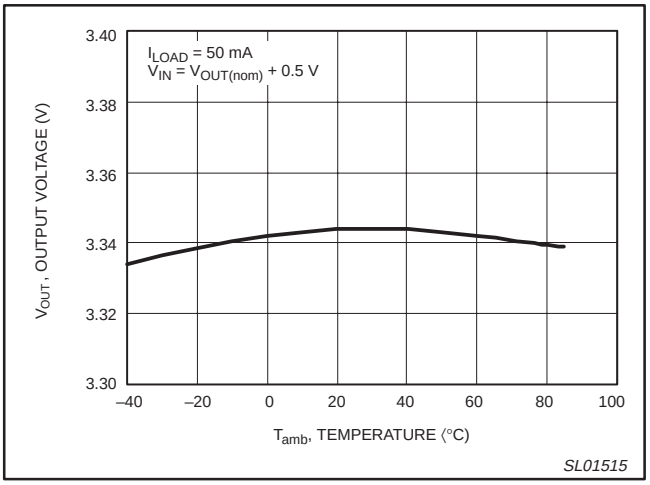


Figure 3. Output voltage versus temperature.

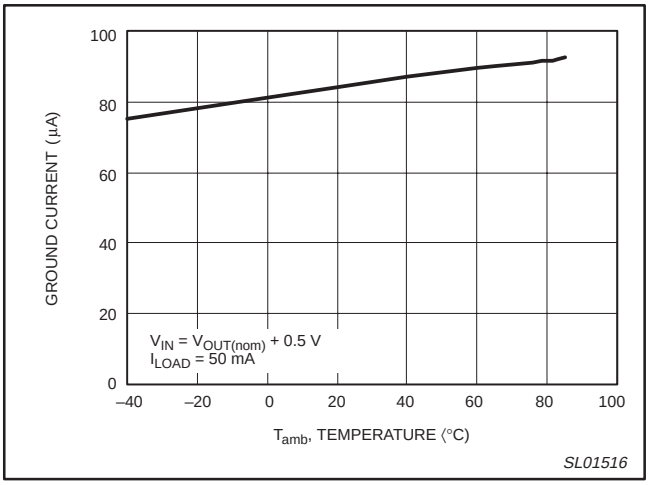


Figure 4. Ground current versus temperature.

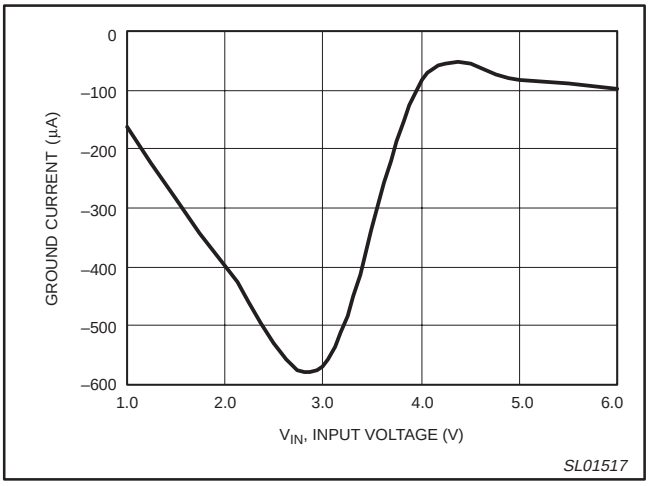


Figure 5. Ground current versus input voltage (no load).

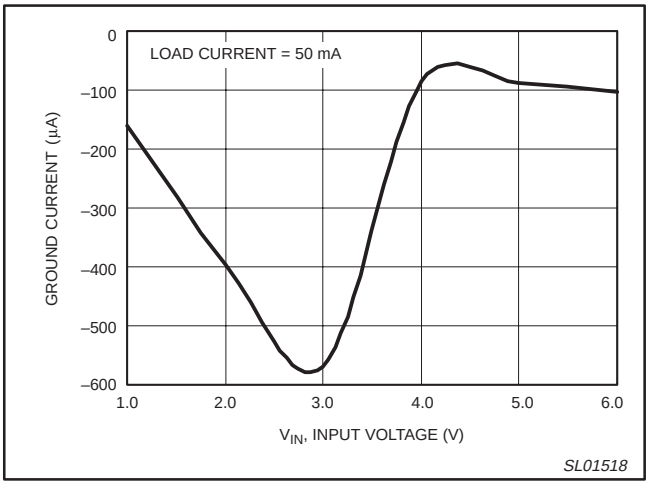


Figure 6. Ground current versus input voltage with load.

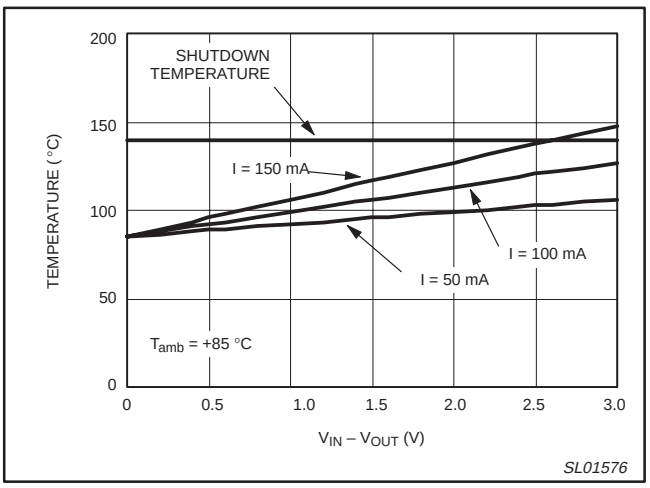


Figure 7. T_j versus $V_{IN} - V_{OUT}$ for 3 output currents.

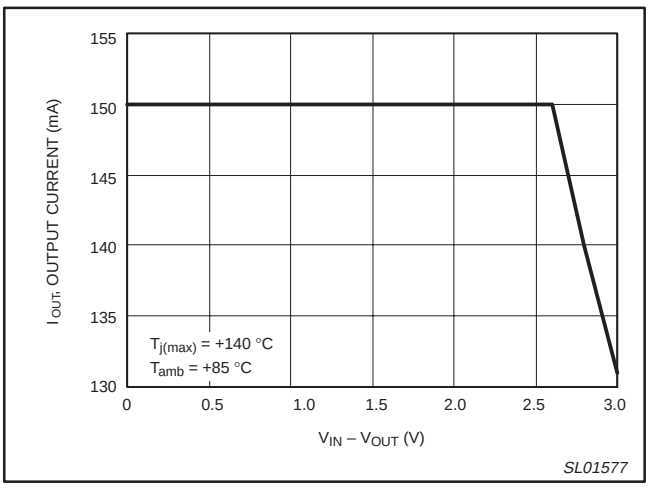


Figure 8. Maximum I_{OUT} versus $V_{IN} - V_{OUT}$.

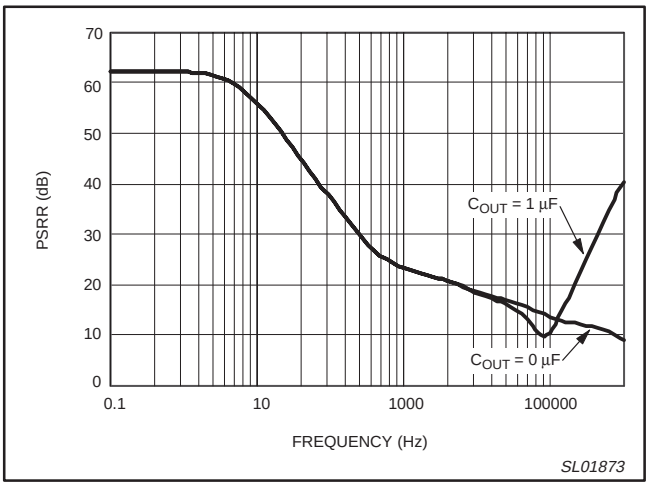


Figure 9. Power supply rejection ratio versus frequency.

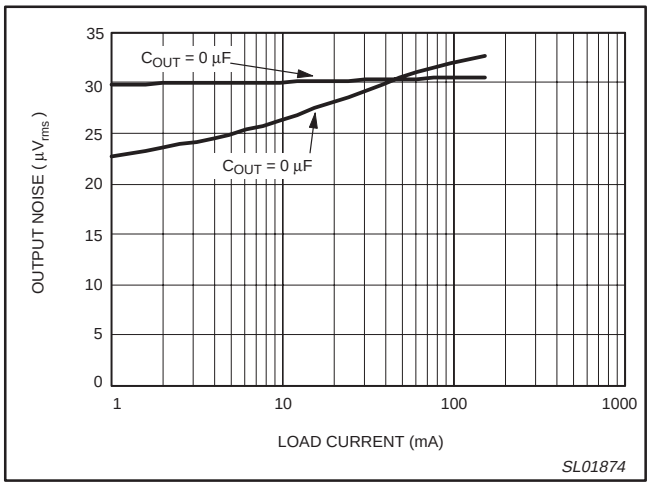


Figure 10. Output noise versus load current.

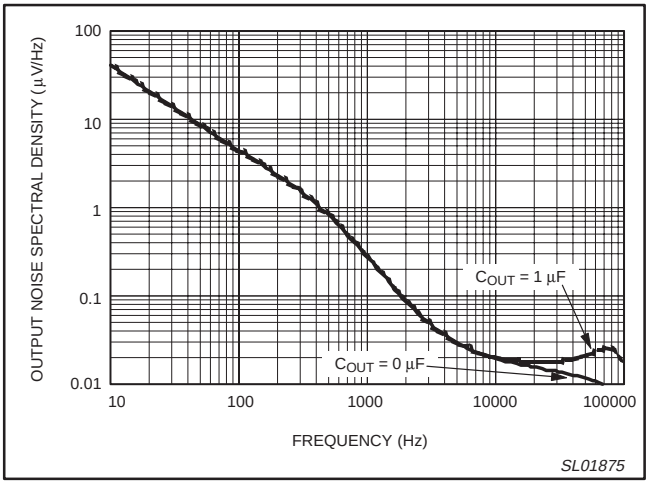


Figure 11. Output noise spectral density versus frequency.

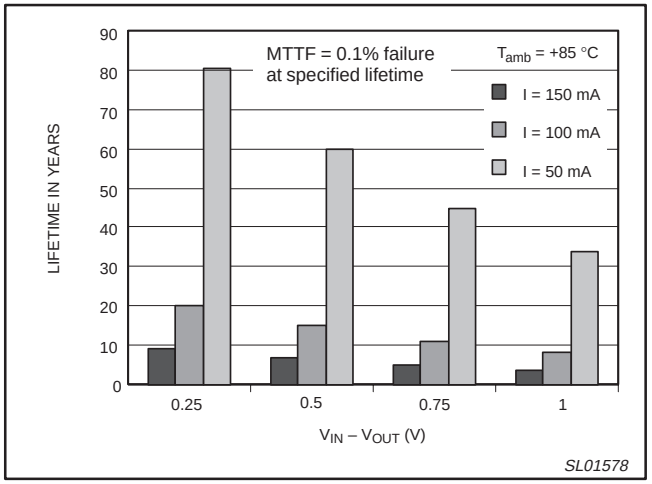


Figure 12. Lifetime versus V_{IN} – V_{OUT} for 3 output currents.

TECHNICAL DESCRIPTION

General discussion

The SA57000-XX is a low dropout, low-quiescent current linear regulator designed primarily for battery-powered applications and stabilizes with or without input/output capacitors. The device delivers up to 150 mA and is available with preset output voltages of 2.5 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 3.3 V, and 3.6 V for both SOT 23-5 and WL-CSP packages.

The 1.23 band-gap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, which allows more current to pass to the output. The output voltage is fed back through an internal resistor voltage divider connected to the V_{OUT} pin.

Band-gap

The band-gap circuitry generates a temperature independent voltage by properly adding two voltages with negative and positive temperature coefficient. The band-gap voltage is typically 1.23 volts with a temperature variation of 5 mV over the temperature range from –40 °C to +125 °C.

Low-pass filter

Low-pass filter is basically an RC filter with a low cut-off frequency. **No external capacitor is used**. There is one comparator, which turns on the bypass paths to charge or discharge the capacitor if the output of the filter is higher or lower than the band-gap voltage by a specified amount.

Output amplifier

The output amplifier is a folded-cascode PMOS amplifier which controls the gate of the output transistor and sources the load current. A portion of the output voltage is compared to the reference voltage and a constant voltage is maintained at output. The output is also monitored by a comparator which trips PWROK if the output voltage falls below the nominal output level by a specified amount due to low battery condition or any other reason. The current limiter circuit monitors the output current and limits the load current to a certain value to avoid any damage due to short circuit.

Bias circuit

The bias block provides bias currents and voltages for the other blocks. It has a self start-up circuit and it can establish the bias currents and voltages very fast.

Temperature sensor

The temperature sensor block monitors the die temperature and flags PWROK when the temperature crosses 125 °C. If the die temperature goes beyond 144 °C typical value, the output amplifier is shut down. Both the temperatures corresponding to Power-OK or shutdown have a hysteresis of 13 °C.

ESD protection

The standard ESD blocks protect the CMOS circuit against electrostatic discharge (ESD).

PRWROK output

PWROK goes LOW when the output voltage goes out of regulation as during drop-out, current limit or thermal shutdown. PowerOK is an open-drain N-channel MOSFET. To obtain a logic-level output, connect a 10 kΩ pull-up resistor from PWROK pin to V_{OUT} pin. To minimize current consumption, make this resistor as large as practical. A 100 kΩ resistor works well for most applications. The PowerOK is not active during shutdown.

Current limit

The SA57000-XX includes a current limiter that monitors and controls the pass transistor's gate voltage, limiting the output current to 300 mA typical value. For design purposes, consider the current limit to be 160 mA minimum value. The output can be shorted to ground for an indefinite period of time without damaging the part.

Thermal-overload protection

When the junction temperature exceeds T_j = 144 °C typical value, the thermal sensor signals the shutdown logic, turning off the output amplifier and allowing the die to cool. The thermal sensor will turn the output amplifier on again after the die's junction temperature decreases by 13 °C hysteresis value, resulting in a pulsed output during continuous thermal overload conditions.

TIMING DIAGRAM

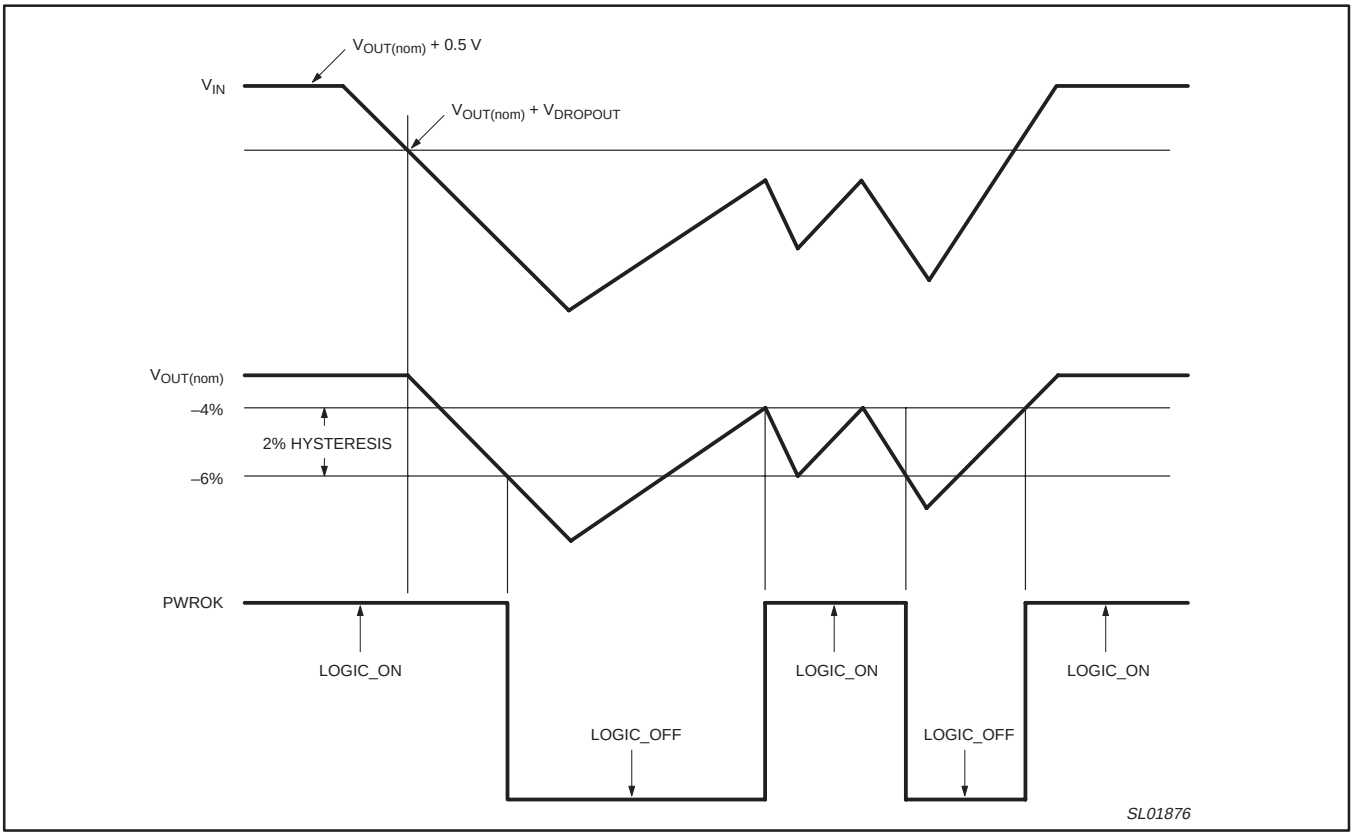
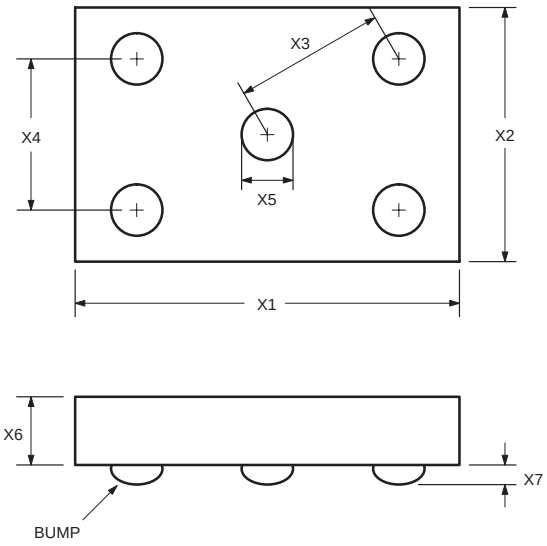


Figure 13. Timing diagram.

WL-CSP5: wafer level, chip-scale package; 5 bumps



DIMENSIONS (mm are the original dimensions)

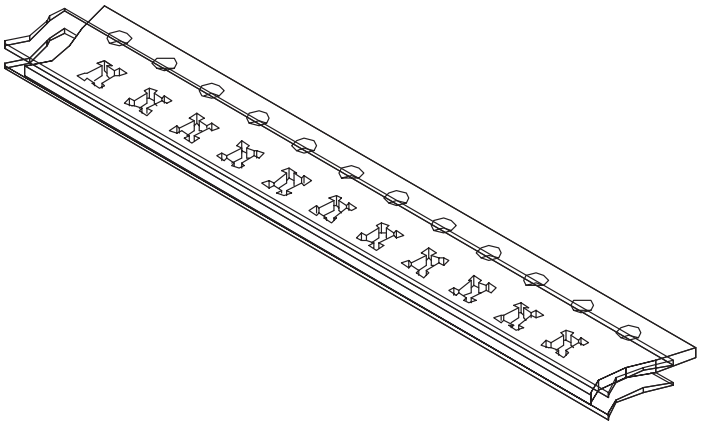
UNIT	X1	X2	X3	X4	X5	X6	X7
mm	1.30 1.24	0.87 0.81	0.5	0.5	0.195 0.165	0.467 0.447	0.145 0.115

SL02055

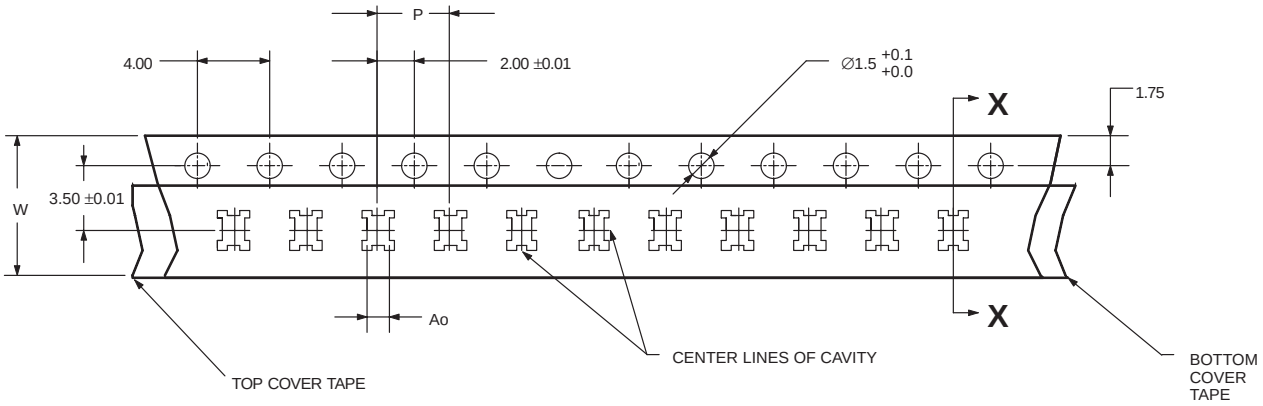
TAPE & REEL IN WAFER LEVEL CHIP-SCALE PACKAGE

LOADED TAPE DIRECTION OF FEED





NOTES:
All dimensions in millimeters.
10 sprocket hole pitch cumulative tolerance ±0.20
Material: conductive polystyrene
Camber not to exceed 1.0 mm in 100 mm.
Cover tape shown for illustrative purposes only.

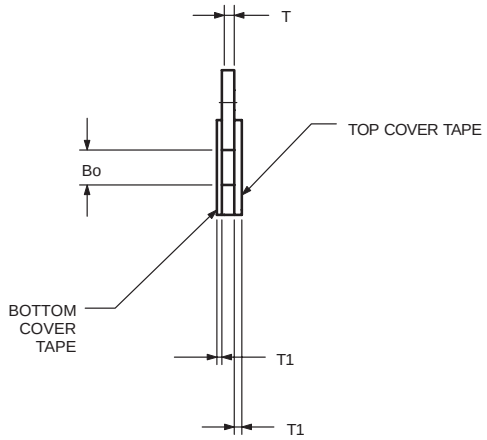


DIMENSIONS (mm are the original dimensions)

UNIT	Ao	Bo	T	T1	P	W
mm	1.09 0.99	1.598 1.498	0.76 0.74	0.10 (max.)	4.05 3.95	8.3 7.9

Heat seal cover tape for carrier tape width 8 mm

Type tape:	clear static dissipative tape
Base material:	transparent polyester
Cover tape width:	5.3 ± 0.1 mm
Cover tape length:	480 m/reel
Supplier:	Advanced Integrated Materials (AIM)
Part Number:	CT5–00530–0480



SECTION 'X – X'

SL02056

PACKING METHOD

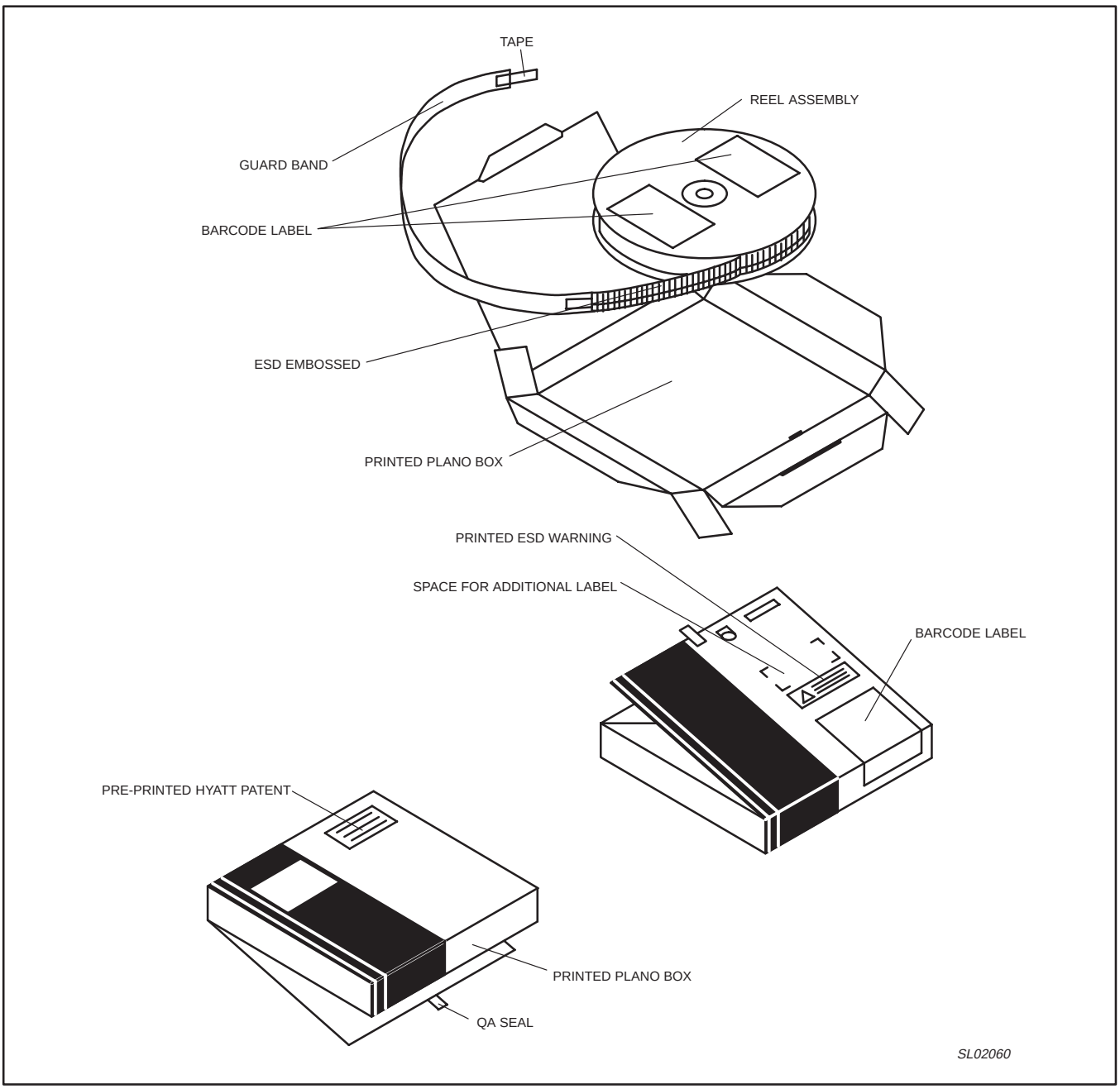
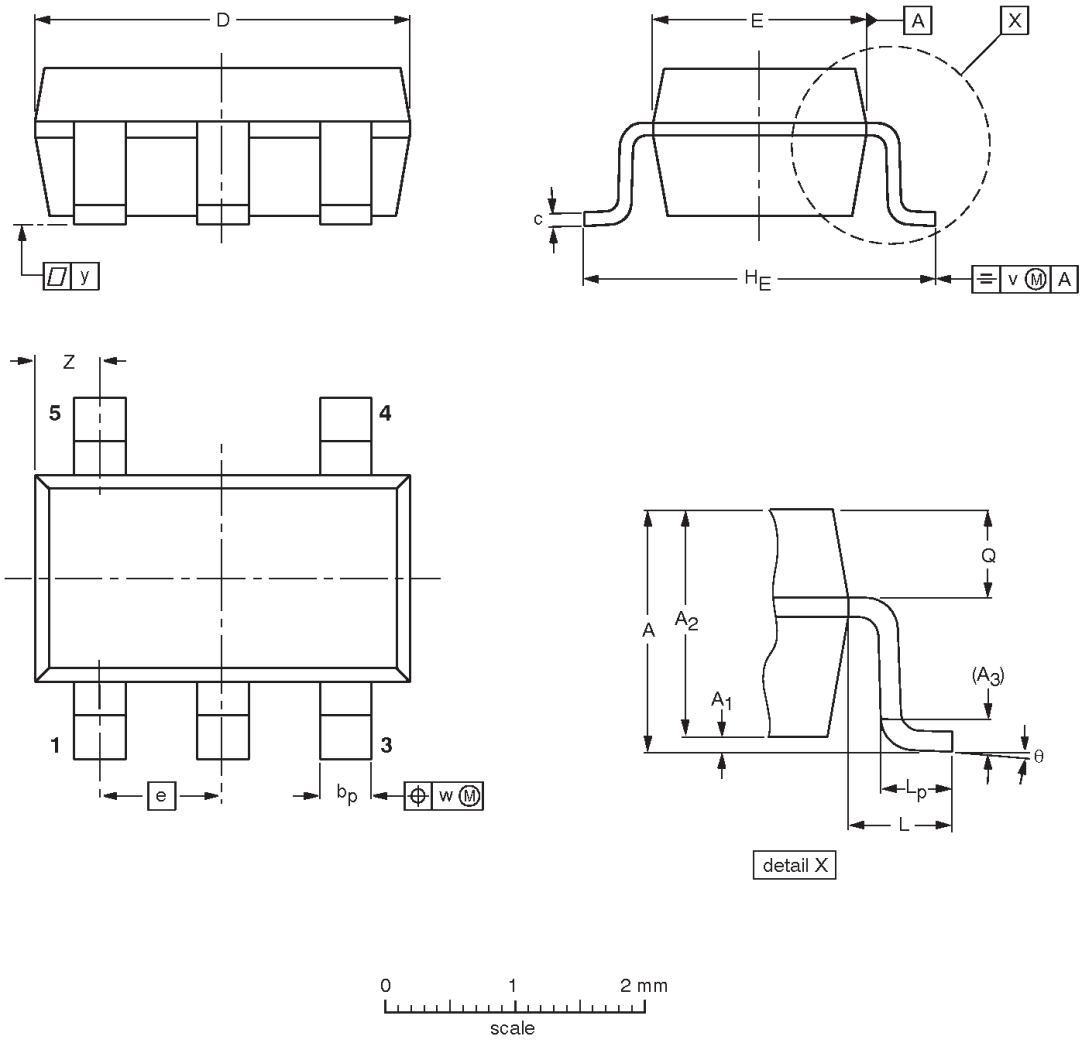


Figure 14. Tape and reel packing method

SO5: plastic small outline package; 5 leads; body width 1.6 mm **SOT680-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.45	0.15 0.05	1.3 0.9	0.2	0.5 0.3	0.22 0.08	3.05 2.75	1.75 1.45	0.95	3.0 2.6	0.6	0.6 0.3	0.45 0.35	0.2	0.2	0.1	0.75 0.25	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT680-1		MO-178				~~01-03-22~~ 01-11-15

REVISION HISTORY

Rev	Date	Description
_6	20030730	**Product data (9397 750 11836); ECN 853-2265 29874 of 28 July 2003; supersedes data of 2003 Apr 30 (9397 750 11452).** Modifications: ● Add “Marking code” table to page 3.
_5	20030430	**Product data (9397 750 11452); ECN 853-2265 29874 of 29 April 2003; supersedes data of 2003 Apr 01 (9397 750 10539).**
_4	20030401	**Product data (9397 750 10539); ECN 853–2265 29019 of 07 October 2002; supersedes data of 2001 Oct 16 (9397 750 08983).**
_3	20011016	Product data (9397 750 08983); ECN 853-2265 27240 of 16 October 2001.
_2	20010827	Product data (9397 750 08722); ECN 853–2265 26991 of 27 August 2001.
_1	20010712	Product data (9397 750 08564); ECN 853-2265 26703 of 12 July 2001.

CapFREE™ 150 mA, low-noise, low dropout regulator with thermal protection

SA57000-XX

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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Date of release: 07-03

Document order number: 9397 750 11836

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