CMOS Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers with Shutdown

AD8591/AD8592/AD8594

FEATURES

Single-supply operation: 2.5 V to 6 V
High output current: ±250 mA
Extremely low shutdown supply current: 100 nA
Low supply current: 750 µA/Amp
Wide bandwidth: 3 MHz
Slew rate: 5 V/µs
No phase reversal
Very low input bias current
High impedance outputs when in shutdown mode
Unity-gain stable

APPLICATIONS

Mobile communication handset audio
PC audio
PCMCIA/modem line driving
Battery-powered instrumentation
Data acquisition
ASIC input or output amplifiers
LCD display reference level drivers

GENERAL DESCRIPTION

The AD8591, AD8592, and AD8594 are single, dual, and quad rail-to-rail, input and output single-supply amplifiers featuring 250 mA output drive current and a power saving shutdown mode. The AD8592 includes an independent shutdown function for each amplifier. When both amplifiers are in shutdown mode, the total supply current is reduced to less than 1 µA. The AD8591 and AD8594 include a single master shutdown function that reduces the total supply current to less than 1 µA. All amplifier outputs are in a high impedance state when in shutdown mode.

These amplifiers have very low input bias currents, making them suitable for integrators and diode amplification. Outputs are stable with virtually any capacitive load. Supply current is less than 750 µA per amplifier in active mode.

Applications for these amplifiers include audio amplification for portable computers, portable phone headsets, sound ports, sound cards, and set-top boxes. The AD859x family is capable of driving heavy capacitive loads, such as LCD panel reference levels.

The ability to swing rail to rail at both the input and output enables designers to buffer CMOS DACs, ASICs, and other wide output swing devices in single-supply systems.

PIN CONFIGURATIONS

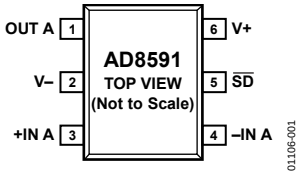


Figure 1. 6-Lead SOT-23 (RJ Suffix)

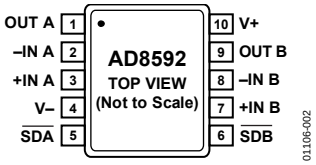


Figure 2. 10-Lead MSOP (RM Suffix)

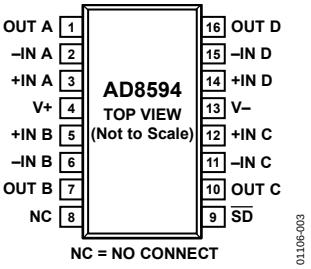


Figure 3. 16-Lead Narrow SOIC (R Suffix)

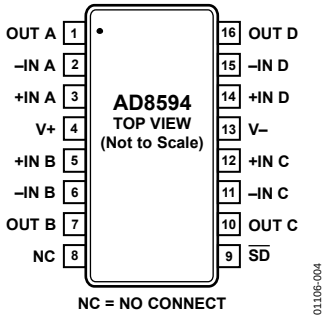


Figure 4. 16-Lead TSSOP (RU Suffix)

The AD8591, AD8592, and AD8594 are specified over the industrial temperature range (−40°C to +85°C). The AD8591, single, is available in the tiny 6-lead SOT-23 package. The AD8592, dual, is available in the 10-lead surface-mount MSOP package. The AD8594, quad, is available in 16-lead narrow SOIC and 16-lead TSSOP packages.

Rev. B
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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Pin Configurations ... 1
Revision History ... 2
Specifications ... 3
  Electrical Characteristics ... 3
Absolute Maximum Ratings ... 5
  Thermal Resistance ... 5
  ESD Caution ... 5
Typical Performance Characteristics ... 6
Theory of Operation ... 11
  Input Voltage Protection ... 11
  Output Phase Reversal ... 11
  Output Short-Circuit Protection ... 11
  Power Dissipation ... 11
  Capacitive Loading ... 12
  PC98-Compliant Headphone/Speaker Amplifier ... 12
  A Combined Microphone and Speaker Amplifier for Cellphone and Portable Headsets ... 13
  An Inexpensive Sample-and-Hold Circuit ... 13
  Direct Access Arrangement for PCMCIA Modems (Telephone Line Interface) ... 14
  Single-Supply Differential Line Driver ... 14
Outline Dimensions ... 15
  Ordering Guide ... 16

REVISION HISTORY

1/09—Rev. A to Rev. B

Updated Format ... Universal
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Deleted Spice Model for AD8591/AD8592/AD8594 Amplifiers Sections ... 12
Changes to PC98-Compliant Headphone/Speaker Amplifier Section and Figure 38 ... 12
Changes to Figure 39 ... 13
Changes to Figure 42 and Figure 43 ... 14
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 16

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 2.7 V, V_{CM} = 1.35 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				25	mV
		−40°C < T_A < +85°C			30	mV
Input Bias Current	I_B			5	50	pA
		−40°C < T_A < +85°C			60	pA
Input Offset Current	I_{OS}			1	25	pA
		−40°C < T_A < +85°C			30	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	38	45		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.3 V to 2.4 V		25		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C		20		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C < T_A < +85°C		50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	−40°C < T_A < +85°C		20		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA	2.55	2.61		V
		−40°C to +85°C	2.5			V
Output Voltage Low	V_{OL}	I_L = 10 mA		60	100	mV
		−40°C to +85°C			125	mV
Output Current	I_{OUT}			±250		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		60		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.5 V to 6 V	45	55		dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V			1	mA
		−40°C < T_A < +85°C			1.25	mA
Supply Current Shutdown Mode	I_{SD}	All amplifiers shut down		0.1	1	µA
		−40°C < T_A < +85°C			1	µA
	I_{SD1}	Amplifier 1 shut down (AD8592)			1.4	mA
	I_{SD2}	Amplifier 2 shut down (AD8592)			1.4	mA
SHUTDOWN INPUTS						
Logic High Voltage	V_{INH}	−40°C < T_A < +85°C	1.6			V
Logic Low Voltage	V_{INL}	−40°C < T_A < +85°C			0.5	V
Logic Input Current	I_{IN}	−40°C < T_A < +85°C			1	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/µs
Settling Time	t_S	To 0.01%		1.4		µs
Gain Bandwidth Product	GBP			2.2		MHz
Phase Margin	Φo			67		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
		f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2	25	mV
		−40°C < T_A < +85°C			30	mV
Input Bias Current	I_B			5	50	pA
		−40°C < T_A < +85°C			60	pA
Input Offset Current	I_{OS}			1	25	pA
		−40°C < T_A < +85°C			30	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	38	47		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	15	30		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C		20		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C < T_A < +85°C		50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	−40°C < T_A < +85°C		20		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA	4.9	4.94		V
		−40°C to +85°C	4.85			V
Output Voltage Low	V_{OL}	I_L = 10 mA		50	100	mV
		−40°C to +85°C			125	mV
Output Current	I_{OUT}			±250		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		40		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.5 V to 6 V	45	55		dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V			1.25	mA
		−40°C < T_A < +85°C			1.75	mA
Supply Current Shutdown Mode	I_{SD}	All amplifiers shut down		0.1	1	μA
		−40°C < T_A < +85°C			1	μA
	I_{SD1}	Amplifier 1 shut down (AD8592)			1.6	mA
	I_{SD2}	Amplifier 2 shut down (AD8592)			1.6	mA
SHUTDOWN INPUTS						
Logic High Voltage	V_{INH}	−40°C < T_A < +85°C	2.4			V
Logic Low Voltage	V_{INL}	−40°C < T_A < +85°C			0.8	V
Logic Input Current	I_{IN}	−40°C < T_A < +85°C			1	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		5		V/μs
Full Power Bandwidth	BW_P	1% distortion		325		kHz
Settling Time	t_S	To 0.01%		1.6		μs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	Φo			70		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
		f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S
Differential Input Voltage	±6 V
Output Short-Circuit Duration to GND[1]	Observe Derating Curves
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] For supplies less than ±5 V, the differential input voltage is limited to the supplies.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
6-Lead SOT-23 (RJ)	230	92	°C/W
10-Lead MSOP (RM)	200	44	°C/W
16-Lead SOIC (R)	120	36	°C/W
16-Lead TSSOP (RU)	180	35	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

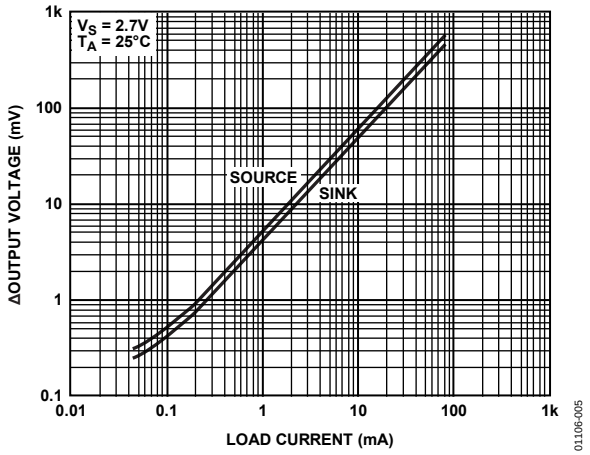


Figure 5. Output Voltage to Supply Rail vs. Load Current

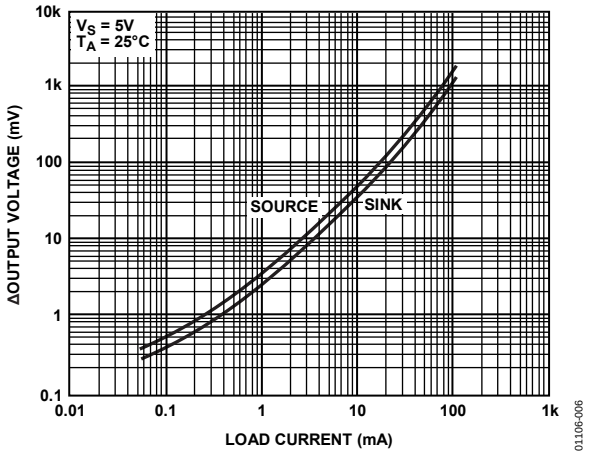


Figure 6. Output Voltage to Supply Rail vs. Load Current

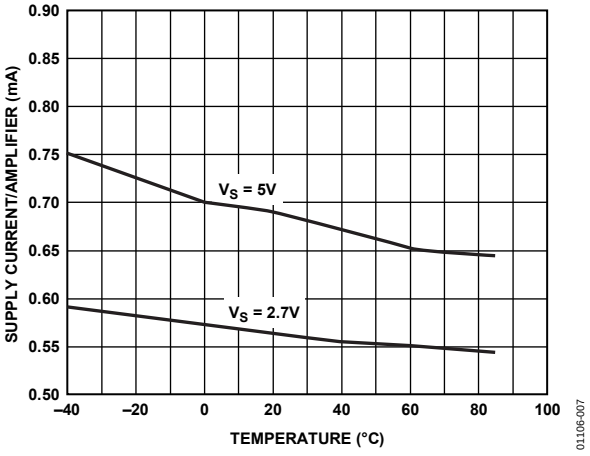


Figure 7. Supply Current per Amplifier vs. Temperature

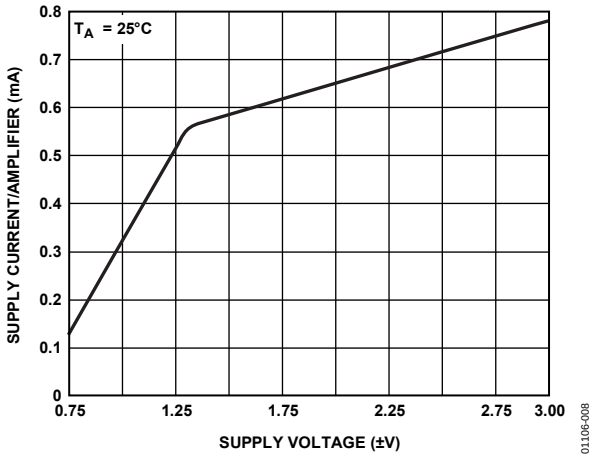


Figure 8. Supply Current per Amplifier vs. Supply Voltage

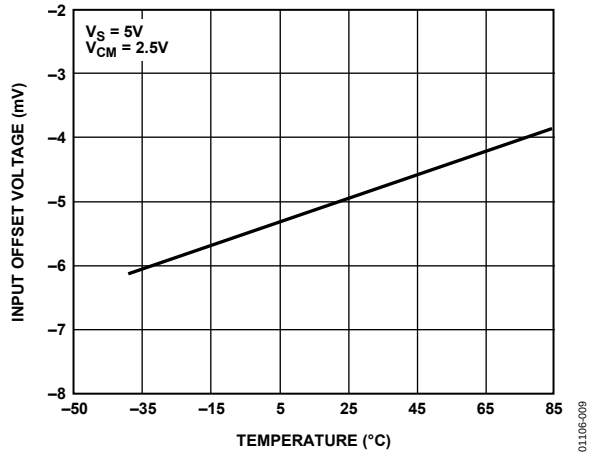


Figure 9. Input Offset Voltage vs. Temperature

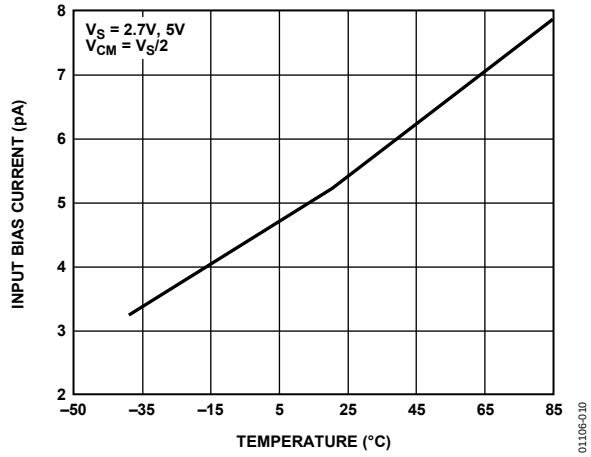


Figure 10. Input Bias Current vs. Temperature

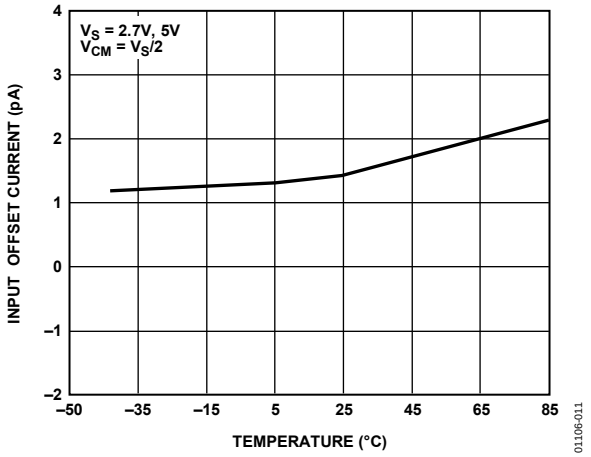


Figure 11. Input Offset Current vs. Temperature

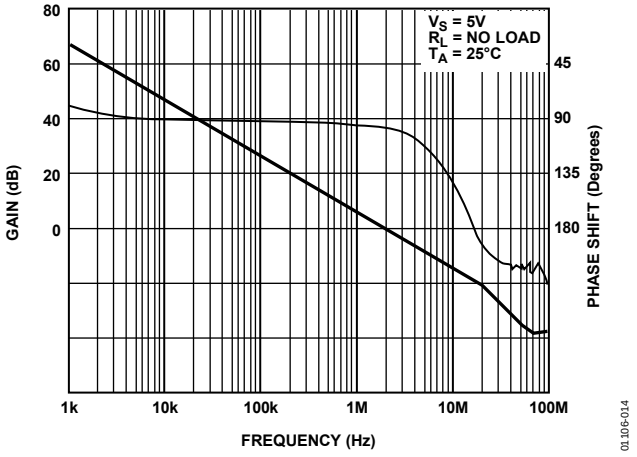


Figure 14. Open-Loop Gain and Phase vs. Frequency

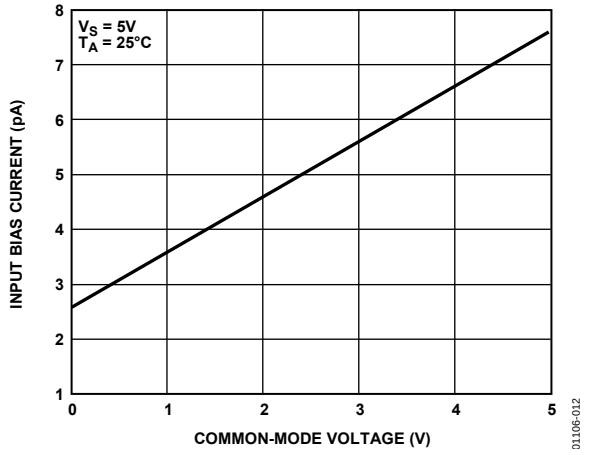


Figure 12. Input Bias Current vs. Common-Mode Voltage

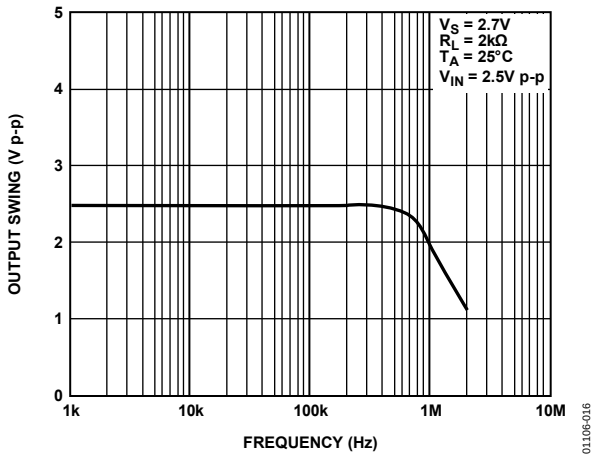


Figure 15. Closed-Loop Output Voltage Swing vs. Frequency

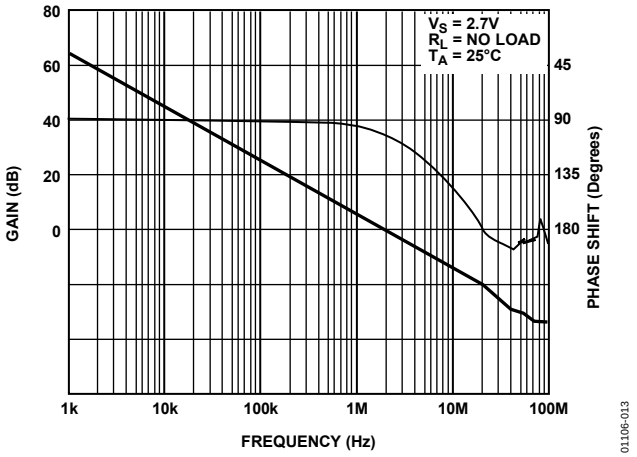


Figure 13. Open-Loop Gain and Phase vs. Frequency

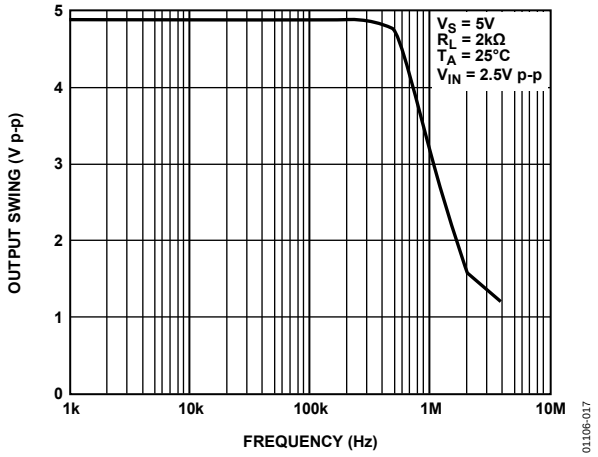


Figure 16. Closed-Loop Output Voltage Swing vs. Frequency

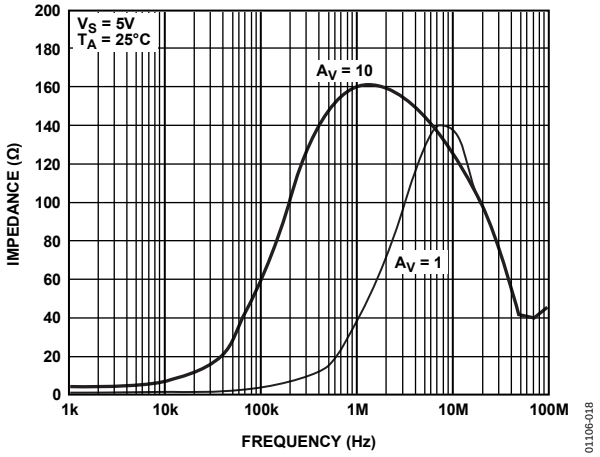


Figure 17. Closed-Loop Output Impedance vs. Frequency

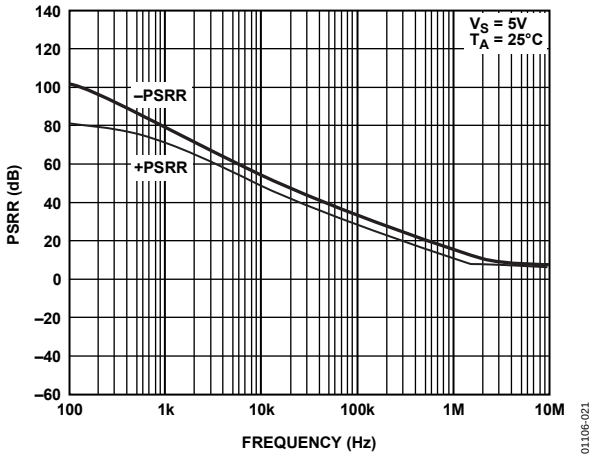


Figure 20. Power Supply Rejection Ratio vs. Frequency

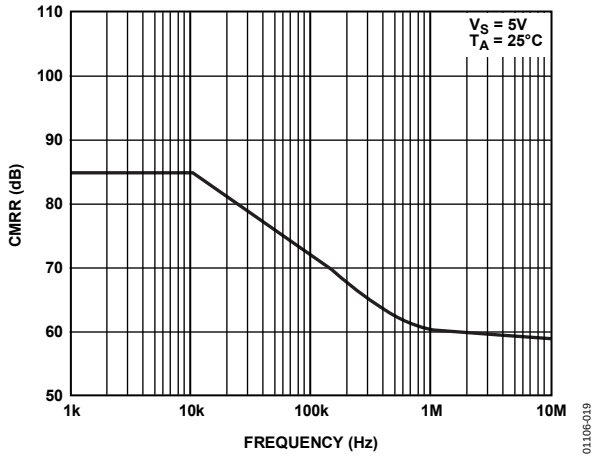


Figure 18. Common-Mode Rejection Ratio vs. Frequency

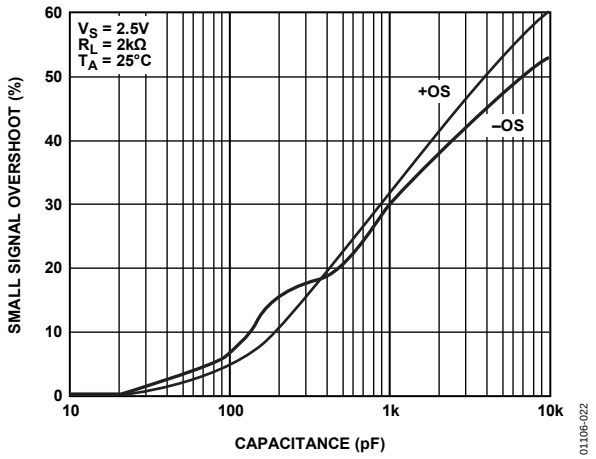


Figure 21. Small Signal Overshoot vs. Load Capacitance

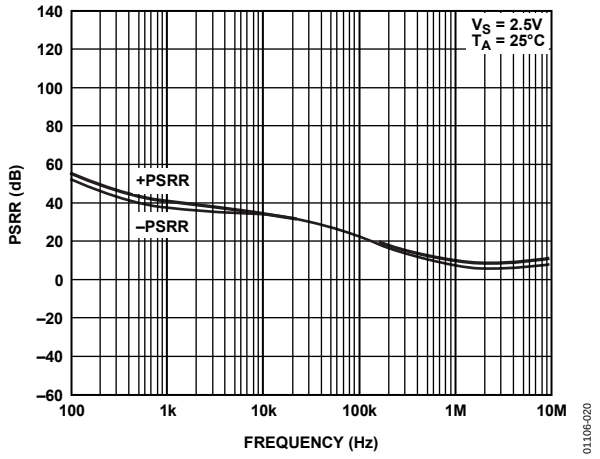


Figure 19. Power Supply Rejection Ratio vs. Frequency

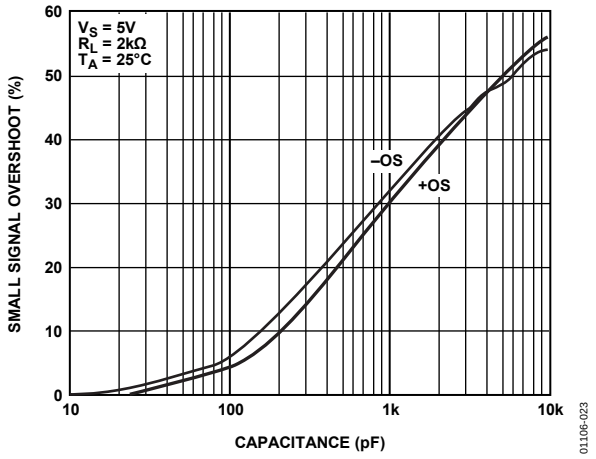


Figure 22. Small Signal Overshoot vs. Load Capacitance

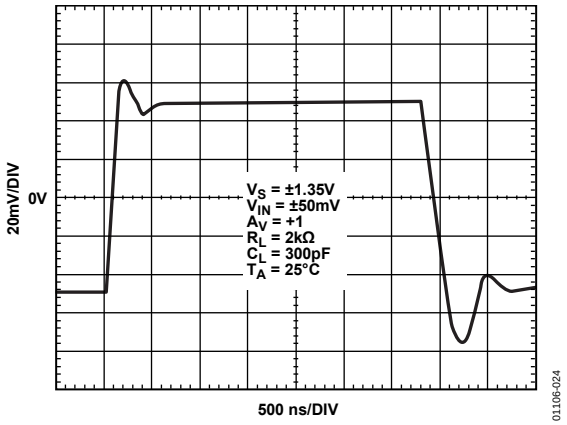


Figure 23. Small Signal Transient Response

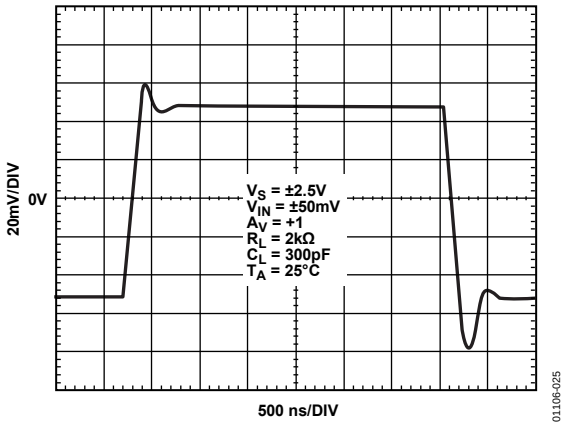


Figure 24. Small Signal Transient Response

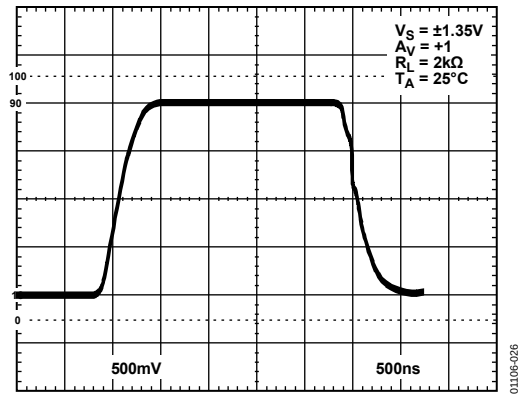


Figure 25. Large Signal Transient Response

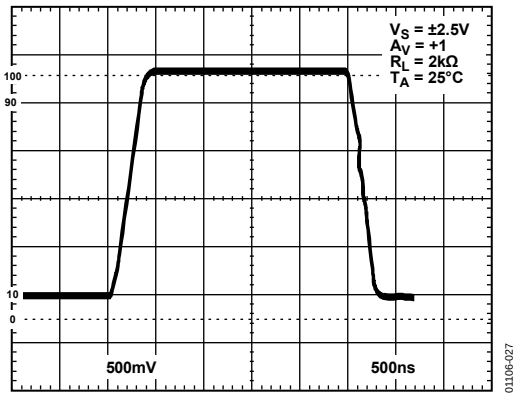


Figure 26. Large Signal Transient Response

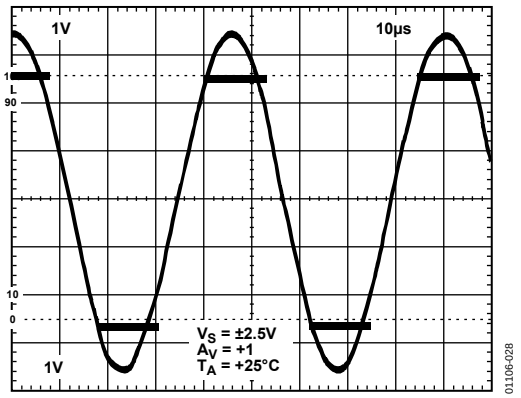


Figure 27. No Phase Reversal

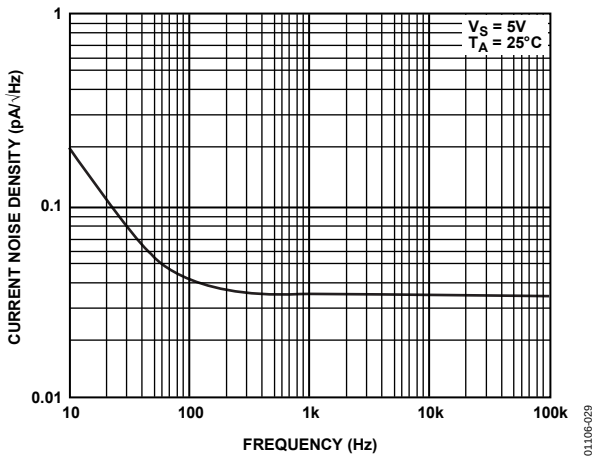


Figure 28. Current Noise Density vs. Frequency

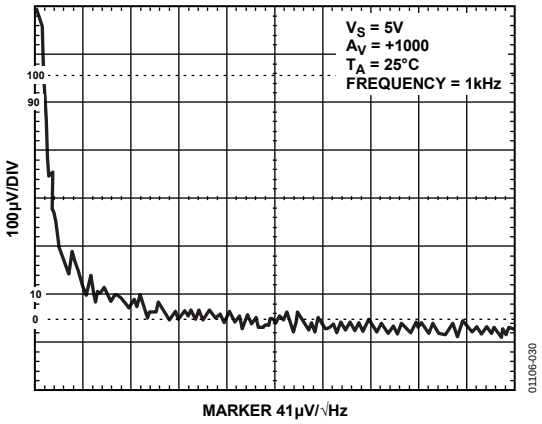


Figure 29. Voltage Noise Density vs. Frequency

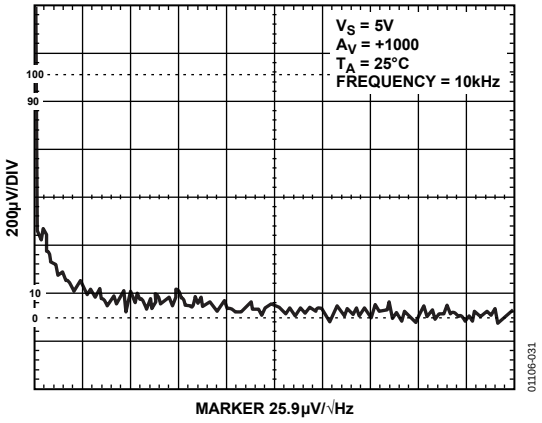


Figure 30. Voltage Noise Density vs. Frequency

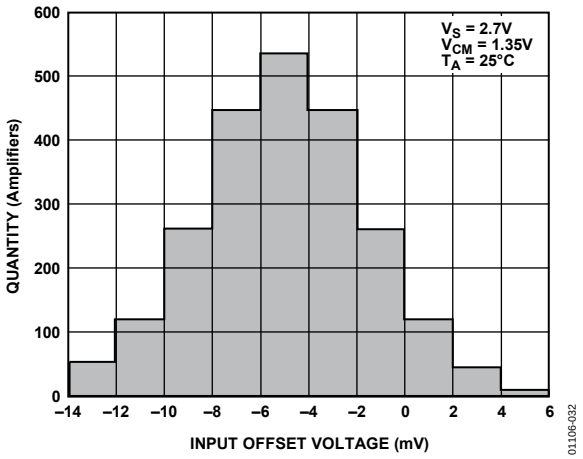


Figure 31. Input Offset Voltage Distribution

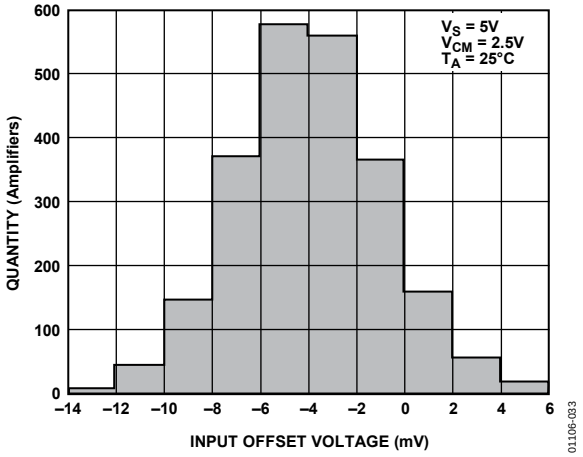


Figure 32. Input Offset Voltage Distribution

THEORY OF OPERATION

The AD859x amplifiers are CMOS, high output drive, rail-to-rail input and output single-supply amplifiers designed for low cost and high output current drive. The parts include a power saving shutdown function that makes the AD8591/AD8592/AD8594 op amps ideal for portable multimedia and telecommunications applications.

Figure 33 shows the simplified schematic for the AD8591/AD8592/AD8594 amplifiers. Two input differential pairs, consisting of an n-channel pair (M1, M2) and a p-channel pair (M3, M4), provide a rail-to-rail input common-mode range. The outputs of the input differential pairs are combined in a compound folded-cascode stage that drives the input to a second differential pair gain stage. The outputs of the second gain stage provide the gate voltage drive to the rail-to-rail output stage.

The rail-to-rail output stage consists of M15 and M16, which are configured in a complementary common source configuration. As with any rail-to-rail output amplifier, the gain of the output stage, and thus the open-loop gain of the amplifier, is dependent on the load resistance. In addition, the maximum output voltage swing is directly proportional to the load current. The difference between the maximum output voltage to the supply rails, known as the dropout voltage, is determined by the on-channel resistance of the AD8591/AD8592/AD8594 output transistors. The output dropout voltage is given in Figure 5 and Figure 6.

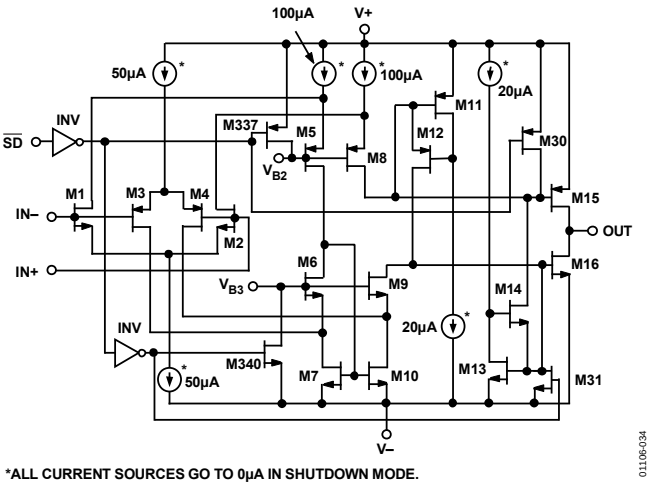


Figure 33. Simplified Schematic

INPUT VOLTAGE PROTECTION

Although not shown in the simplified schematic, ESD protection diodes are connected from each input to each power supply rail. These diodes are normally reverse-biased, but turn on if either input voltage exceeds either supply rail by more than 0.6 V. If this condition occurs, limit the input current to less than ±5 mA. This is done by placing a resistor in series with the input(s). The minimum resistor value should be

$$R_{IN} \geq \frac{V_{IN,MAX}}{5\text{ mA}} \quad (1)$$

OUTPUT PHASE REVERSAL

The AD8591/AD8592/AD8594 are immune to output voltage phase reversal with an input voltage within the supply voltages of the device. However, if either of the inputs of the device exceeds 0.6 V outside of the supply rails, the output could exhibit phase reversal. This is due to the ESD protection diodes becoming forward-biased, thus causing the polarity of the input terminals of the device to switch.

The technique recommended in the Input Voltage Protection section should be applied in applications where the possibility of input voltages exceeding the supply voltages exists.

OUTPUT SHORT-CIRCUIT PROTECTION

To achieve high output current drive and rail-to-rail performance, the outputs of the AD859x family do not have internal short-circuit protection circuitry. Although these amplifiers are designed to sink or source as much as 250 mA of output current, shorting the output directly to the positive supply could damage or destroy the device. To protect the output stage, limit the maximum output current to ±250 mA.

By placing a resistor in series with the output of the amplifier, as shown in Figure 34, the output current can be limited. The minimum value for R_X is

$$R_X \geq \frac{V_{SY}}{250\text{ mA}} \quad (2)$$

For a 5 V single-supply application, R_X should be at least 20 Ω. Because R_X is inside the feedback loop, V_{OUT} is not affected. The trade-off in using R_X is a slight reduction in output voltage swing under heavy output current loads. R_X also increases the effective output impedance of the amplifier to $R_O + R_X$, where R_O is the output impedance of the device.

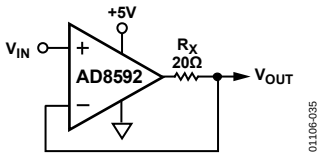


Figure 34. Output Short-Circuit Protection

POWER DISSIPATION

Although the AD859x amplifiers are able to provide load currents of up to 250 mA, proper attention should be given to not exceeding the maximum junction temperature for the device. The junction temperature equation is

$$T_J = P_{DISS} \times \theta_{JA} + T_A \quad (3)$$

where:
T_J is the AD859x junction temperature.
P_{DISS} is the AD859x power dissipation.
θ_{JA} is the AD859x junction-to-ambient thermal resistance of the package.
T_A is the ambient temperature of the circuit.

In any application, the absolute maximum junction temperature must be limited to 150°C. If the junction temperature is exceeded, the device could suffer premature failure. If the output voltage and output current are in phase, for example, with a purely resistive load, the power dissipated by the AD859x can be found as

$$P_{DISS} = I_{LOAD} \times (V_{SY} - V_{OUT}) \quad (4)$$

where:
I_{LOAD} is the AD859x output load current.
V_{SY} is the AD859x supply voltage.
V_{OUT} is the output voltage.

By calculating the power dissipation of the device and using the thermal resistance value for a given package type, the maximum allowable ambient temperature for an application can be found using Equation 3.

CAPACITIVE LOADING

The AD859x exhibits excellent capacitive load driving capabilities and can drive to 10 nF directly. Although the device is stable with large capacitive loads, there is a decrease in amplifier bandwidth as the capacitive load increases. Figure 35 shows a graph of the AD8592 unity-gain bandwidth under various capacitive loads.

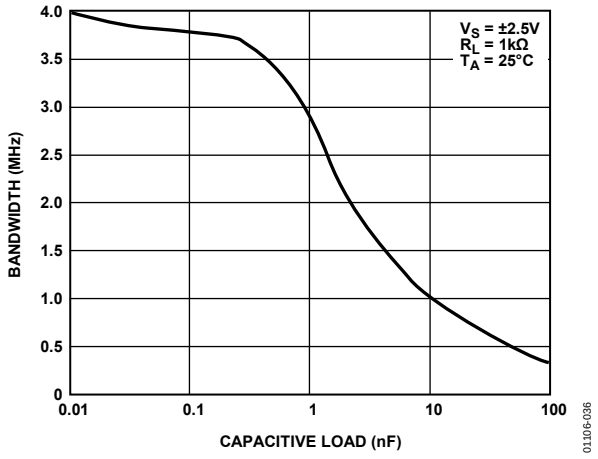


Figure 35. Unity-Gain Bandwidth vs. Capacitive Load

When driving heavy capacitive loads directly from the AD859x output, a snubber network can be used to improve the transient response. This network consists of a series RC connected from the output of the amplifier to ground, placing it in parallel with the capacitive load. The configuration is shown in Figure 36. Although this network does not increase the bandwidth of the amplifier, it significantly reduces the amount of overshoot, as shown in Figure 37.

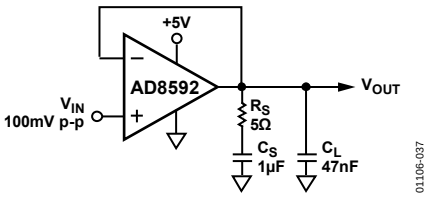


Figure 36. Configuration for Snubber Network to Compensate for Capacitive Loads

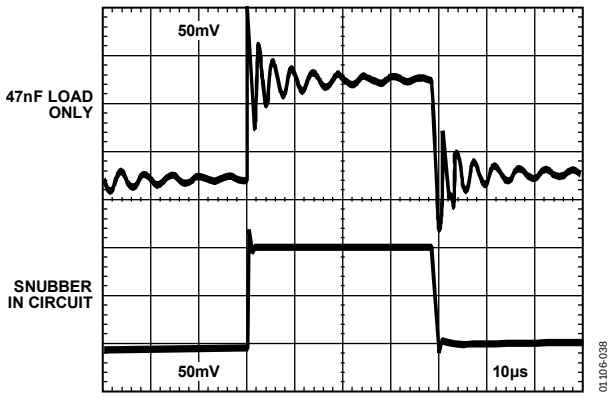


Figure 37. Snubber Network Reduces Overshoot and Ringing Caused by Driving Heavy Capacitive Loads

The optimum values for the snubber network should be determined empirically based on the size of the capacitive load. Table 5 shows a few sample snubber network values for a given load capacitance.

Table 5. Snubber Networks for Large Capacitive Loads

	Snubber Network	
Load Capacitance, C_L (nF)	**R_S (Ω)**	**C_S (µF)**
0.47	300	0.1
4.7	30	1
47	5	1

PC98-COMPLIANT HEADPHONE/SPEAKER AMPLIFIER

Because of its high output current performance and shutdown feature, the AD8592 makes an excellent amplifier for driving an audio output jack in a computer application. Figure 38 shows how the AD8592 can be interfaced with an AC'97 codec to drive headphones or speakers.

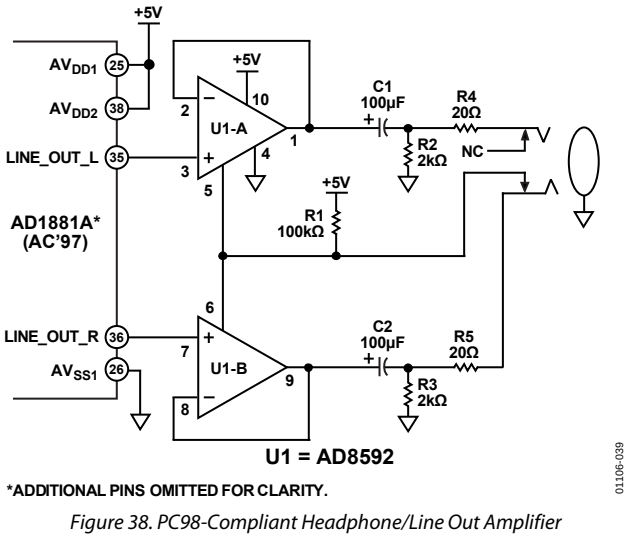


Figure 38. PC98-Compliant Headphone/Line Out Amplifier

When headphones are plugged into the jack, the normalizing contacts disconnect from the audio contacts. This allows the voltage to the AD8592 shutdown pins to be pulled to 5 V, activating the amplifiers. With no plug in the output jack, the shutdown voltage is pulled to 100 mV through the R1 and R3 + R5 voltage divider. This powers the AD8592 down when it is not needed, saving current from the power supply or battery.

If gain is required from the output amplifier, add four additional resistors, as shown in Figure 39. The gain of the AD8592 can be set as

$$A_V = \frac{R7}{R6} \quad (5)$$

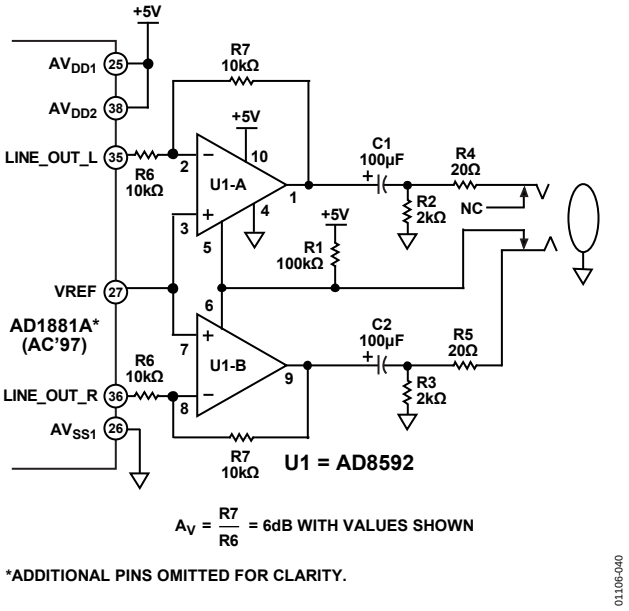


Figure 39. PC98-Compliant Headphone/Line Out Amplifier with Gain

Input coupling capacitors are not required for either circuit because the reference voltage is supplied from the AD1881A.

R4 and R5 help protect the AD8592 output in case the output jack or headphone wires accidentally are shorted to ground. The output coupling capacitors, C1 and C2, block dc current from the headphones and create a high-pass filter with a corner frequency of

$$f_{-3dB} = \frac{1}{2\pi C1\left(R4 + R_L\right)} \quad (6)$$

where R_L is the resistance of the headphones.

A COMBINED MICROPHONE AND SPEAKER AMPLIFIER FOR CELLPHONE AND PORTABLE HEADSETS

The dual amplifiers in the AD8592 make an efficient design for interfacing with a headset containing a microphone and speaker. Figure 40 demonstrates a simple method for constructing an interface to a codec.

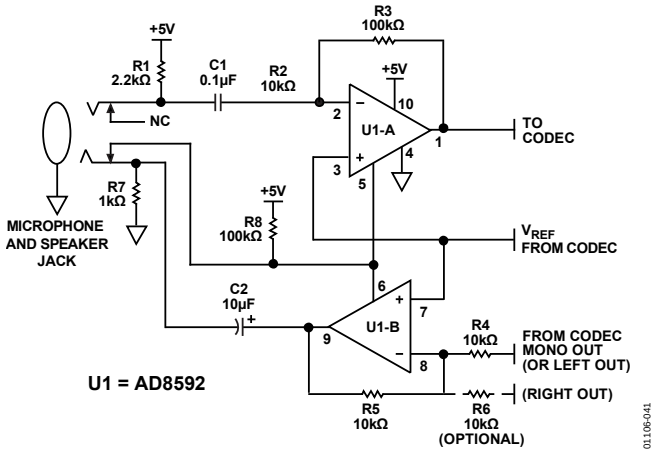


Figure 40. Speaker/Microphone Headset Amplifier Circuit

U1-A is used as a microphone preamplifier, where the gain of the preamplifier is set as R3/R2. R1 is used to bias an electret microphone, and C1 blocks any dc voltages from the amplifier. U1-B is the speaker amplifier, and its gain is set at R5/R4. To sum a stereo output, add R6, equal in value to R4.

Using the same principle described in the PC98-Compliant Headphone/Speaker Amplifier section, the normalizing contact on the microphone/speaker jack can be used to put the AD8592 into shutdown when the headset is not plugged in. The AD8592 shutdown inputs can also be controlled with TTL- or CMOS-compatible logic, allowing microphone or speaker muting, if desired.

AN INEXPENSIVE SAMPLE-AND-HOLD CIRCUIT

The independent shutdown control of each amplifier in the AD8592 allows a degree of flexibility in circuit design. One particular application for which this feature is useful is in designing a sample-and-hold circuit for data acquisition. Figure 41 shows a schematic of a simple, yet extremely effective, sample-and-hold circuit using a single AD8592 and one capacitor.

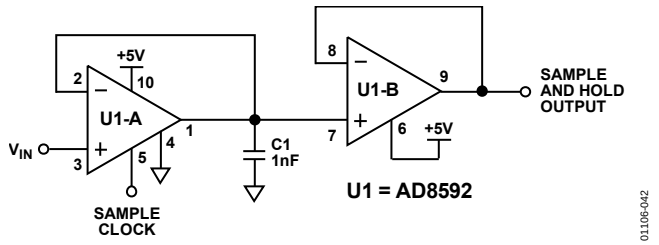


Figure 41. An Efficient Sample-and-Hold Circuit

The U1-A amplifier is configured as a unity-gain buffer driving a 1 nF capacitor. The input signal is connected to the noninverting input, and the sample clock controls the shutdown for that amplifier. When the sample clock is high, the U1-A amplifier is active and the output follows V_{IN}. When the sample clock goes low, U1-A shuts down with the output of the amplifier going to a high impedance state, holding the voltage on the C1 capacitor.

The U1-B amplifier is used as a unity-gain buffer to prevent loading on C1. Because of the low input bias current of the U1-B CMOS input stage and the high impedance state of the U1-A output in shutdown, there is little voltage droop from C1 during the hold period. This circuit can be used with sample frequencies as high as 500 kHz and as low as 1 Hz. By increasing the C1 value, lower voltage droop is achieved for very low sample rates.

DIRECT ACCESS ARRANGEMENT FOR PCMCIA MODEMS (TELEPHONE LINE INTERFACE)

Figure 42 illustrates a 5 V transmit/receive telephone line interface for 600 Ω systems. It allows full duplex transmission of signals on a transformer-coupled 600 Ω line in a differential manner. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible signal on a single supply to the transformer. Because of the high output current drive and low dropout voltages of the AD8594, the largest signal available on a single 5 V supply is approximately 4.5 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier for two reasons. It prevents the transmit signal from interfering with the receive signal, and it extracts the receive signal from the transmission line for amplification by A4. The gain of A4 can be adjusted in the same manner as the gain of A1 to meet the input signal requirements of the modem. Standard resistor values permit the use of single inline package (SIP) format resistor arrays. Couple this with the 16-lead TSSOP or SOIC footprint of the AD8594, and this circuit offers a compact, cost-effective solution.

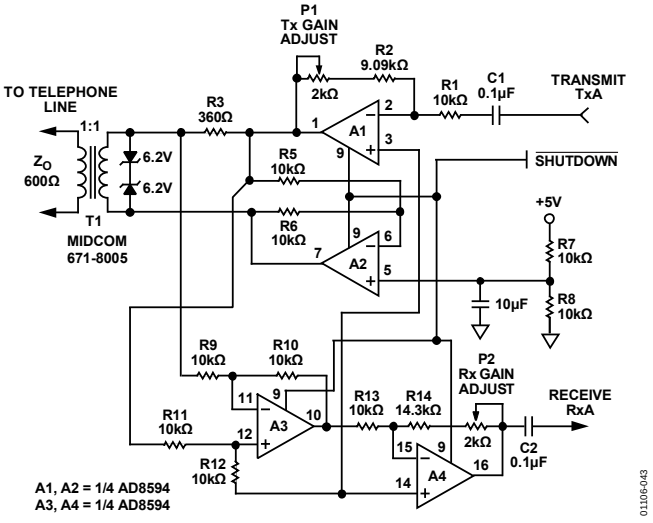


Figure 42. Single-Supply Direct Access Arrangement for PCMCIA Modems

SINGLE-SUPPLY DIFFERENTIAL LINE DRIVER

Figure 43 shows a single-supply differential line driver circuit that can drive a 600 Ω load with less than 0.7% distortion from 20 Hz to 15 kHz with an input signal of 4 V p-p and a single 5 V supply. The design uses an AD8594 to mimic the performance of a fully balanced transformer-based solution. However, this design occupies much less board space, while maintaining low distortion, and can operate down to dc. Like the transformer-based design, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1.

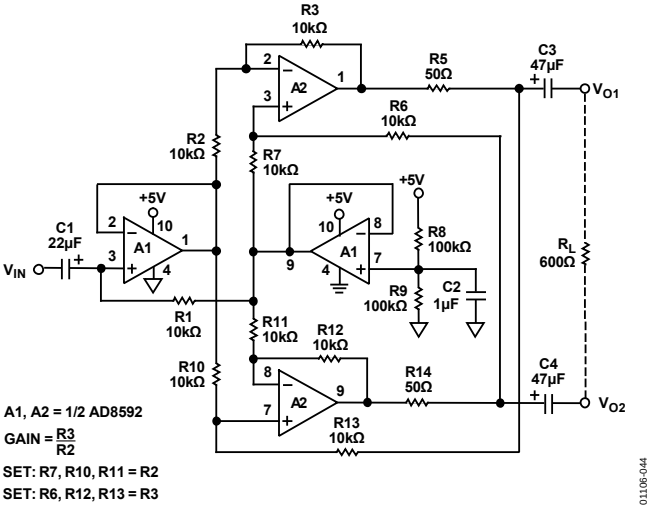


Figure 43. Low Noise, Single-Supply Differential Line Driver

R8 and R9 set up the common-mode output voltage equal to half of the supply voltage. C1 is used to couple the input signal and can be omitted if the dc voltage of the input is equal to half of the supply voltage.

The circuit can also be configured to provide additional gain, if desired. The gain of the circuit is

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R3}{R2} \quad (7)$$

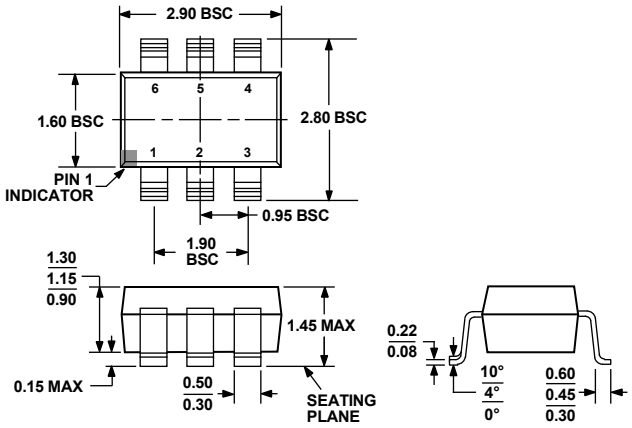
where:

$V_{OUT} = V_{O1} - V_{O2}$

$R2 = R7 = R10 = R11$

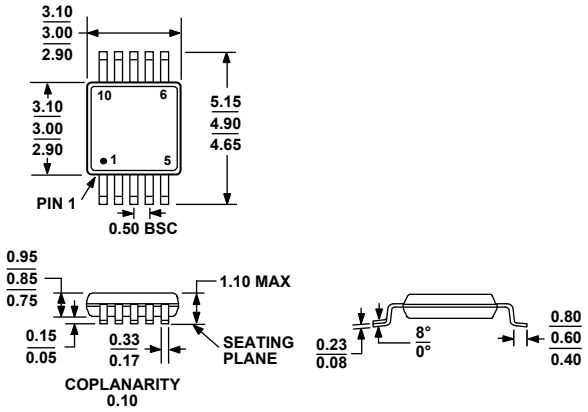
$R3 = R6 = R12 = R1$

OUTLINE DIMENSIONS



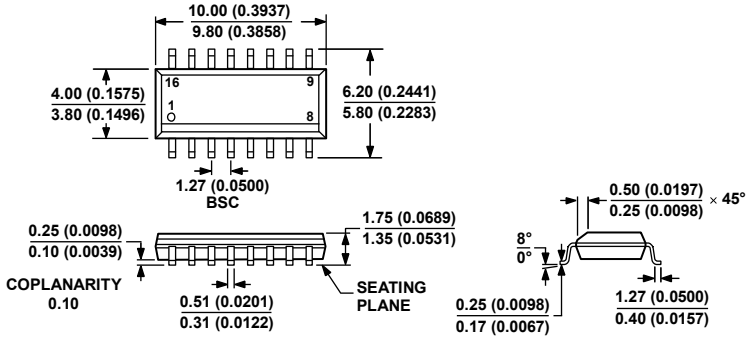
COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 44. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 45. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 46. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-16)
Dimensions shown in millimeters and (inches)

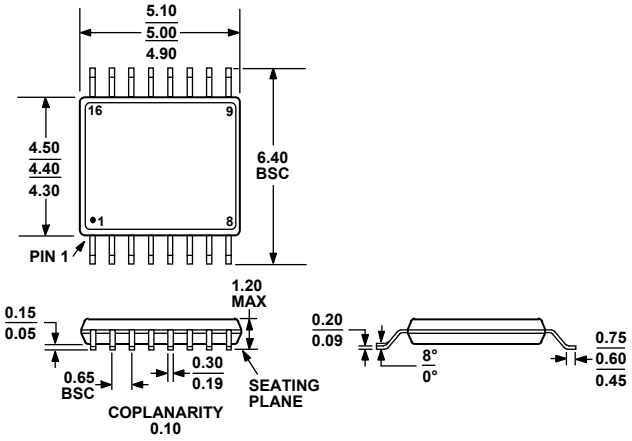


Figure 47. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8591ART-REEL	−40°C to +85°C	6-Lead SOT-23	RJ-6	A9A
AD8591ART-REEL7	−40°C to +85°C	6-Lead SOT-23	RJ-6	A9A
AD8591ARTZ-REEL[1]	−40°C to +85°C	6-Lead SOT-23	RJ-6	A9A#
AD8591ARTZ-REEL7[1]	−40°C to +85°C	6-Lead SOT-23	RJ-6	A9A#
AD8592ARM-REEL	−40°C to +85°C	10-Lead MSOP	RM-10	AQA
AD8592ARMZ-REEL[1]	−40°C to +85°C	10-Lead MSOP	RM-10	AQA#
AD8594AR	−40°C to +85°C	16-Lead SOIC_N	R-16	
AD8594AR-REEL	−40°C to +85°C	16-Lead SOIC_N	R-16	
AD8594AR-REEL7	−40°C to +85°C	16-Lead SOIC_N	R-16	
AD8594ARZ[1]	−40°C to +85°C	16-Lead SOIC_N	R-16	
AD8594ARZ-REEL[1]	−40°C to +85°C	16-Lead SOIC_N	R-16	
AD8594ARZ-REEL7[1]	−40°C to +85°C	16-Lead SOIC_N	R-16	
AD8594ARU-REEL	−40°C to +85°C	16-Lead TSSOP	RU-16	
AD8594ARUZ-REEL[1]	−40°C to +85°C	16-Lead TSSOP	RU-16	

[1] Z = RoHS Compliant Part, # denotes RoHS compliant part may be top or bottom marked.

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