



SLUS549A − DECEMBER 2002 − REVISED SEPTEMBER 2003

# SINGLE-CHIP, LI-ION AND LI-POL CHARGER IC WITH AUTONOMOUS USB-PORT AND AC-ADAPTER SUPPLY MANAGEMENT (bqTINY™-II)

## FEATURES

- **Small 3 mm × 3 mm MLP Package**
- **Charges and Powers Systems from Either AC Adapter or USB With Autonomous Power-Source Selection**
- **Integrated USB Control With Selectable 100 mA and 500 mA Charge Rates**
- **Ideal for Low-Dropout Charger Designs for Single-Cell Li-Ion or Li-Pol Packs in Space Limited Portable Applications**
- **Integrated Power FET and Current Sensor for Up to 1-A Charge Applications From AC Adapter**
- **Precharge Conditioning With Safety Timer**
- **Power Good (AC Adapter Present) Status Output**
- **Optional Battery Temperature Monitoring Before and During Charge**
- **Automatic Sleep Mode for Low-Power Consumption**

## APPLICATIONS

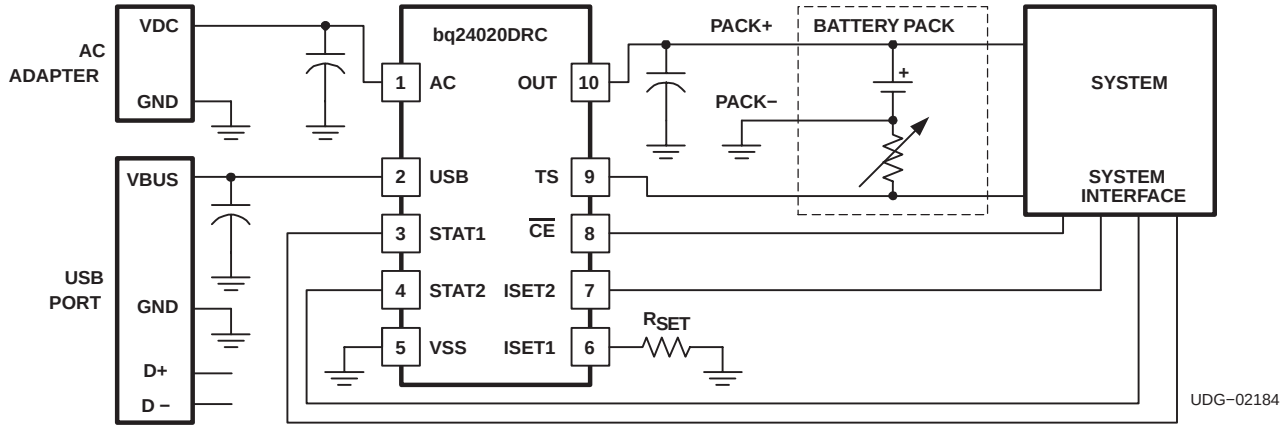
- **PDAs, MP3 Players**
- **Digital Cameras**
- **Internet Appliances**
- **Smartphones**

## DESCRIPTION

The bqTINY-II series are highly integrated and flexible Li-Ion linear charge and system power management devices targeted at space limited charger applications. The bqTINY-II series offer integrated USB-port and ac-adapter supply management with autonomous power-source selection, power FET and current sensor, high-accuracy current and voltage regulation, charge status, and charge termination, in a single monolithic device.

The bqTINY-II automatically selects the USB-Port or the ac-adapter as the power source for the system. In the USB configuration, the host can select from the two preset charge rates of 100 mA and 500 mA. In the ac−adapter configuration an external resistor sets the magnitude of the system or charge current.

The bqTINY-II charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on minimum current. An internal charge timer provides a backup safety for charge termination. The bqTINY-II automatically re-starts the charge if the battery voltage falls below an internal threshold. The bqTINY-II automatically enters sleep mode when both supplies are removed.




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## DESCRIPTION (CONTINUED)

In addition to the standard features, different versions of the bqTINY-II offer a multitude of additional features. These include temperature sensing input for detecting hot or cold battery packs; power good ($\overline{PG}$) output indicating the presence of input power; a TTL-level charge enable input ($\overline{CE}$) used to disable or enable the charge process; and a TTL-level timer and taper−detect enable ($\overline{TTE}$) input used to disable or enable the fast-charge timer and charge termination.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOSFET gates.

## ORDERING INFORMATION

| $T_J$ | CHARGE REGULATION VOLTAGE (V)(1) | OPTIONAL FUNCTIONS(1) | FAST-CHARGE TIMER (Hours) | PART NUMBER(2) | MARKINGS |
|---|---|---|---|---|---|
| −40°C to 125°C | 4.2 | $\overline{CE}$ and TS | 5 | bq24020DRCR | AZS |
| | 4.2 | $\overline{PG}$ and $\overline{CE}$ | 5 | bq24022DRCR | AZU |
| | 4.2 | $\overline{CE}$ and $\overline{TTE}$ | 5 | bq24023DRCR | AZV |
| | 4.2 | $\overline{CE}$ and TS | 7 | bq24025DRCR | AZX |

(1) The DRC package is available taped and reeled only in quantities of 3,000 devices per reel.

## DISSIPATION RATINGS

| PACKAGE | $\theta_{JA}$ | $T_A$ < 40°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C |
|---|---|---|---|
| DRC(1) | 46.87 °C/W | 1.5 W | 0.021 W/°C |

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2x3 via matrix.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | bq24020 bq24022 bq24023 bq24025 | |
|---|---|---|---|
| Input voltage(2) | AC, USB, STAT1, STAT2, TS, $\overline{PG}$, $\overline{CE}$, $\overline{TTE}$, OUT, ISET1, ISET2 | −0.3 to 7.0 | V |
| Output sink/source current | STAT1, STAT2, $\overline{PG}$ | 15 | mA |
| Output current | TS | 200 | µA |
| Output current | OUT | 1.5 | A |
| Operating free−air temperature range, $T_A$ | | −40 to 125 | °C |
| Junction temperature range, $T_J$ | | | |
| Storage temperature, $T_{stg}$ | | −65 to 150 | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 300 | |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to $V_{SS}$.

## RECOMMENDED OPERATING CONDITIONS(1)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage (from AC input), $V_{CC}$ | 4.5 | | 6.5 | V |
| Supply voltage (from USB input), $V_{CC}$ | 4.35 | | 6.5 | V |
| Operating junction temperature range, $T_J$ | −40 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

over $0°C \le T_J \le 125°C$ and recommended supply voltage, unless otherwise noted

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **INPUT CURRENT** | | | | | |
| VCC current, $I_{CC(VCC)}$ | $V_{CC} > V_{CC(min)}$ | | 1.2 | 2.0 | mA |
| Sleep current, $I_{CC(SLP)}$ | Sum of currents into OUT pin, $V_{CC} < V_{(SLP)}$ | | 2 | 5 | µA |
| Standby current, $I_{CC(STBY)}$ | $\overline{CE}$ = High, $0°C \le T_J \le 85°C$ | | | 150 | µA |
| Input current on OUT pin, $I_{IB(OUT)}$ | Charge DONE, $V_{CC} > V_{CC(MIN)}$ | | 1 | 5 | µA |
| Input current on $\overline{CE}$ pin, $I_{IB(CE)}$ | | | | 1 | µA |
| Input bias current on $\overline{TTE}$ pin, $I_{IB(TTE)}$ | | | | 1 | µA |
| **VOLTAGE REGULATION** $V_{O(REG)} + V_{(DO-MAX)} \le V_{CC}$ , $I_{(TERM)} < I_{O(OUT)} \le 1$ A | | | | | |
| Output voltage, $V_{O(REG)}$ | | | 4.20 | | V |
| Voltage regulation accuracy | $T_A$ = 25°C | −0.35% | | 0.35% | |
| | | −1% | | 1% | |
| AC dropout voltage ($V_{(AC)}-V_{(OUT)}$), $V_{(DO)}$ | $V_{O(OUT)} = V_{O(REG)}$, $V_{O(REG)} + V_{(DO-MAX)}) \le V_{CC}$, $I_{O(OUT)}$ = 1A | | 350 | 500 | mV |
| USB dropout voltage ($V_{(USB)} - V_{(OUT)}$), $V_{(DO)}$ | $V_{O(OUT)} = V_{O(REG)}$ $V_{O(REG)} + V_{(DO-MAX)}) \le V_{CC}$, ISET2 = High | | 350 | 500 | mV |
| | $V_{O(OUT)} = V_{O(REG)}$ $V_{O(REG)} + V_{(DO-MAX)}) \le V_{CC}$, ISET2 = Low | | 60 | 100 | mV |
| **CURRENT REGULATION** | | | | | |
| AC output current range, $I_{O(OUT)}$(1) | $V_{I(OUT)} > V_{(LOWV)}$, $V_{I(AC)} - V_{I(OUT)} > V_{(DO-MAX)}$, $V_{CC} \ge$ 4.5 V, | 50 | | 1000 | mA |
| USB output current range, $I_{O(OUT)}$ | $V_{CC(MIN)} \ge$ 4.5 V, $V_{USB} - V_{I(OUT)} > V_{(DO-MAX)}$, $V_{I(OUT)} > V_{(LOWV)}$, ISET2 = Low | 80 | | 100 | mA |
| | $V_{CC(MIN)} \ge$ 4.5 V, $V_{USB} - V_{I(OUT)} > V_{(DO-MAX)}$, $V_{I(OUT)} > V_{(LOWV)}$, ISET2 = High | 400 | | 500 | mA |
| Output current set voltage, $V_{(SET)}$ | Voltage on ISET1 pin, $V_{CC} \ge$ 4.5 V, $V_{IN} \ge$ 4.5 V, $V_{I(OUT)} > V_{(LOWV)}$, $V_{IN} - V_{I(OUT)} > V_{(DO-MAX)}$ | 2.463 | 2.500 | 2.538 | V |
| Output current set factor, $K_{(SET)}$ | 50 mA ≤ $I_{O(OUT)} \le$ 1 A | 307 | 322 | 337 | |
| | 10 mA ≤ $I_{O(OUT)}$ < 50 mA | 296 | 320 | 346 | |
| | 1 mA ≤ $I_{O(OUT)}$ < 10 mA | 246 | 320 | 416 | |
| **PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION** | | | | | |
| Precharge to fast-charge transition threshold, $V_{(LOWV)}$ | Voltage on OUT pin | 2.8 | 3.0 | 3.2 | V |
| Deglitch time for fast-charge to precharge transition | $V_{CC(MIN)} \ge$ 4.5 V, $t_{FALL}$ = 100 ns, 10 mV overdrive $V_{I(OUT)}$ decreasing below threshold | 250 | 375 | 500 | ms |
| Precharge range, $I_{O(PRECHG)}$(2) | 0 V < $V_{I(OUT)}$ < $V_{(LOWV)}$, $t < t_{(PRECHG)}$ | 5 | | 100 | mA |
| Precharge set voltage, $V_{(PRECHG)}$ | Voltage on ISET1 pin, 0 V < $V_{I(OUT)} > V_{(LOWV)}$, $V_{O(REG)}$ = 4.2 V, $t < t_{(PRECHG)}$ | 240 | 255 | 270 | mV |

(1) $$I_{O(OUT)} = \frac{\left(K_{(SET)} \times V_{(SET)}\right)}{R_{SET}}$$

(2) $$I_{O(PRECHG)} = \frac{\left(K_{(SET)} \times V_{(PRECHG)}\right)}{R_{SET}}$$

## ELECTRICAL CHARACTERISTICS (continued)

over $0°C \le T_J \le 125°C$ and recommended supply voltage, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CHARGE TAPER AND TERMINATION DETECTION** | | | | | | |
| Charge taper detection range, $I_{(TAPER)}$(3) | | $V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TAPER)}$ | 5 | | 100 | mA |
| Charge taper detection set voltage, $V_{(TAPER)}$ | | Voltage on ISET1 pin, $V_{O(REG)}$ = 4.2 V, $V_{I(OUT)} > V_{(RCH)}$, $t < t_{(TAPER)}$ | 235 | 250 | 265 | mV |
| Charge termination detection set voltage, $V_{(TERM)}$(4) | | Voltage on ISET pin, $V_{O(REG)}$ = 4.2 V, $V_{I(OUT)} > V_{(RCH)}$ | 11 | 18 | 25 | mV |
| Deglitch time for TAPER detection, $t_{TPRDET}$ | | $V_{CC(MIN)} \ge 4.5$ V, $t_{FALL}$ = 100 ns charging current increasing or decreasing above and below 10 mV overdrive | 250 | 375 | 500 | ms |
| Deglitch time for termination detection, $t_{TRMDET}$ | | $V_{CC(MIN)} \ge 4.5$ V, $t_{FALL}$ = 100 ns charging current decreasing below 10 mV overdrive | 250 | 375 | 500 | ms |
| **TEMPERATURE SENSE COMPARATOR** | | | | | | |
| Low-voltage threshold, $V_{(LTF)}$ | | | 2.475 | 2.500 | 2.525 | V |
| High-voltage threshold, $V_{(HTF)}$ | | | 0.485 | 0.500 | 0.515 | V |
| Current source, $I_{(TS)}$ | | | 96 | 102 | 108 | µA |
| Deglitch time for temperature fault, $t_{(DEGL)}$ | | | 250 | 375 | 500 | ms |
| **BATTERY RECHARGE THRESHOLD** | | | | | | |
| Recharge threshold, $V_{RCH}$ | | | $V_{O(REG)}$ −0.115 | $V_{O(REG)}$ −0.10 | $V_{O(REG)}$ −0.085 | V |
| Deglitch time for recharge detect, $t_{(DEGL)}$ | | $V_{CC(MIN)} \ge 4.5$ V, $t_{FALL}$ = 100 ns decreasing below or increasing above threshold, 10 mV overdrive | 250 | 375 | 500 | ms |
| **STAT1, STAT2, and $\overline{PG}$ OUTPUTS** | | | | | | |
| Low-level output saturation voltage, $V_{OL}$ | | $I_O$ = 5 mA | | | 0.25 | V |
| **CHARGE ENABLE ($\overline{CE}$) AND TIMER AND TERMINATION ENABLE ($\overline{TTE}$) INPUTS** | | | | | | |
| Low-level input voltage, $V_{IL}$ | | $I_{IL}$ = 10 µA | 0 | | 0.4 | V |
| High-level input voltage, $V_{IH}$ | | $I_{IL}$ = 20 µA | 1.4 | | | V |
| $\overline{CE}$ or $\overline{TTE}$ low-level input current, $I_{IL}$ | | | −1 | | | µA |
| $\overline{CE}$ or $\overline{TTE}$ high-level input current, $I_{IH}$ | | | | | 1 | µA |
| ISET2 low-level input current, $I_{IL}$ | | $I_{ISET2}$ = 0 | −20 | | | µA |
| ISET2 high-level input current, $I_{IH}$ | | $I_{ISET2} = V_{CC}$ | | | 40 | µA |
| ISET2 high-Z input current, $I_{IH}$ | | | | | 1 | V |
| **TIMERS** | | | | | | |
| Precharge time, $t_{(PRECHG)}$ | | | 1,620 | 1,800 | 1,930 | s |
| Taper time, $t_{(TAPER)}$ | | | 1,620 | 1,800 | 1,930 | s |
| Charge time, $t_{(CHG)}$ | bq24020 bq24022 bq24023 | | 16,200 | 18,000 | 19,300 | s |
| | bq24025 | | 22,680 | 25,200 | 27,720 | s |
| Timer fault recovery current, $I_{(FAULT)}$ | | | | 200 | | µA |

(3) $$I_{O(TAPER)} = \frac{\left(K_{(SET)} \times V_{(TAPER)}\right)}{R_{SET}}$$

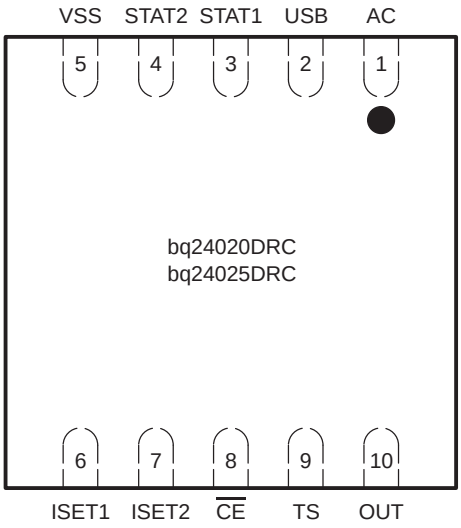
(4) $$I_{O(TERM)} = \frac{\left(K_{(SET)} \times V_{(TERM)}\right)}{R_{SET}}$$

## ELECTRICAL CHARACTERISTICS (continued)

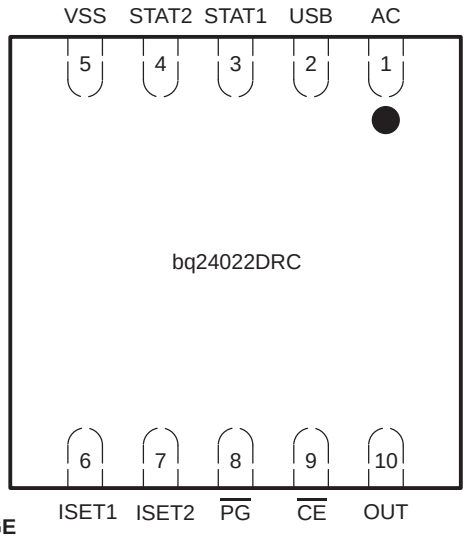
over $0°C \le T_J \le 125°C$ and recommended supply voltage, unless otherwise noted

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **SLEEP COMPARATOR** | | | | | |
| Sleep-mode entry threshold voltage, $V_{(SLP)}$ | $2.3\ V \le V_{I(OUT)} \le V_{O(REG)}$ | | | $V_{CC} \le V_{I(OUT)}$ +80 mV | V |
| Sleep mode exit threshold voltage, $V_{(SLPEXIT)}$ | $2.3\ V \le V_{I(OUT)} \le V_{O(REG)}$ | $V_{CC} \ge V_{I(OUT)}$ +190mV | | | |
| Sleep mode deglitch time | AC and USB decreasing below threshold, $t_{FALL}$ = 100 ns, 10 mV overdrive | 250 | 375 | 500 | ms |
| **THERMAL SHUTDOWN THRESHOLDS** | | | | | |
| Thermal trip threshold, $T_{(SHTDWN)}$ | | | 165 | | °C |
| Thermal hysteresis | | | 15 | | |
| **UNDERVOLTAGE LOCKOUT** | | | | | |
| Undervoltage lockout $V_{(UVLO)}$ | Decreasing $V_{CC}$ | 2.4 | 2.5 | 2.6 | V |
| Hysteresis | | | 27 | | mV |

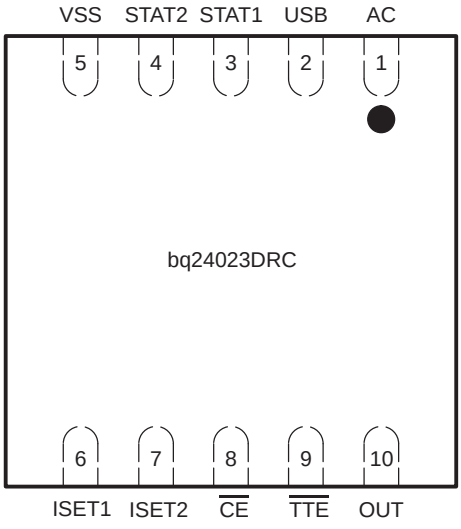
**DRC PACKAGE**
**(TOP VIEW)**




**DRC PACKAGE**
**(TOP VIEW)**



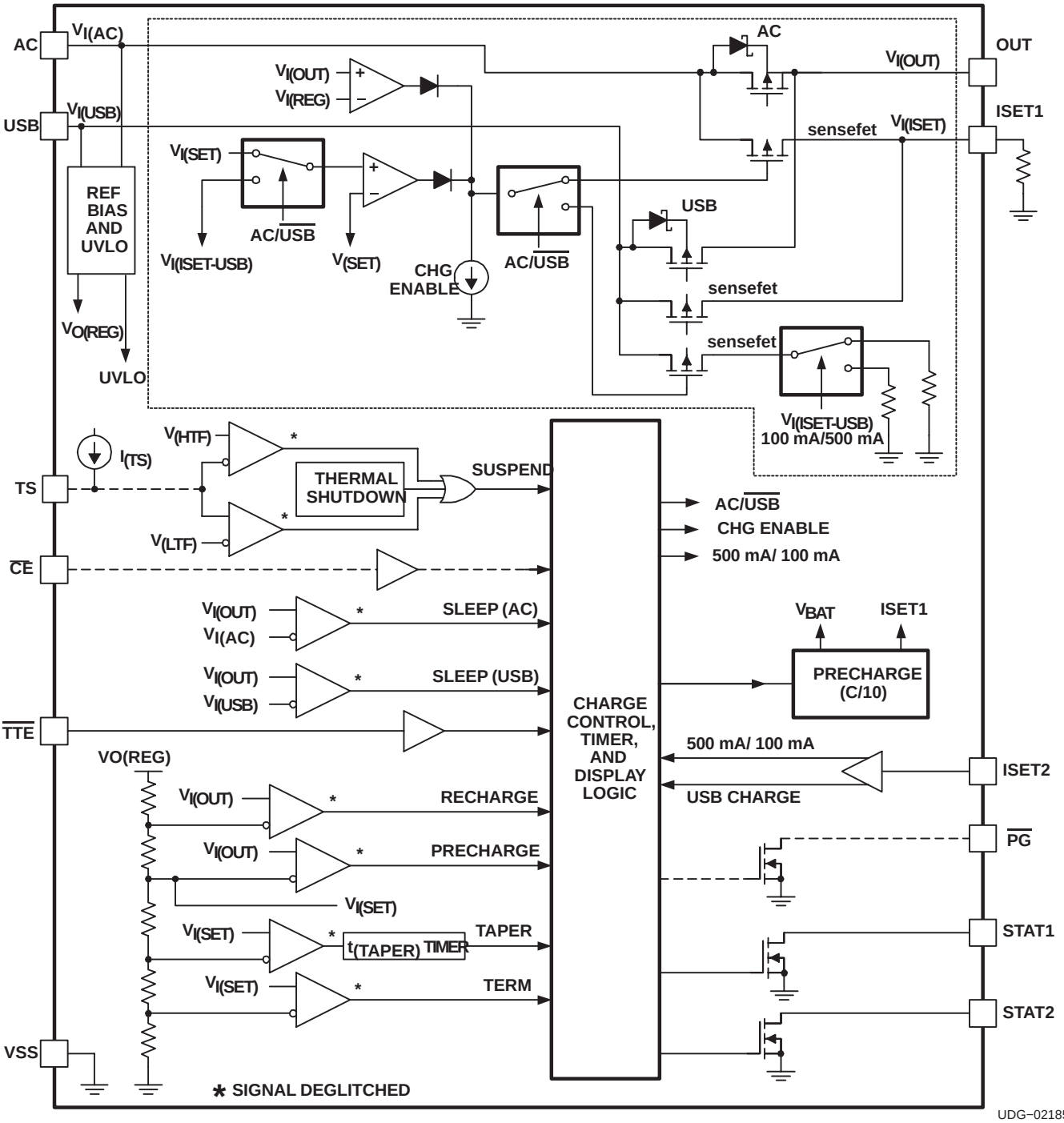

**DRC PACKAGE**
**(TOP VIEW)**



## TERMINAL FUNCTIONS

| NAME | TERMINAL | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| | bq24020 bq24025 | bq24022 | bq24023 | | |
| AC | 1 | 1 | 1 | I | AC charge input voltage |
| $\overline{CE}$ | 8 | 9 | 8 | I | Charge enable input (active low) |
| ISET1 | 6 | 6 | 6 | I | Charge current set point for AC input and precharge and taper set point for both AC and USB |
| ISET2 | 7 | 7 | 7 | I | Charge current set point for USB port (high=500 mA, Low=100 mA, hi-z=disable USB charge) |
| OUT | 10 | 10 | 10 | O | Charge current output |
| $\overline{PG}$ | − | 8 | − | O | Powergood status output (active low) |
| STAT1 | 3 | 3 | 3 | O | Charge status output 1 (open-drain) |
| STAT2 | 4 | 4 | 4 | O | Charge status output 2 (open-drain) |
| TS | 9 | − | − | I | Temperature sense input |
| $\overline{TTE}$ | − | − | 9 | I | Timer and termination enable input (active low) |
| USB | 2 | 2 | 2 | I | USB charge input voltage |
| VSS | 5 | 5 | 5 | − | Ground input |
| Exposed Thermal Pad | pad | pad | pad | − | There is an internal electrical connection between the exposed thermal pad and VSS pin of the device. The exposed thermal pad must be connected to the same potential as the Vss pin on the printed circuit board. **Do not use the thermal pad as the primary ground input for the device.** VSS pin must be connected to ground at all times |

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS

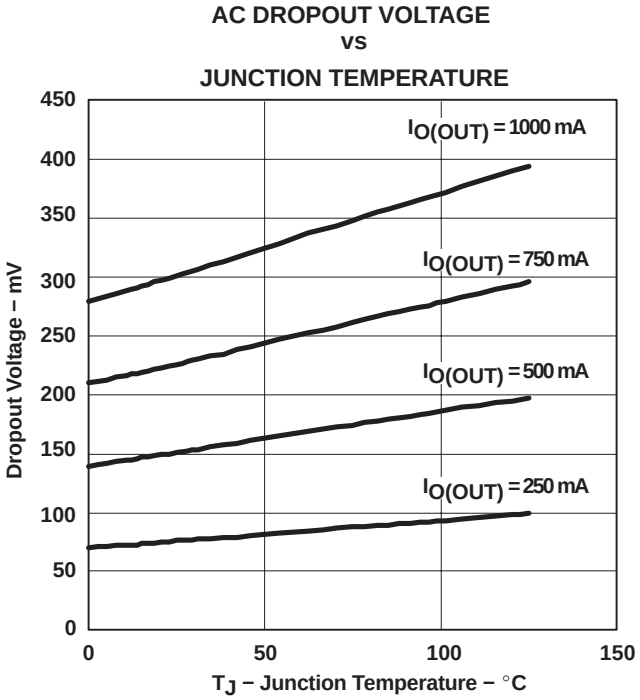



**Figure 1**

The bqTINYII supports a precision Li-Ion, Li-Pol charging system suitable for single-cells. Figure 3 shows a typical charge profile, application circuit and Figure 4 shows an operational flow chart.

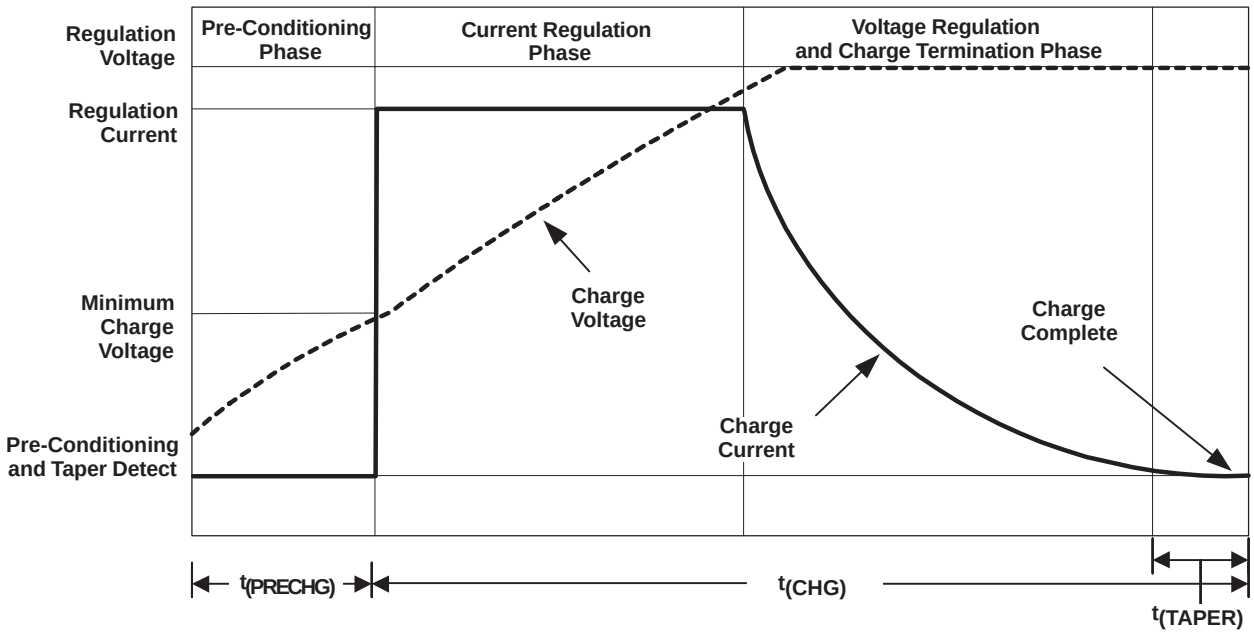



**Figure 2. Typical Charging Profile**

## FUNCTIONAL DESCRIPTION

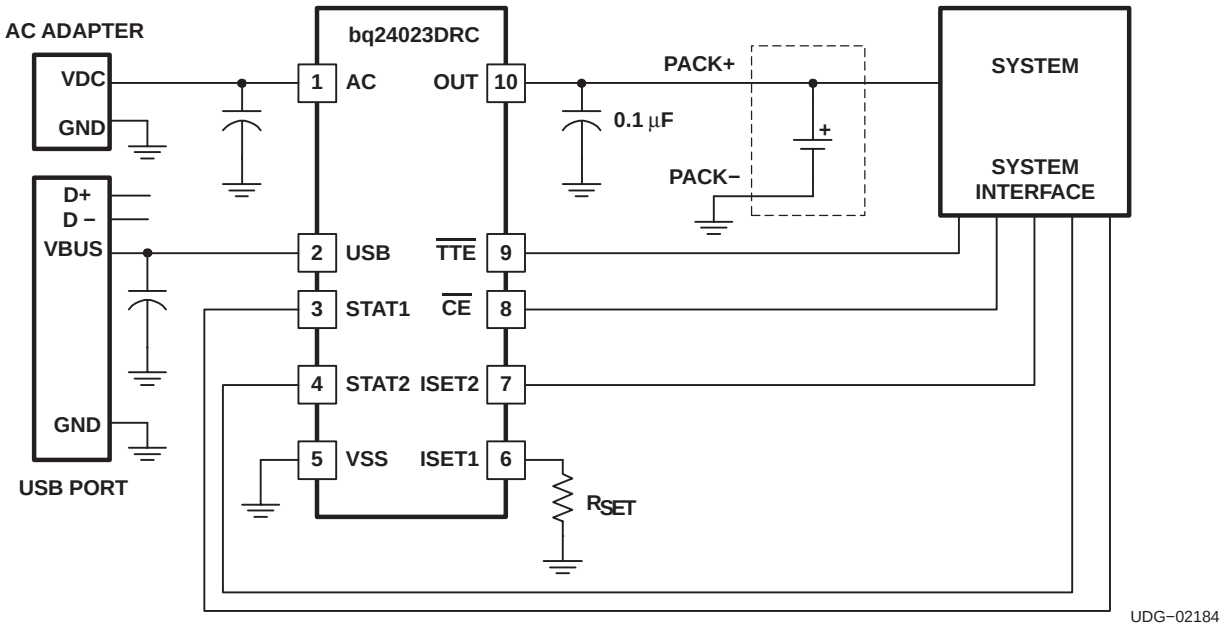



**Figure 3. Typical Application Circuit**

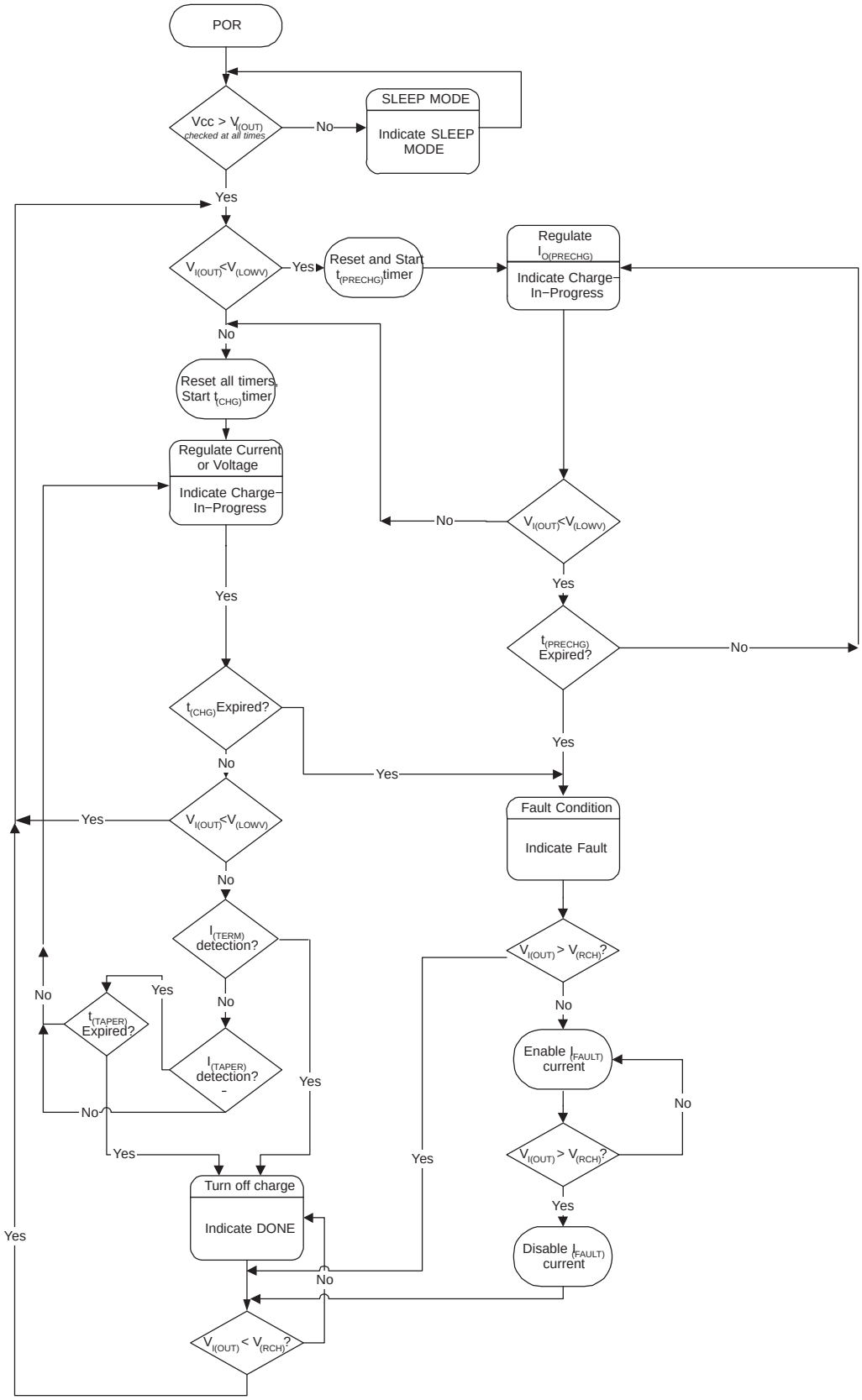



**Figure 4. Operational Flow Chart**

## FUNCTIONAL DESCRIPTION

### AUTONOMOUS POWER SOURCE SELECTION

As default the bqTINY-II attempts to charge from the AC input. If AC input is not present, the USB is selected. If both inputs are available, the AC adapter has the priority. See Figure 5 for details.

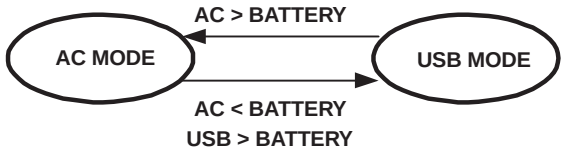



**Figure 5. Typical Charging Profile**

### TEMPERATURE QUALIFICATION (bq24020 only)

The bqTINY-II continuously monitors battery temperature by measuring the voltage between the TS and VSS pins. An internal current source provides the bias for most common 10-kΩ negative-temperature coefficient thermistors (NTC) (see Figure 6). The device compares the voltage on the TS pin against the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected the device immediately suspend the charge. The device suspend charge by turning off the powerFET and holding the timer value (i.e. timers are NOT reset). Charge is resumed when the temperature returns to the normal range.

The allowed temperature range for 103AT type thermistor is 0°C to 45°C. However the user may modify these thresholds by adding two external resistors. See Figure 7.

### BATTERY PRE-CONDITIONING

During a charge cycle if the battery voltage is below the $V_{(LOWV)}$ threshold, the bqTINY-II applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET1 and Vss, $R_{SET}$, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{O\,(PRECHG)} = \frac{V_{(PRECGH)} \times K_{(SET)}}{R_{SET}} \quad (1)$$

The bqTINY-II activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bqTINY-II turns off the charger and enunciates FAULT on the STATx pins. Please refer to the *TIMER FAULT RECOVERY* section for additional details.

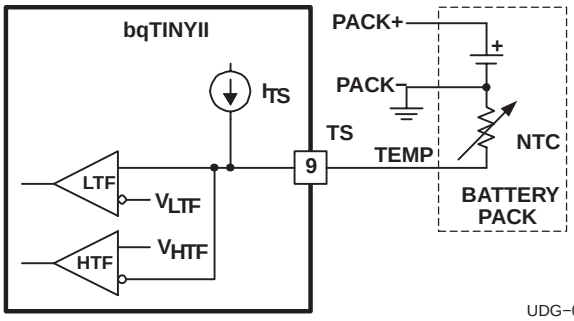



**Figure 6. Temperature Sensing Configuration**

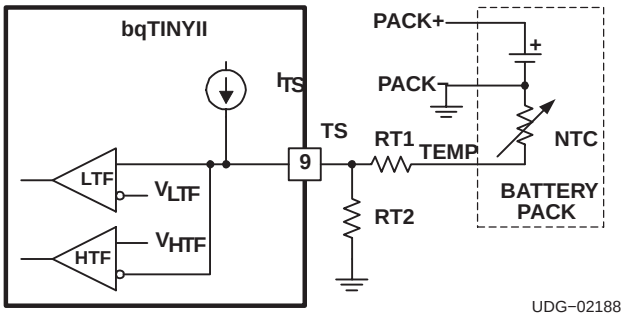



**Figure 7. Temperature Sensing Thresholds**

## FUNCTIONAL DESCRIPTION

### BATTERY CHARGE CURRENT

The bqTINY-II offers on-chip current regulation with programmable set point. The resistor connected between the ISET1 and $V_{SS}$, $R_{SET}$, determines the AC charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}} \quad (2)$$

When charging from a USB port, the host controller has the option of selecting either 100 mA or 500 mA charge rate using ISET2 pin. A low-level signal sets current at 100 mA and a high level signal sets current at 500 mA. A high-Z input disables USB charging

### BATTERY VOLTAGE REGULATION

The voltage regulation feedback is through the OUT pin. This input is tied directly to the positive side of the battery pack. The bqTINY-II monitors the battery−pack voltage between the OUT and VSS pins. When the battery voltage rises to $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

As a safety backup, the bqTINY-II also monitors the charge time in the charge mode. If charge is not terminated within this time period, $t_{(CHG)}$, the bqTINY-II turns off the charger and enunciates FAULT on the STATx pins. Please refer to the *TIMER FAULT RECOVERY* section for additional details.

### CHARGE TAPER DETECTION, TERMINATION AND RECHARGE

The bqTINY-II monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected the bqTINY-II initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The resistor connected between the ISET1 and $V_{SS}$, $R_{SET}$, determines the taper detection level. The $V_{(TAPER)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TAPER)} = \frac{V_{(TAPER)} \times K_{(SET)}}{R_{SET}} \quad (3)$$

The bqTINY-II resets the taper timer in the event that the charge current returns above the taper threshold, $I_{(TAPER)}$.

In addition to the taper current detection, the bqTINY-II terminates charge in the event that the charge current falls below the $I_{(TERM)}$ threshold. This feature allows for quick recognition of a battery removal condition or insertion of a fully charged battery. Note that charge timer and taper timer are bypassed for this feature. The resistor connected between the ISET1 and $V_{SS}$, $R_{SET}$, determines the taper detection level. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}} \quad (4)$$

After charge termination, the bqTINY-II re-starts the charge once the voltage on the OUT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

## FUNCTIONAL DESCRIPTION

### SLEEP MODE

The bqTINY-II enters the low-power sleep mode if both AC and USB are removed from the circuit. This feature prevents draining the battery during the absence of input supply.

### CHARGE STATUS OUTPUTS

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in the following table. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

**Table 1. Status Pins Summary**

| CHARGE STATE | STAT1 | STAT2 |
|---|---|---|
| Precharge in progress | ON | ON |
| Fast charge in progress | ON | OFF |
| Charge done | OFF | ON |
| Charge suspend (temperature) | OFF | OFF |
| Timer fault | OFF | OFF |
| Sleep mode | OFF | OFF |

(†) OFF means the open-drain output transistor on the STAT1 and STAT2 pins is in an off state.

### $\overline{\text{PG}}$ OUTPUT

The open-drain $\overline{\text{PG}}$ (Power Good) indicates when the AC adapter is present. The output turns ON when a valid voltage is detected. This output is turned off in the sleep mode. The $\overline{\text{PG}}$ pin can be used to drive an LED or communicate to the host processor.

### $\overline{\text{CE}}$ INPUT (CHARGE ENABLE)

The $\overline{\text{CE}}$ digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level signal disables the charge and places the device in a low-power mode. A high-to-low transition on this pin also resets all timers and timer fault conditions. Note that this applies to both AC and USB charging.

### $\overline{\text{TTE}}$ INPUT (TIMER AND TERMINATION ENABLE)

The $\overline{\text{TTE}}$ digital input is used to disable or enable the fast-charge timer and charge taper detection. A low-level signal on this pin enables the fast-charge timer and taper timer and a high-level signal disables this feature. Note that this applies to both AC and USB charging.

### THERMAL SHUTDOWN AND PROTECTION

The bqTINY-II monitors the junction temperature, $T_J$, of the die and suspends charging if $T_J$ exceeds $T_{(SHTDWN)}$. Charging resumes when $T_J$ falls below $T_{(SHTDWN)}$ by approximately 15°C.

## FUNCTIONAL DESCRIPTION

### TIMER FAULT RECOVERY

As shown in Figure 4, bqTINY-II provides a recovery method to deal with timer fault conditions. The following summarizes this method:

**Condition #1:** Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs

Recovery method: bqTINY-II waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the bqTINY-II clears the fault and starts a new charge cycle. A POR or $\overline{CE}$ or $\overline{TTE}$ toggle also clears the fault.

**Condition #2:** Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs

Recovery method: Under this scenario, the bqTINY-II applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqTINY-II disables the $I_{(FAULT)}$ current and executes the recovery method described for condition #1. Once the battery falls below the recharge threshold, the bqTINY-II clears the fault and starts a new charge cycle. A POR or $\overline{CE}$ or $\overline{TTE}$ toggle also clears the fault.

## APPLICATION INFORMATION

### THERMAL CONSIDERATIONS

The bqTINY-II is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled, *QFN/SON PCB Attachment Application Note* (TI Literature No. SLUA271).

The most common measure of package thermal performance is thermal impedance ($\theta_{JA}$) measured (or modeled) from the device junction to the air surrounding the package surface (ambient). The mathematical expression for $\theta_{JA}$ is:

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad (5)$$

Where:

- $T_J$ = device junction temperature
- $T_A$ = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of $\theta_{JA}$ include:

- whether or not the device is board mounted
- trace size, composition, thickness, and geometry
- orientation of the device (horizontal or vertical)
- volume of the ambient air surrounding the device under test and airflow
- whether other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation:

$$P = \left(V_{IN} - V_{I(BAT)}\right) \times I_{O(OUT)} \quad (6)$$

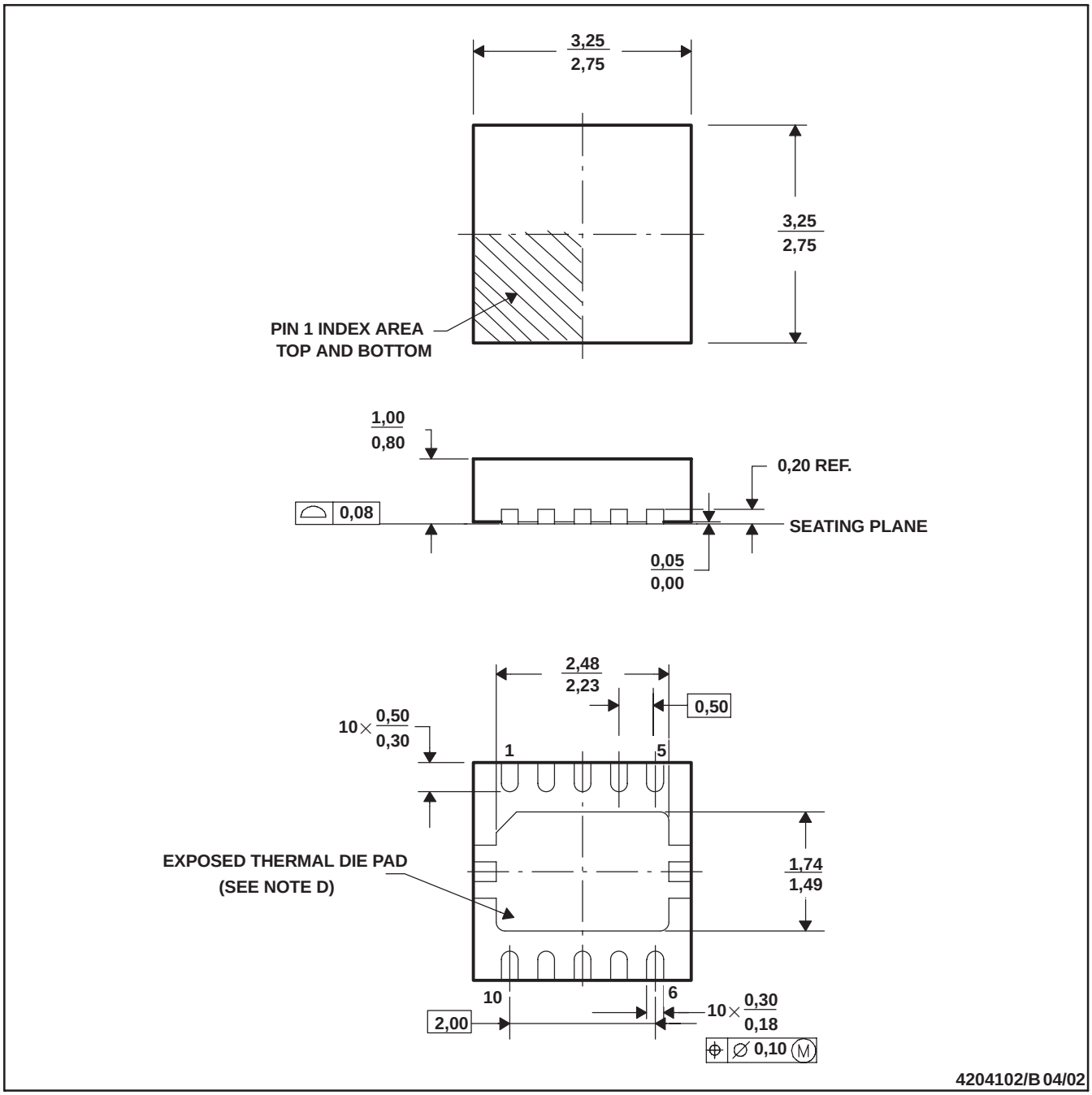
Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at it's lowest. See Figure 2.

### PCB LAYOUT CONSIDERATIONS

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from $V_{CC}$ to $V_{SS}$ and the output filter capacitors from OUT to VSS should be placed as close as possible to the bqTINY, with short trace runs to both signal and $V_{SS}$ pins.
- All low-current $V_{SS}$ connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The BAT pin is the voltage feedback to the device and should be connected with its trace as close to the battery pack as possible.
- The high current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bqTINY-II is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (TI Literature No. SLUA271).

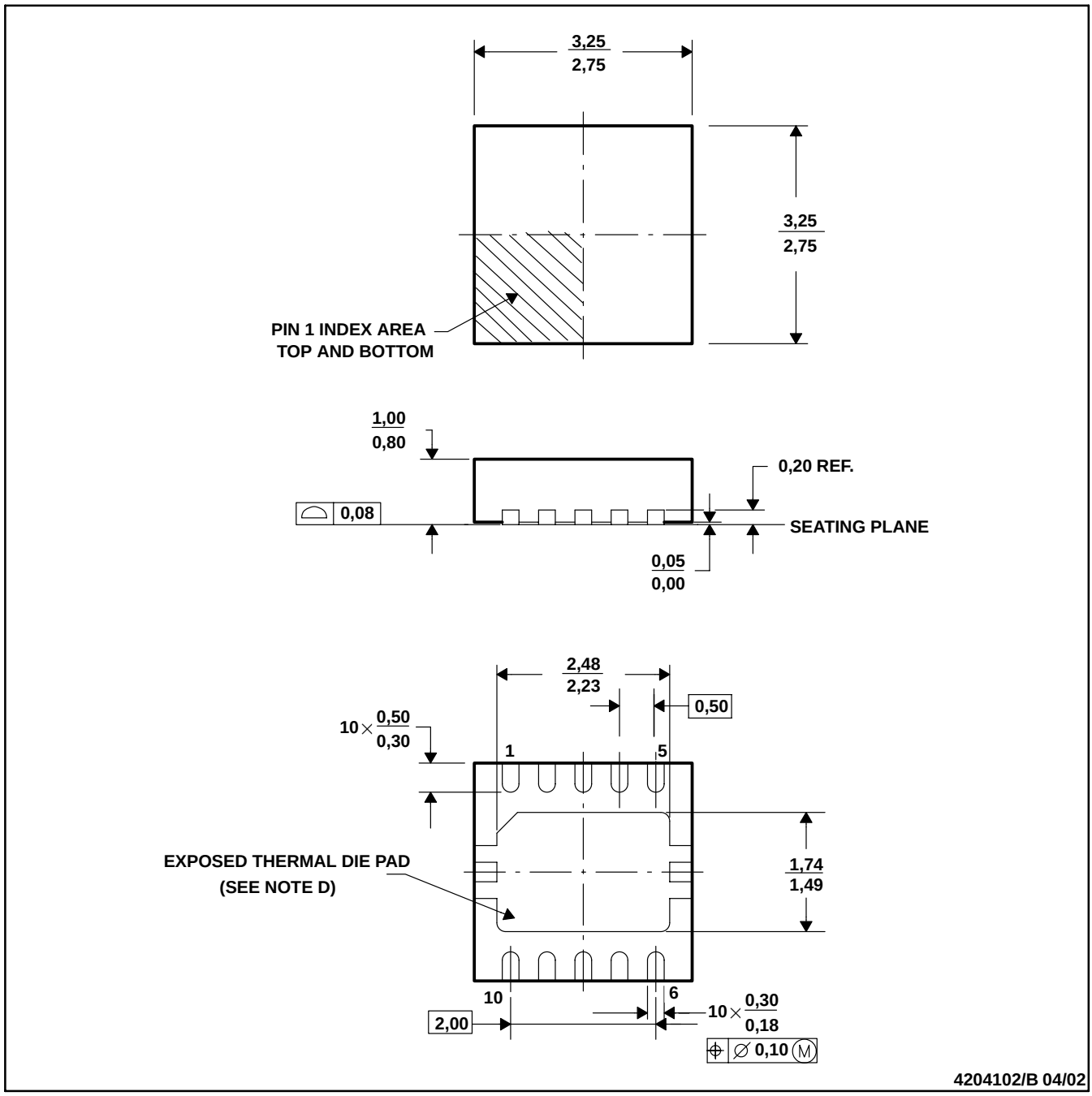
**DRC (S−PDSO−N10)** **CUSTOM DEVICE** **PLASTIC SMALL OUTLINE**




NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.

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