Description

The AP2552/53 and AP2552A/53A are single channel precision adjustable current-limited switches optimized for applications that require precision current limiting, or to provide up to 2.1A of continuous load current during heavy loads/short circuits. These devices offer a programmable current-limit threshold between 75mA and 2.36A (typ) via an external resistor. Current limit accuracy ±6% can be achieved at high current-limit settings. The rise and fall times are controlled to minimize current surges during turn on/off.

The devices have fast short-circuit response time for improved overall system robustness. They provide a complete protection solution for applications subject to heavy capacitive loads and the prospect of short circuit, offering reverse current blocking and limiting, over-current, over-temperature and short-circuit protection, as well as controlled rise time and under-voltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and does not require any external components.

AP2552/53 limits the output current to a safe level when the output current exceeds current-limit threshold.

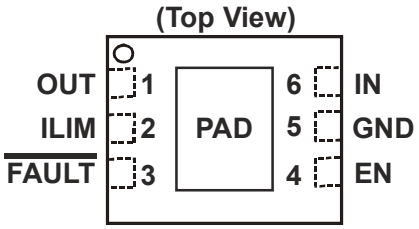
AP2552A/53A provides latch-off function during over-current or reverse-voltage conditions.

All devices are available in SOT26 and U-DFN2020-6 packages.

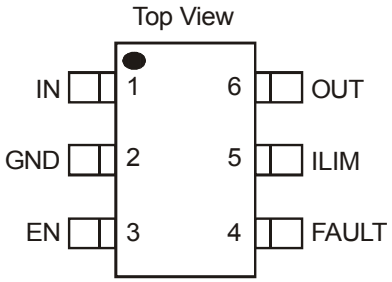
Applications

- Set-Top Boxes
- LCD TVs & Monitors
- Residential Gateways
- Laptops, Desktops, Servers, e-Readers, Printers, Docking Stations, HUBs

Pin Assignments



U-DFN2020-6



SOT26

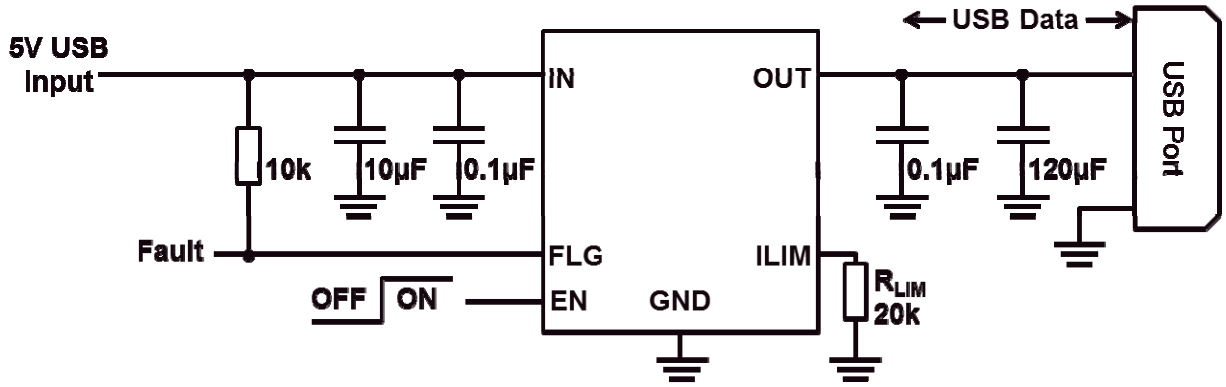
Features

- Up to 2.1A Maximum Load Current
- Accurate Adjustable Current Limit, 75mA - 2360mA
- ±6% Accurate Adjustable Current Limit, 1.63A with R_{LIM} = 15kΩ
- Constant-Current (AP2552/53) During Over-Current
- Output Latch-Off (AP2552A/53A) at Over-Current
- Fast Short-Circuit Response Time: 2μs (typ)
- Reverse Current Blocking During Shutdown and Reverse Current Limiting During Enable
- Operating Range: 2.7V - 5.5V
- Built-in Soft-Start with 3ms Typical Rise Time
- Over-Current , Output Over-Voltage and Thermal Protection
- Fault Report (FAULT) with Blanking Time
- ESD Protection: 2kV HBM, 500V CDM
- Active Low (AP2552/52A) or Active High (AP2553/53A) Enable
- Ambient Temperature Range: -40ºC to +85°C
- SOT26 and U-DFN2020-6 Package: Available in “Green” Molding Compound (No Br, Sb)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- 15kV ESD Protection per IEC 61000-4-2 (with external capacitance)
- UL Recognized, File Number E322375, Vol. 1
- 1IEC60950-1 CB Scheme Certified

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Applications Circuit



120µF Output Capacitance is a Requirement of USB

Available Options

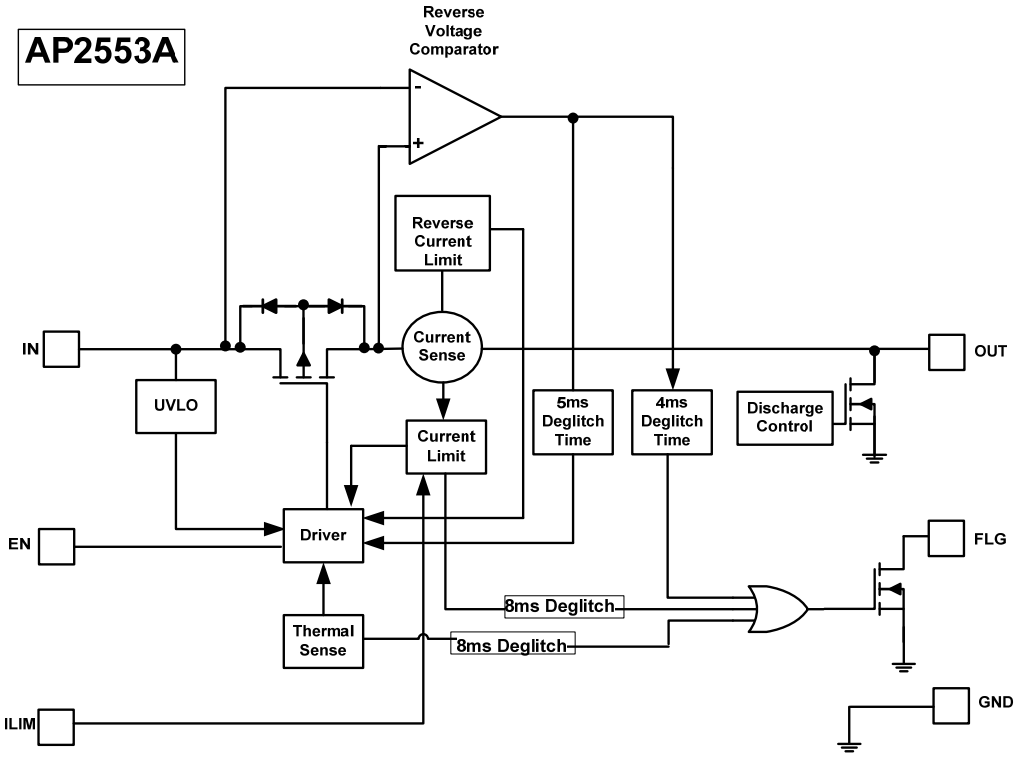
Part Number	Channel	Enable Pin (EN)	Recommended Maximum Continuous Load Current (A)	Current-Limit Protection	Package
AP2552	1	Active Low	2.1	Constant-Current	U-DFN2020-6 SOT26
AP2553	1	Active High			
AP2552A	1	Active Low	2.1	Latch-Off	U-DFN2020-6 SOT26
AP2553A	1	Active High			

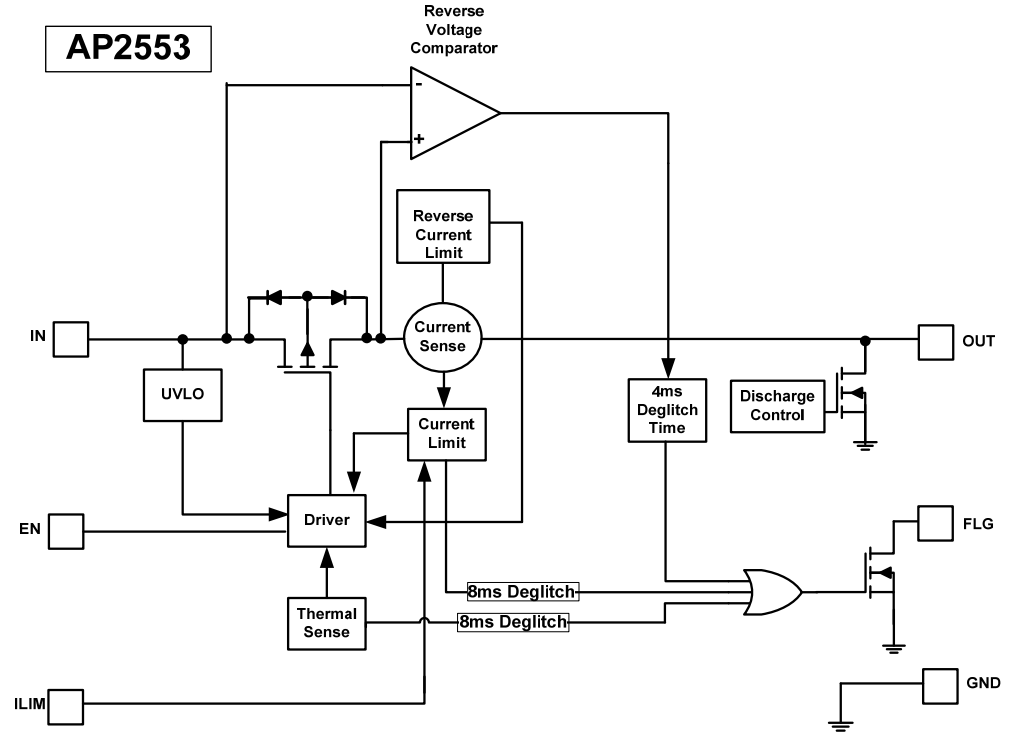
Pin Descriptions

Pin Name	Pin Number				I/O	Function
	AP2552W6-7	AP2553W6-7	AP2552FDC-7	AP2553FDC-7		
IN	1	1	6	6	I	Input, connect a 0.1µF or greater ceramic capacitor from IN to GND as close to IC as possible.
GND	2	2	5	5	—	Ground, connect to external exposed pad.
$\overline{EN}$	3	—	4	—	I	Enable input, logic low turns on power switch.
EN	—	3	—	4	I	Enable input, logic high turns on power switch.
$\overline{FAULT}$	4	4	3	3	O	Active-low open-drain output, asserted during over-current, over-temperature, or reverse-voltage conditions.
ILIM	5	5	2	2	O	Use external resistor to set current-limit threshold; recommended 10kΩ≦RLIM≦232kΩ.
OUT	6	6	1	1	O	Output
Exposed Pad	—	—	Pad	Pad	—	No internal connection; recommend to connect to GND externally for improved power dissipation. It should not be used as electrical ground conduction path.

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Functional Block Diagram





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Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol		Parameter	Ratings	Unit
ESD	HBM	Human Body Model ESD Protection	2	kV
	CDM	Charged Device Model ESD Protection	500	V
	IEC system level	Surges per EN61000-4-2. 1999 Applied to Output Terminals of EVM Note (5)	15	kV
V_{IN}, V_{OUT}, $V_{\overline{FAULT}}$, VILIM, V_{EN}, $V_{\overline{EN}}$		Voltage on IN, OUT, $\overline{FAULT}$, ILIM, EN, $\overline{EN}$	-0.3 to +6.5	V
—		Continuous $\overline{FAULT}$ Sink Current	25	mA
—		ILIM Source Current	1	mA
I_{LOAD}		Maximum Continuous Load Current	Internal Limited	A
$T_{J(MAX)}$		Maximum Junction Temperature	-40 to +150	°C
T_{ST}		Storage Temperature Range (Note 4)	-65 to +150	°C

Notes: 4. UL Recognized Rating from -30°C to +70°C (Diodes qualified T_{ST} from -65°C to +150°C).
5. External capacitors need to be connected to the output, EVM board was tested with capacitor 2.2uF 50V 0805. This level is a pass test only and not a limit.

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Dissipation Rating Table

Board	Package	Thermal Resistance θ_{JA}	Thermal Resistance θ_{JC}	$T_A \le +25°C$ Power Rating	Derating Factor Above T_A = +25°C	T_A = +70°C Power Rating	T_A = +85°C Power Rating
High-K (Note 6)	W6	160°C/W	55°C/W	625mW	6.25mW/°C	340mW	250mW
High-K (Note 6)	FDC	120°C/W	34°C/W	833mW	8.33mW/°C	450mW	330mW

Note: 6. The JEDEC high-K (2s2p) board used to derive this data was a 3in x 3in, multilayer board with 1oz internal power and ground planes with 2oz copper traces on top and bottom of the board.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.7	5.5	V
I_{OUT}	Continuous Output Current (-40°C ≤ T_A ≤ +85°C)	0	2.1	A
V_{EN}, $V_{\overline{EN}}$	Enable Voltage	0	5.5	V
V_{IH}	High-Level Input Voltage on EN or $\overline{EN}$	2.0	V_{IN}	V
V_{IL}	Low-Level Input Voltage on EN or $\overline{EN}$	0	0.8	V
R_{LIM}	Current-Limit Threshold Resistor Range (1% initial tolerance)	10	210	kΩ
I_O	Continuous $\overline{FAULT}$ Sink Current	0	10	mA
––	Input De-Coupling Capacitance, IN to GND	0.1	–	µF
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Operating Junction Temperature	-40	+125	°C

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Electrical Characteristics (@T_A = +25°C, V_{IN} = 2.7V to 5.5V, V_{EN} = 0V or V_{EN} = V_{IN}, R_{FAULT} = 10kΩ, unless otherwise specified.)

Symbol	Parameter	Test Conditions (Note 7)		Min	Typ	Max	Unit
Supply							
V_{UVLO}	Input UVLO	V_{IN} Rising		–	2.4	2.65	V
ΔV_{UVLO}	Input UVLO Hysteresis	V_{IN} Decreasing		–	25	–	mV
I_{SHDN}	Input Shutdown Current	V_{IN} = 5.5V, Disabled, OUT = Open		–	0.1	1	μA
I_Q	Input Quiescent Current	V_{IN} = 5.5V, Enabled, OUT = Open, R_{LIM} = 20kΩ		–	100	140	μA
		V_{IN} = 5.5V, Enabled, OUT = Open, R_{LIM} = 210kΩ		–	80	120	μA
I_{REV}	Reverse Leakage Current	Disabled, V_{IN} = 0V, V_{OUT} = 5.5V, I_{REV} at V_{IN}		–	0.01	1	μA
Power Switch							
$R_{DS(ON)}$	Switch On-Resistance	SOT26 Package,	T_J = +25°C, V_{IN} = 5.0V	–	70	95	mΩ
			-40°C ≤ T_A ≤ +85°C	–	–	135	
		U-DFN2020-6 Package	T_J = +25°C, V_{IN} = 5.0V	–	80	105	
			-40°C ≤ T_A ≤ +85°C	–	–	150	
t_R	Output Turn-On Rise Time	V_{IN} = 5.5V, C_L = 1μF, R_{LOAD} = 100Ω. See Figure 1		–	1.1	1.5	ms
		V_{IN} = 2.7V, C_L = 1μF, R_{LOAD} = 100Ω.		–	0.7	1	ms
t_F	Output Turn-Off Fall Time	V_{IN} = 5.5V, C_L = 1μF, R_{LOAD} = 100Ω. See Figure 1		0.1	–	0.5	ms
		V_{IN} = 2.7V, C_L = 1μF, R_{LOAD} = 100Ω.		0.1	–	0.5	ms
Current Limit							
I_{LIMIT}	Current-Limit Threshold (maximum DC output current), V_{OUT} = V_{IN} -0.5V	R_{LIM} = 10kΩ	-40°C ≤ T_A ≤ +85°C	2200	2365	2542	mA
		R_{LIM} = 15kΩ	-40°C ≤ T_A ≤ +85°C	1540	1632	1730	
		R_{LIM} = 20kΩ	T_J = +25°C	1180	1251	1326	
			-40°C ≤ T_A ≤ +85°C	1160	1251	1340	
		R_{LIM} = 49.9kΩ	T_J = +25°C	500	530	562	
			-40°C ≤ T_A ≤ +85°C	485	529	573	
		R_{LIM} = 210kΩ		121	142	162	
		I_{LIM} Shorted to IN or GND		50	75	100	
I_{SHORT}	Short-Circuit Current Limit, OUT Connected to GND	R_{LIM} = 10kΩ		–	2620	–	mA
		R_{LIM} = 15kΩ		–	1820	–	
		R_{LIM} = 20kΩ		–	1380	–	
		R_{LIM} = 49.9kΩ		–	570	–	
		R_{LIM} = 210kΩ		–	150	–	
		I_{LIM} Shorted to IN or GND		–	75	–	
t_{SHORT}	Short-Circuit Response Time	V_{OUT} = 0V to I_{OUT} = I_{LIMIT} (OUT shorted to ground) See Figure 2		–	2	–	μs
Enable Pin							
$I_{LEAK-EN}$	EN Input Leakage Current	V_{IN} = 5V, V_{EN} = 0V and 6V		-0.5	–	0.5	μA
t_{ON}	Turn-On Time	C_L = 1μF, R_L = 100Ω. See Figure 1		–	–	3	ms
t_{OFF}	Turn-Off Time	C_L = 1μF, R_L = 100Ω. See Figure 1		–	–	1	ms
Output Discharge							
R_{DIS}	Discharge Resistance (Note 8)	V_{IN} = 5V, Disabled, I_{OUT} =1mA		–	600	–	Ω
R_{DIS_LATCH}	Discharge Resistance During Latch-Off	V_{IN} = 5V, Latch-Off, AP2552A/53A Only		–	1000	–	Ω

Notes: 7. Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
8. The discharge function is active when the device is disabled (when enable is de-asserted or during power-up power-down when V_{IN}< V_{UVLO}). The discharge function offers a resistive discharge path for the external storage capacitor for limited time.

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Electrical Characteristics (cont.)

(@T_A = +25°C, V_{IN} = 2.7V to 5.5V, V_{EN} = 0V or V_{EN} = V_{IN}, R_{FAULT} = 10kΩ, unless otherwise specified.)

Symbol	Parameter	Test Conditions (Note 6)	Min	Typ	Max	Unit
Reverse Voltage Protection						
V_{RVP}	Reverse-Voltage Comparator Trip Point	$V_{OUT} - V_{IN}$	95	135	190	mV
IROCP	Reverse Current Limit	$V_{OUT} - V_{IN}$ = 200mV	–	0.72	–	A
t_{TRIG}	Time from Reverse-Voltage Condition to MOSFET Turn Off (AP2552A/AP2553A)	V_{IN} = 5V	3	4.75	7	ms
Fault Flag						
V_{OL}	FAULT Output Low Voltage	I_{FAULT} = 1mA	–	–	180	mV
I_{FOH}	FAULT Off Current	V_{FAULT} = 6V	–	–	1	μA
t_{Blank_OC}	FAULT Blanking and Latch Off Time (Over-Current)	Assertion or deassertion due to overcurrent	5	7.5	10	ms
t_{Blank_RV}	FAULT Blanking Time (Reverse-Voltage)	Assertion or deassertion due to reverse-voltage	2	3.75	6	ms
Thermal Shutdown						
T_{SHDN}	Thermal Shutdown Threshold	Enabled, R_{LOAD} = 1kΩ	–	160	–	°C
T_{SHDN_OCP}	Thermal Shutdown Threshold under Current Limit	Enabled, R_{LOAD} = 1kΩ	–	140	–	°C
T_{HYS}	Thermal Shutdown Hysteresis	–	–	20	–	°C

Typical Performance Characteristics

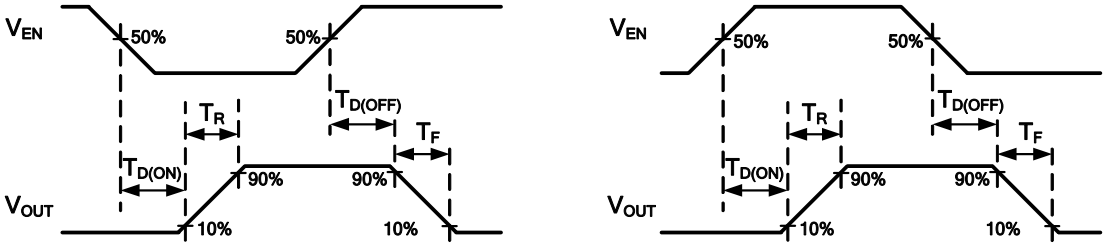


Figure 1 Voltage Waveforms: AP2552/52A (left), AP2553/53A (right)

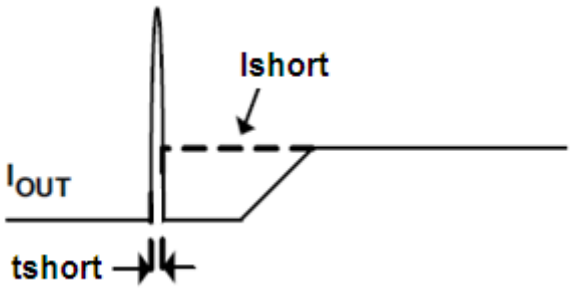
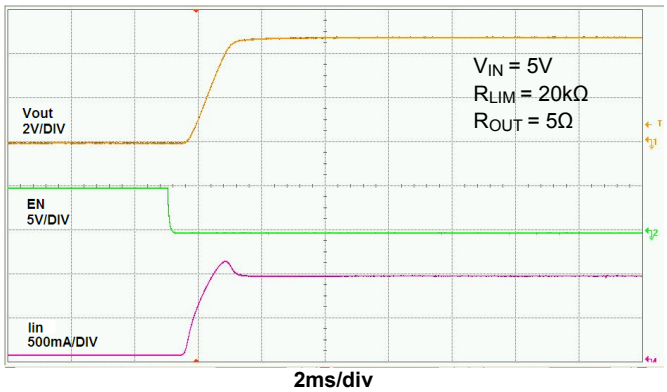


Figure 2 Response Time to Short Circuit Waveform

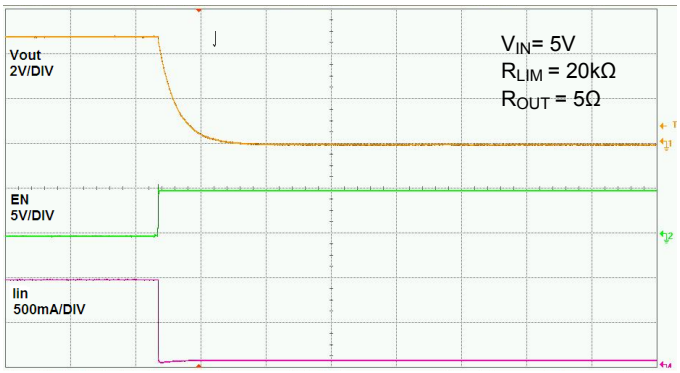
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Typical Performance Characteristics (cont.)



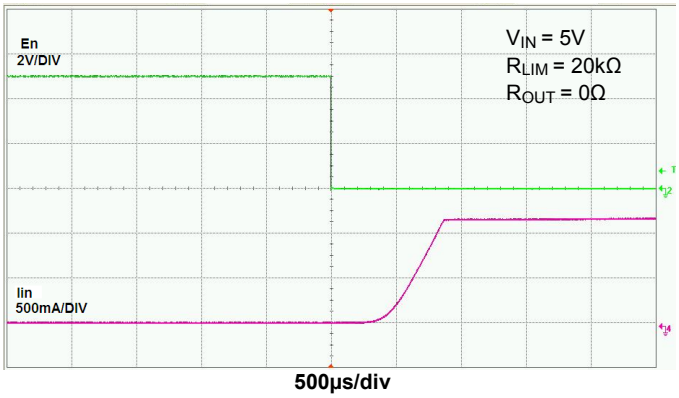
2ms/div

Figure 3 Turn-On Delay and Rise Time



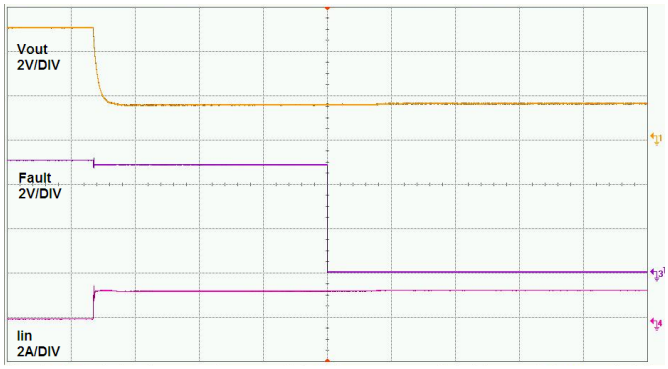
2ms/div

Figure 4 Turn-Off Delay and Fall Time



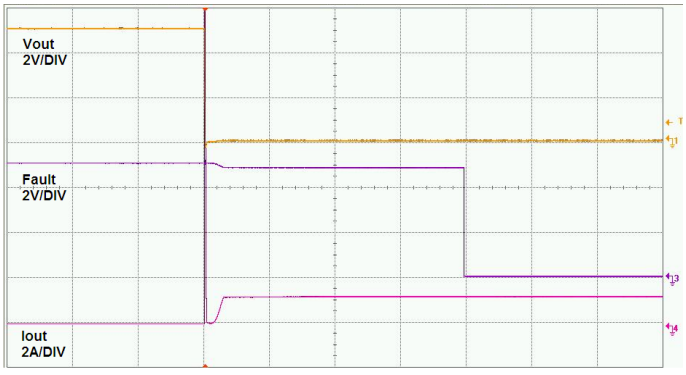
500µs/div

Figure 5 Device Enabled into Short-circuit



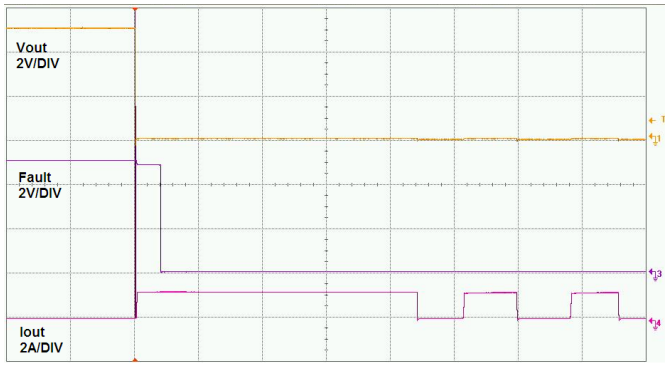
2ms/div

Figure 6 No Load to 1Ω Transient Response



2ms/div

Figure 7 Short-Circuit Current Limit Response

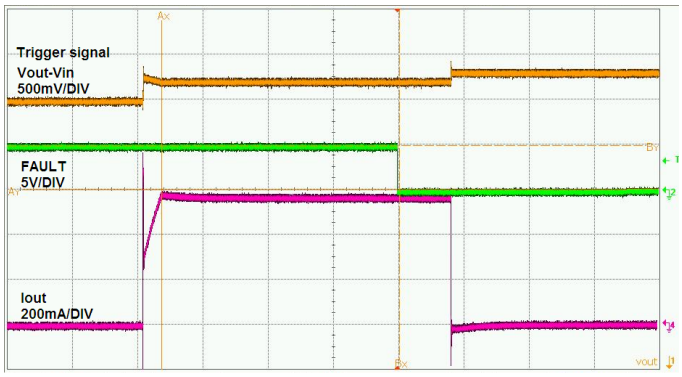


20ms/div

Figure 8 Extended Short-Circuit into Thermal Cycles

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Typical Performance Characteristics (cont.)



1ms/div

Figure 9 Reverse Current Limit Response(AP2552A/AP2553A)

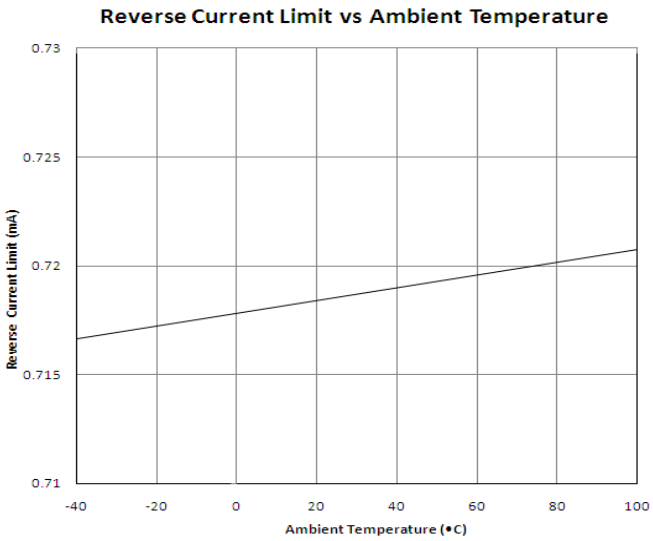


Figure 10 Reverse Current Limit vs. Ambient Temperature

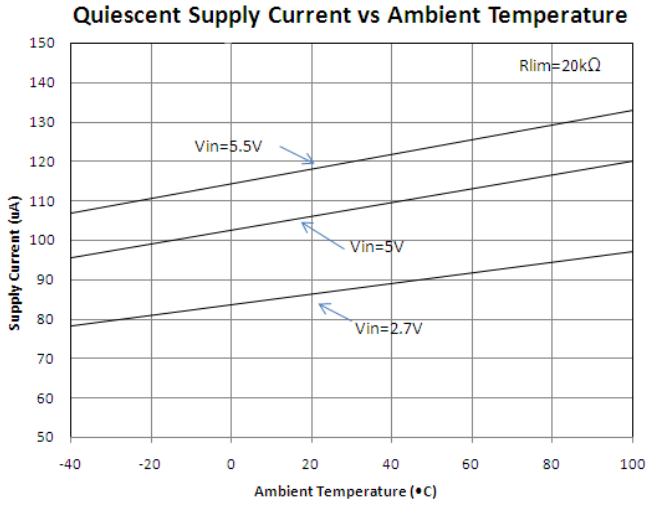


Figure 11 Quiescent Current vs. Ambient Temperature

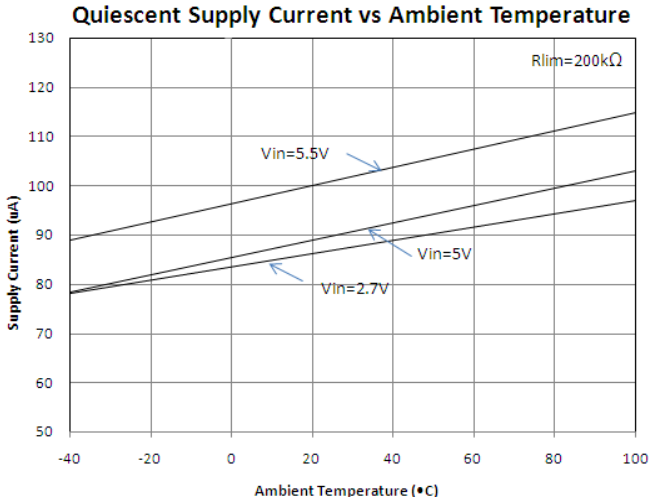


Figure 12 Quiescent Current vs. Ambient Temperature

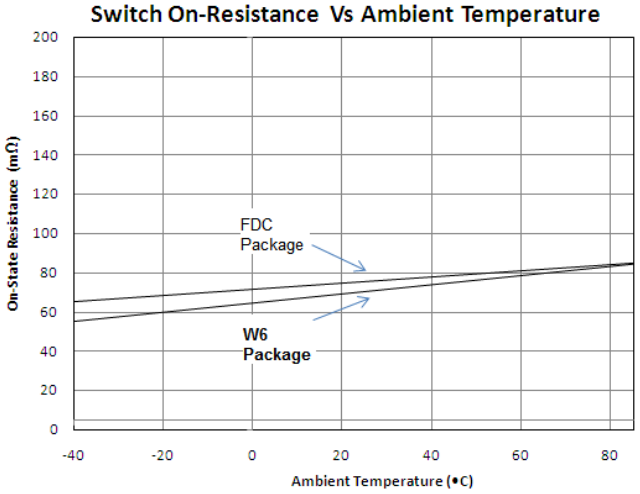


Figure 13 Switch On-Resistance vs. Ambient Temperature

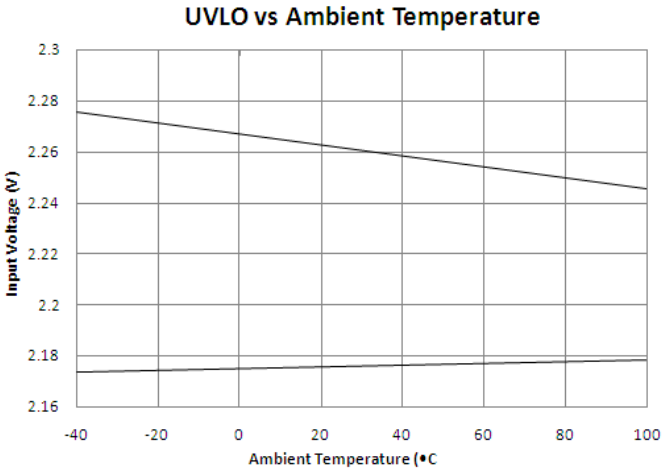


Figure 14 Under-Voltage Lock Out vs. Ambient Temperature

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Application Information

The AP2552/53 AND AP2552A/53A are integrated high-side power switches optimized for Universal Serial Bus (USB) that require protection functions. The power switches are equipped with a driver that controls the gate voltage and incorporates slew-rate limitation. This, along with the various protection features and special functions, makes these power switches ideal for hot-swap or hot-plug applications.

Protection Features:

Under-Voltage Lockout (UVLO)

Whenever the input voltage falls below UVLO threshold (~2.5V), the power switch is turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

Over-Current and Short-Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, AP2552/53 maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

For AP2552A/53A, when an overcurrent condition is detected, the devices will limit the current until the overload condition is removed or the internal deglitch time (7-ms typical) is reached, and AP2552A/53A will be turned off. AP2552A/53A will remain latched off until power is cycled or the device enable is toggled.

The different overload conditions and the corresponding response of the AP2552/53 and AP2552A/53A are outlined below:

NO	Conditions	Explanation	Behavior of the AP2552/53
1	Short-circuit condition at start-up	Output is shorted before input voltage is applied or before the part is enabled	The IC senses the short circuit and immediately clamps output current to a certain safe level namely I_{SHORT}.
2	Short-circuit or overcurrent condition	Short-Circuit or Overload condition that occurs when the part is enabled.	• At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. • After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at I_{SHORT} /I_{LIMIT}.
3	Gradual increase from nominal operating current to I_{LIMIT}	Load increases gradually until the current-limit threshold.(I_{TRIG})	The current rises until I_{LIMIT} or thermal limit. Once the threshold has been reached, the device switches into its current limiting mode and is set at I_{LIMIT}.

NO	Conditions	Explanation	Behavior of the AP2552A/53A
1	Short-circuit condition at start-up	Output is shorted before input voltage is applied or before the part is enabled	The IC senses the short circuit and immediately clamps output current to a certain safe level namely I_{SHORT}. When the internal deglitch time (7-ms typical) is reached and the devices will be turned off.
2	Short-circuit or overcurrent condition	Short-Circuit or Overload condition that occurs when the part is enabled.	• At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. • After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at I_{SHORT} /I_{LIMIT}. When the internal deglitch time (7-ms typical) is reached and the devices will be turned off.
3	Gradual increase from nominal operating current to I_{LIMIT}	Load increases gradually until the current-limit threshold.(I_{TRIG})	The current rises until I_{LIMIT} or thermal limit. Once the threshold has been reached, the device switches into its current limiting mode and is set at I_{LIMIT}. When the internal deglitch time (7-ms typical) is reached and the devices will be turned off.

Over-Current FAULT Signal

The FAULT signal will be asserted in response to OCP before the device reaches its current limit. The output current upon FAULT signal triggered will be lower than the I_limit value. To implement FAULT signal for precision system protection control, it is recommended to leave enough margin from maximum continuous operating current for each RLIM value condition.

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Application Information (cont.)

Current-Limit Threshold Programming

The current-limit threshold can be programmed using an external resistor. The current-limit threshold is proportional to the current sourced out of I_{LIM}.

The recommended 1% resistor range for R_{LIM} is 10kΩ ≤R_{LIM}≤210kΩ. Figure 15 includes current-limit tolerance due to variations caused by temperature and process. This graph does not include the external resistor tolerance. The traces routing the RLIM resistor to the AP2552/53 and AP2552A/53A should be as short as possible to reduce parasitic effects on the current-limit accuracy.

To design below a maximum current-limit threshold, find the intersection of R_{LIM} and the maximum desired load current on the $I_{OS(max)}$ (I_{LIM}) curve and choose a value of R_{LIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{LIM} and the $I_{OS(min)}$ (I_{LIM}) curve.

Best Fit Current-Limit Threshold Equations (I_{LIMIT}):

$$I_{LIM\,(MAX)}(mA) = \frac{20.08}{R_{LIM}^{0.904}\ k\Omega} \qquad I_{LIM(TYP)}(mA) = \frac{19.94}{R_{LIM}^{0.925}\ k\Omega} \qquad I_{LIM(MIN)}(mA) = \frac{20.26}{R_{LIM}^{0.956}\ k\Omega}$$

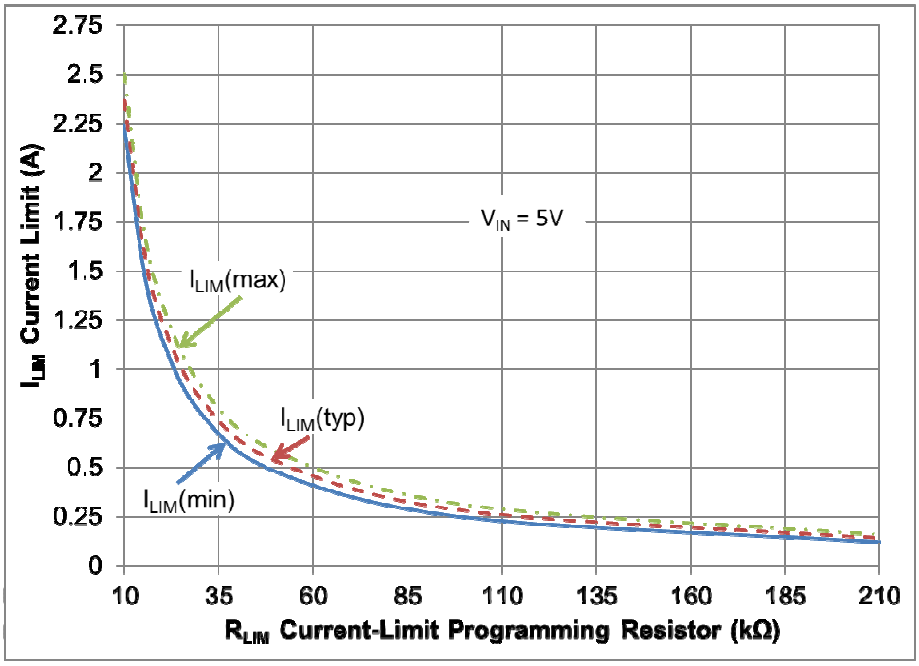


Figure 15 Current-Limit Threshold vs. R_{LIM}

Thermal Protection

Thermal protection prevents the IC from damage when the die temperature exceeds safe margins. This mainly occurs when heavy-overload or short-circuit faults are present for extended periods of time. The AP2552/53 AND AP2552A/53A implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately +160°C (+140°C in case the part is under current limit), the thermal protection feature activates as follows: The internal thermal sense circuitry turns the power switch off and the FAULT output is asserted, thus preventing the power switch from damage. Hysteresis in the thermal sense circuit allows the device to cool down by approximately +20°C before the output is turned back on. This built-in thermal hysteresis feature is an excellent feature, as it avoids undesirable oscillations of the thermal protection circuit. The switch continues to cycle in this manner until the load fault is removed, resulting in a pulsed output.

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Application Information (cont.)

Reverse-Current and Reverse-Voltage Protection

The USB specification does not allow an output device to source current back into the USB port. In a normal MOSFET switch, current will flow in reverse direction (from the output side to the input side) when the output side voltage is higher than the input side. A reverse-current limit **(ROCP)** feature is implemented in the AP2552/53 AND AP2552A/53A to limit such back currents. The ROCP circuit is activated when the output voltage is higher than the input voltage. After the reverse current circuit has tripped (reached the reverse current trip threshold), the current is clamped at this IROCP level.

In addition to ROCP, reverse over-voltage protection (**ROVP**) is also implemented. The ROVP circuit is activated by the ***reverse voltage comparator trip point;*** i.e., the difference between the output voltage and the input voltage.

For AP2552/53, once ROVP is activated, FAULT assertion occurs at a de-glitch time of 4ms. Recovery from ROVP is automatic when the fault is removed. FAULT de-assertion de-glitch time is same as the de-assertion time.

For AP2552A/53A, once ROVP is activated and when the condition exists for more than 5ms (TYP), output device is disabled and shut down. This is called the "Time from Reverse-Voltage Condition to MOSFET Turn Off". FAULT assertion occurs at a de-glitch time of 4ms after ROVP is reached. Recovery from this fault is achieved by recycling power or toggling EN. FAULT de-assertion de-glitch time is same as the de-assertion time.

Special Functions:

Discharge Function

When enable is de-asserted, or when the input voltage is under UVLO level, the discharge function is active. The output capacitor is discharged through an internal NMOS that has a discharge resistance of 100Ω. Hence, the output voltage drops down to zero. The time taken for discharge is dependent on the RC time constant of the resistance and the output capacitor.

FAULT Response

The FAULT open-drain output goes active low for any of following faults: Current limit threshold, short- circuit current limit, reverse-voltage condition or thermal shutdown. The time from when a fault condition is encountered to when the FAULT output goes low is 7ms (TYP). The FAULT output remains low until over-current, short-circuit current limit and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FAULT due to the 7ms deglitch timeout. This 7-ms timeout is also applicable for over-current recovery and over-temperature recovery. The AP2552/53 and AP2552-2/53A are designed to eliminate erroneous over-current reporting without the need for external components, such as an RC delay network.

For the AP2552/53 and AP2552A/53A when the reverse voltage condition is triggered, FAULT output goes low after 4ms (TYP). This 4ms (TYP) timeout is also applicable for the recovery from reverse voltage fault.

When the ILIM pin is shorted to IN or GND, current-limit threshold and short-circuit current limit will be clamped at typically 75mA. When the ILIM pin is shorted to IN or GND, the AP2552/53 and AP2552A/53A FAULT pin will not assert during current limiting conditions; The FAULT pin will assert during short circuit conditions.

Power Supply Considerations

A 0.01-µF to 0.1-µF X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. This limits the input voltage drop during line transients. Placing a high-value electrolytic capacitor on the input (10µF minimum) and output pin (120µF) is recommended when the output load is heavy. This precaution also reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the device output with a 0.1µF to 4.7µF ceramic capacitor improves the immunity of the device to short-circuit transients. This capacitor also prevents output from going negative during turn-off due to parasitic inductance.

Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature (T_A) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

T_A = Ambient temperature °C
θ_{JA} = Thermal resistance
P_D = Total power dissipation

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Application Information (cont.)

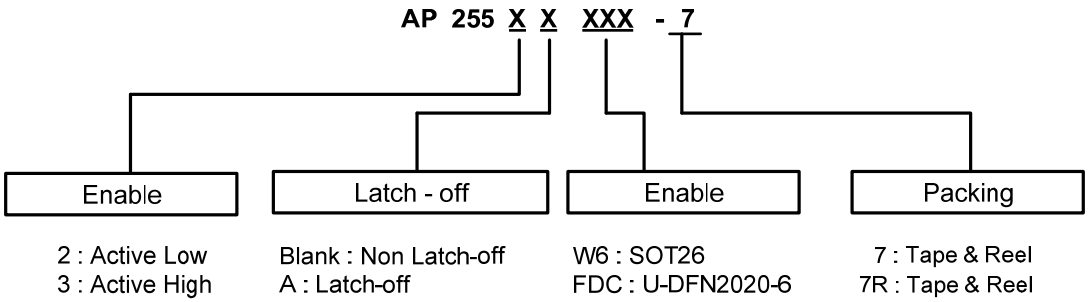
Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise and fall times of the AP2552/53 AND AP2552A/53A, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2552/53 AND AP2552A/53A also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

Generic Hot-Plug Applications

By placing the AP2552/53 AND AP2552A/53A between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.

Ordering Information



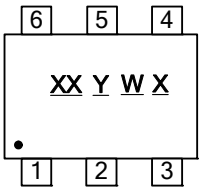
Part Number	Enable Active	Output Fault Condition	Package Code	Packaging	7" Tape and Reel	
					Quantity	Part Number Suffix
AP2552W6-7	Low	Output Current Limits	W6	SOT26	3000/Tape & Reel	-7
AP2552W6-7R			W6	SOT26	3000/Tape & Reel	-7R
AP2552FDC-7			FDC	U-DFN2020-6	3000/Tape & Reel	-7
AP2552FDC-7R			FDC	U-DFN2020-6	3000/Tape & Reel	-7R
AP2553W6-7	High		W6	SOT26	3000/Tape & Reel	-7
AP2553W6-7R			W6	SOT26	3000/Tape & Reel	-7R
AP2553FDC-7			FDC	U-DFN2020-6	3000/Tape & Reel	-7
AP2553FDC-7R			FDC	U-DFN2020-6	3000/Tape & Reel	-7R
AP2552AW6-7	Low	Output Latches Off	W6	SOT26	3000/Tape & Reel	-7
AP2552AW6-7R			W6	SOT26	3000/Tape & Reel	-7R
AP2552AFDC-7			FDC	U-DFN2020-6	3000/Tape & Reel	-7
AP2552AFDC-7R			FDC	U-DFN2020-6	3000/Tape & Reel	-7R
AP2553AW6-7	High		W6	SOT26	3000/Tape & Reel	-7
AP2553AW6-7R			W6	SOT26	3000/Tape & Reel	-7R
AP2553AFDC-7			FDC	U-DFN2020-6	3000/Tape & Reel	-7
AP2553AFDC-7R			FDC	U-DFN2020-6	3000/Tape & Reel	-7R

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Marking Information

(1) SOT26

(Top View)

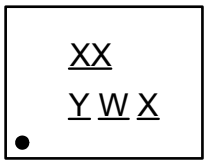


XX : Identification Code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Device	Package	Identification Code
AP2552W6-7	SOT26	BJ
AP2552W6-7R	SOT26	BJ
AP2553W6-7	SOT26	BK
AP2553W6-7R	SOT26	BK
AP2552AW6-7	SOT26	BM
AP2552AW6-7R	SOT26	BM
AP2553AW6-7	SOT26	BN
AP2553AW6-7R	SOT26	BN

(2) U-DFN2020-6

(Top View)



XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

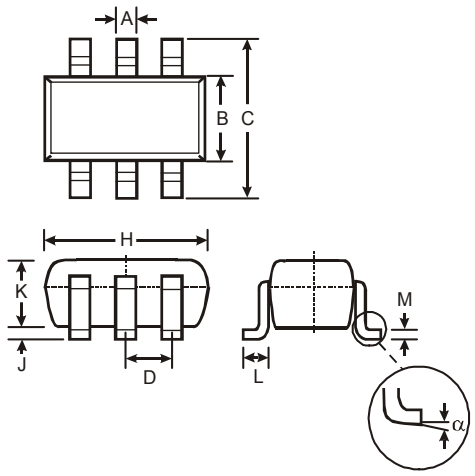
Device	Package	Identification Code
AP2552FDC-7	U-DFN2020-6	BJ
AP2552FDC-7R	U-DFN2020-6	BJ
AP2553FDC-7	U-DFN2020-6	BK
AP2553FDC-7R	U-DFN2020-6	BK
AP2552AFDC-7	U-DFN2020-6	BM
AP2552AFDC-7R	U-DFN2020-6	BM
AP2553AFDC-7	U-DFN2020-6	BN
AP2553AFDC-7R	U-DFN2020-6	BN

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Package Outline Dimensions (All dimensions in mm.)

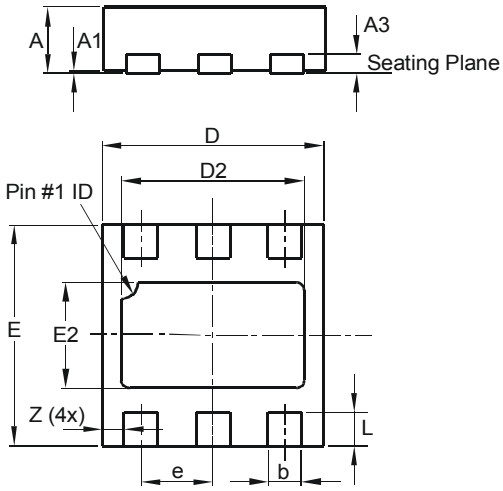
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

(1) Package Type: SOT26



SOT26			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	—	—	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
α	0°	8°	—
All Dimensions in mm			

(2) Package Type: U-DFN2020-6



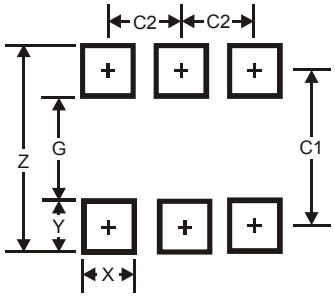
U-DFN2020-6 Type C			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	—	—	0.15
b	0.25	0.35	0.30
D	1.95	2.075	2.00
D2	1.55	1.75	1.65
E	1.95	2.075	2.00
E2	0.86	1.06	0.96
e	—	—	0.65
L	0.25	0.35	0.30
Z	—	—	0.20
All Dimensions in mm			

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Suggested Pad Layout

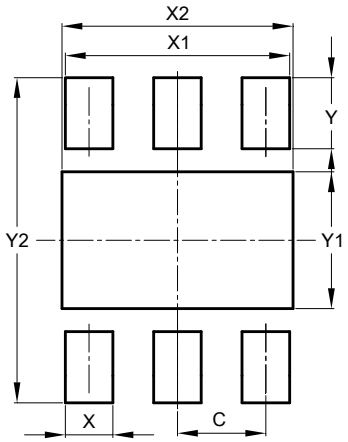
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(1) Package Type: SOT26



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

(2) Package Type: U-DFN2020-6

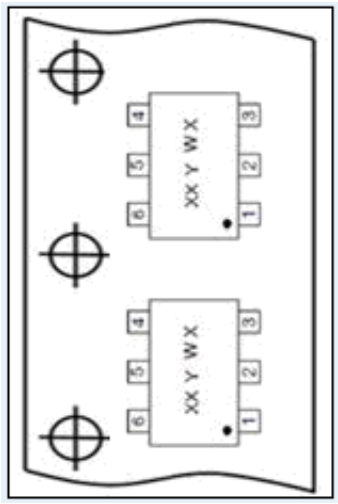


Dimensions	Value (in mm)
C	0.650
X	0.350
X1	1.650
X2	1.700
Y	0.525
Y1	1.010
Y2	2.400

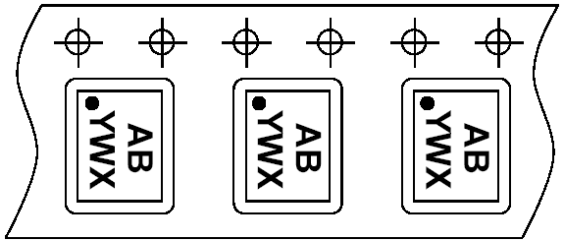
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Taping Orientation (Note 11)

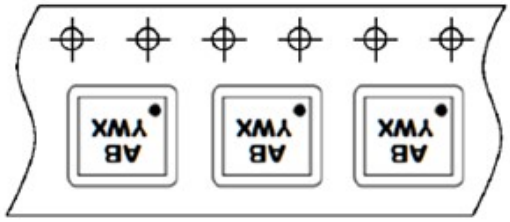
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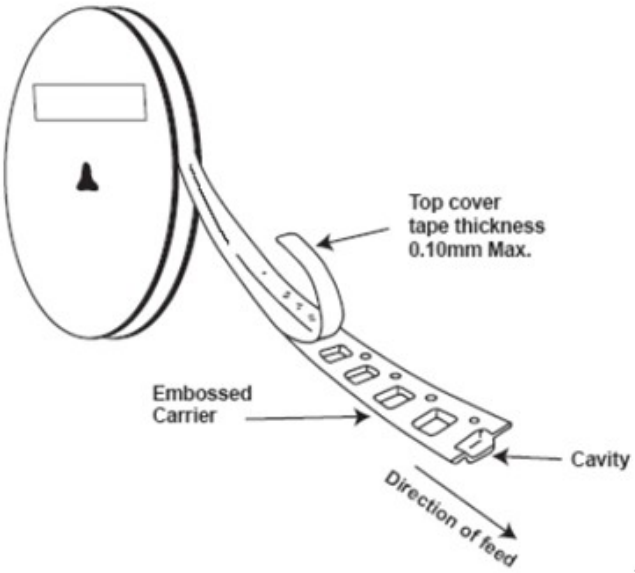


(2) Package Type (-7) : U-DFN2020-6



(3) Package Type (-7R) : U-DFN2020-6





Note: 11. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf.

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