1-4 Cell Li+ Battery SMBus Charge Controller With Independent Comparator and Advanced Circuit Protection

Check for Samples: bq24707, bq24707A

FEATURES

- **SMBus Host-Controlled NMOS-NMOS Synchronous Buck Converter with Programmable 615kHz, 750kHz, and 885kHz Switching Frequency**
- **Real Time System Control on ILIM Pin to Limit Charge Current**
- **Enhanced Safety Features for Over Voltage Protection, Over Current Protection, Battery, Inductor, and MOSFET Short Circuit Protection**
- **Programmable Input Current, Charge Voltage, Charge Current Limits**
  - **±0.5% Charge Voltage Accuracy up to 19.2V**
  - **±3% Charge Current Accuracy up to 8.128A**
  - **±3% Input Current Accuracy up to 8.064A**
  - **±2% 20x Adapter Current or Charge Current Output Accuracy**
- **Programmable Adapter Detection and Indicator**
- **Independent Comparator with Internal Reference**
- **Integrated Soft Start**
- **Integrated Loop Compensation**
- **AC Adapter Operating Range 5V-24V**
- **15μA Off-State Battery Discharge Current**
- **20-pin 3.5 x 3.5 mm^2 QFN Package**
- **bq24707: $\overline{\text{ACOK}}$ delay default 1.3s**
- **bq24707A: $\overline{\text{ACOK}}$ delay default 1.2ms**

APPLICATIONS

- **Portable Notebook Computers, UMPC, Ultra-Thin Notebook, and Netbook**
- **Personal Digital Assistant**
- **Handheld Terminal**
- **Industrial and Medical Equipment**
- **Portable Equipment**

DESCRIPTION

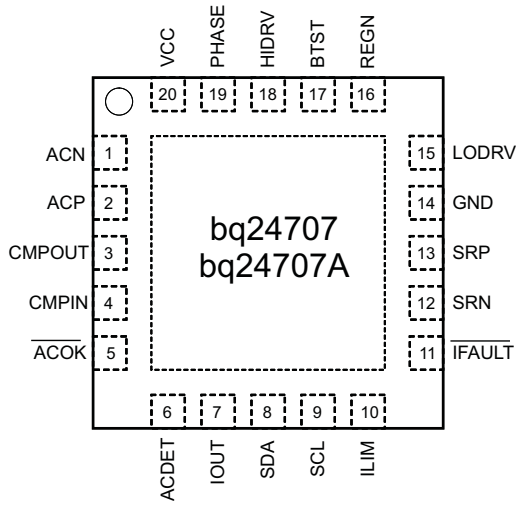
The bq24707 and bq24707A are high-efficiency, synchronous battery charger, offering low component count for space-constraint, multi-chemistry battery charging applications.

SMBus controlled input current, charge current, and charge voltage DACs allow for very high regulation accuracies that can be easily programmed by the system power management micro-controller.

The IC uses the internal input current register or external ILIM pin to throttle down PWM modulation to reduce the charge current.

The IC provides an $\overline{\text{IFAULT}}$ output to alarm if any MOSFET fault or input over current occurs. This alarm output allows users to turn off input power selectors when the fault occurs. Meanwhile, an independent comparator with internal reference is available to monitor input current, output current, or output voltage.

The IC charges one, two, three, or four series Li+ cells, and is available in a 20-pin, 3.5×3.5 mm^2 QFN package.



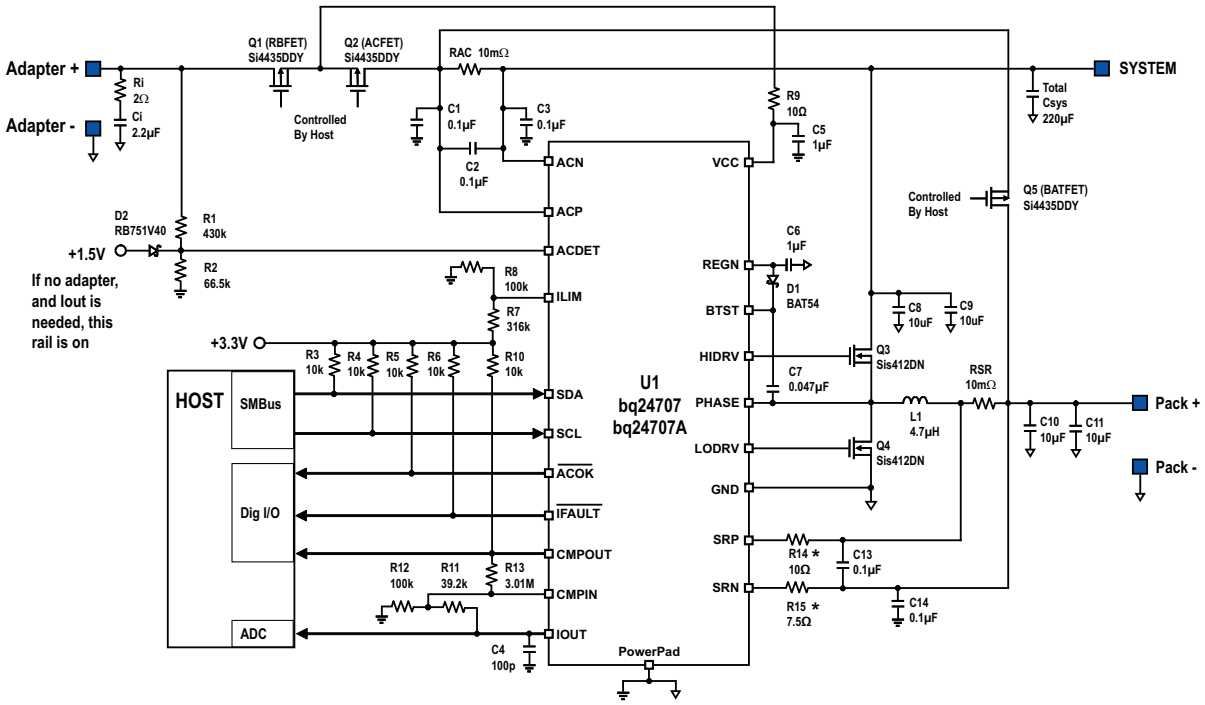
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION



F_s = 750kHz, I_{adpt} = 4.096A, I_{chrg} = 2.944A, I_{lim} = 4A, V_{chrg} = 12.592V, 90W adapter and 3S2P battery pack

See the application information about negative output voltage protection for hard shorts on battery to ground or battery reverse connection.

Figure 1. Typical System Schematic

ORDERING INFORMATION

PART NUMBER	IC MARKING	PACKAGE	ORDERING NUMBER (Tape and Reel)	QUANTITY
bq24707	BQ707	20-PIN 3.5 x 3.5mm^2 QFN	bq24707RGRR	3000
			bq24707RGRT	250
bq24707A	BQ07A	20-PIN 3.5 x 3.5mm^2 QFN	bq24707ARGRR	3000
			bq24707ARGRT	250

COMPARISON TABLE

Condition	bq24707	bq24707A
$\overline{\text{ACOK}}$ default delay	1.3s	1.2ms
Suggest fully charged battery ChargeVoltage() setting after termination	full scale charge voltage(12.592V for 3S battery)	0V
Suggest fully charged battery ChargeCurrent() setting after termination	0A	0A

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE	UNIT
Voltage range	SRN, SRP, ACN, ACP, VCC	–0.3 to 30	V
	PHASE	–2 to 30	
	ACDET, SDA, SCL, LODRV, REGN, IOUT, ILIM, $\overline{ACOK}$, $\overline{IFAULT}$, CMPIN, CMPOUT	–0.3 to 7	
	BTST, HIDRV	–0.3 to 36	
Maximum difference voltage	SRP–SRN, ACP–ACN	–0.5 to 0.5	
Junction temperature range, T_J		–40 to 155	°C
Storage temperature range, T_{stg}		–55 to 155	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

THERMAL INFORMATION

THERMAL METRIC(1)		bq24707/bq24707A	UNITS
		RGR	
		20 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	46.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	15.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage range	SRN, SRP, ACN, ACP, VCC	0		24	V
	PHASE	–2		24	
	ACDET, SDA, SCL, LODRV, REGN, IOUT, ILIM, $\overline{ACOK}$, $\overline{IFAULT}$, CMPIN, CMPOUT	0		6.5	
	BTST, HIDRV	0		30	
Maximum difference voltage	SRP–SRN, ACP–ACN	–0.2		0.2	V
Junction temperature range, T_J		0		125	°C
Storage temperature range, T_{stg}		–55		150	°C

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ELECTRICAL CHARACTERISTICS

4.5 V ≤ $V_{(VCC)}$ ≤ 24 V, 0°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{VCC_OP}	VCC Input voltage operating range		4.5		24	V
CHARGE VOLTAGE REGULATION						
$V_{BAT_REG_RNG}$	BAT voltage regulation range		1.024		19.2	V
$V_{BAT_REG_ACC}$	Charge voltage regulation accuracy	ChargeVoltage() = 0x41A0H	16.716	16.8	16.884	V
			–0.5%		0.5%	
		ChargeVoltage() = 0x3130H	12.529	12.592	12.655	V
			–0.5%		0.5%	
		ChargeVoltage() = 0x20D0H	8.350	8.4	8.450	V
			–0.6%		0.6%	
		ChargeVoltage() = 0x1060H	4.163	4.192	4.221	V
			–0.7%		0.7%	
CHARGE CURRENT REGULATION						
$V_{IREG_CHG_RNG}$	Charge current regulation differential voltage range	$V_{IREG_CHG} = V_{SRP} - V_{SRN}$	0		81.28	mV
$I_{CHRG_REG_ACC}$	Charge current regulation accuracy 10mΩ current sensing resistor	ChargeCurrent() = 0x1000H	3973	4096	4219	mA
			–3%		3%	
		ChargeCurrent() = 0x0800H	1946	2048	2150	mA
			–5%		5%	
		ChargeCurrent() = 0x0200H	410	512	614	mA
			–20%		20%	
		ChargeCurrent() = 0x0100H	172	256	340	mA
			–33%		33%	
		ChargeCurrent() = 0x0080H	64	128	192	mA
			–50%		50%	
INPUT CURRENT REGULATION						
$V_{IREG_DPM_RNG}$	Input current regulation differential voltage range	$V_{IREG_DPM} = V_{ACP} – V_{ACN}$	0		80.64	mV
$I_{DPM_REG_ACC}$	Input current regulation accuracy 10mΩ current sensing resistor	InputCurrent() = 0x1000H	3973	4096	4219	mA
			–3%		3%	
		InputCurrent() = 0x0800H	1946	2048	2150	mA
			–5%		5%	
		InputCurrent() = 0x0400H	870	1024	1178	mA
			–15%		15%	
		InputCurrent() = 0x0200H	384	512	640	mA
			–25%		25%	
INPUT CURRENT OR CHARGE CURRENT SENSE AMPLIFIER						
V_{ACP/N_OP}	Input common mode range	Voltage on ACP/ACN	4.5		24	V
V_{SRP/N_OP}	Output common mode range	Voltage on SRP/SRN	0		19.2	V
V_{IOUT}	IOUT output voltage range		0		1.6	V
I_{IOUT}	IOUT output current		0		1	mA
A_{IOUT}	Current sense amplifier gain	$V_{(ICOUT)}/V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$		20		V/V
V_{IOUT_ACC}	Current sense output accuracy	$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 40.96mV	–2%		2%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 20.48mV	–4%		4%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 10.24mV	–15%		15%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 5.12mV	–20%		20%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 2.56mV	–33%		33%	
		$V_{(SRP-SRN)}$ or $V_{(ACP-ACN)}$ = 1.28mV	–50%		50%	
C_{IOUT_MAX}	Maximum output load capacitance	For stability with 0 to 1mA load			100	pF
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{VCC} > 6.5V, V_{ACDET} > 0.6V (0-55mA load)	5.5	6	6.5	V
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0V, V_{VCC} > UVLO charge enabled and not in TSHUT	65	80		mA
$I_{REGN_LIM_TSHUT}$		V_{REGN} = 0V, V_{VCC} > UVLO charge disabled or in TSHUT	7	16		
C_{REGN}	REGN output capacitor required for stability	I_{LOAD} = 100µA to 65mA		1		µF

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V ≤ $V_{(VCC)}$ ≤ 24 V, 0°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UNDERVOLTAGE LOCK-OUT COMPARATOR (UVLO)						
V_{UVLO}	Input under voltage rising threshold	V_{VCC} rising	3.5	3.75	4	V
V_{UVLO_HYS}	Input under voltage falling hysteresis	V_{VCC} falling		340		mV
FAST DPM COMPARATOR (FAST_DPM)						
V_{FAST_DPM}	Fast DPM comparator stop charging rising threshold with respect to input current limit, voltage across input sense resistor rising edge (specified by design)			108%		
QUIESCENT CURRENT						
I_{BAT}	Total battery leakage current to I_{SRN} + I_{SRP} +I_{PHASE} + I_{VCC} + I_{ACP} + I_{ACN}	V_{VCC} < V_{BAT} = 16.8V, T_J = 0 to 85°C			15	µA
$I_{STANDBY}$	Standby quiescent current, I_{VCC} + I_{ACP} + I_{ACN}	V_{VCC} > V_{UVLO}, V_{ACDET} > 0.6V, charge disabled, T_J = 0 to 85°C		0.5	1	mA
I_{AC_NOSW}	Adapter bias current during charge, I_{VCC} + I_{ACP} + I_{ACN}	V_{VCC} > V_{UVLO}, V_{ACDET} > 2.4V, charge enabled, no switching, T_J = 0 to 85°C		1.5	3	mA
I_{AC_SW}	Adapter bias current during charge, I_{VCC} + I_{ACP} + I_{ACN}	V_{VCC} > V_{UVLO}, V_{ACDET} > 2.4V, charge enabled, switching, MOSFET Sis412DN		10		mA
ACOK COMPARATOR						
V_{ACOK_FALL}	$\overline{ACOK}$ falling threshold	V_{VCC}>V_{UVLO}, V_{ACDET} rising	2.376	2.4	2.424	V
$V_{ACOK_RISE_HYS}$	$\overline{ACOK}$ rising hysteresis	V_{VCC}>V_{UVLO}, V_{ACDET} falling	35	55	75	mV
$t_{ACOK_FALL_DEG}$	$\overline{ACOK}$ falling deglitch (specified by design)	V_{VCC}>V_{UVLO}, V_{ACDET} rising above 2.4V, ChargeOption() bit [15] = 0 (default), (bq24707 only)	0.9	1.3	1.7	s
		V_{VCC}>V_{UVLO}, V_{ACDET} rising above 2.4V, ChargeOption() bit [15] = 0 (default), (bq24707A only)	0.8	1.2	2	ms
		V_{VCC}>V_{UVLO}, V_{ACDET} rising above 2.4V, ChargeOption() bit [15] = 1		10	50	µs
V_{WAKEUP_RISE}	WAKEUP detect rising threshold	V_{VCC}>V_{UVLO}, V_{ACDET} rising		0.57	0.8	V
V_{WAKEUP_FALL}	WAKEUP detect falling threshold	V_{VCC}>V_{UVLO}, V_{ACDET} falling	0.3	0.51		V
VCC to SRN COMPARATOR (VCC_SRN)						
$V_{VCC\text{-}SRN_FALL}$	VCC-SRN falling threshold	V_{VCC} falling towards V_{SRN}	70	125	180	mV
$V_{VCC\text{-}SRN_RHYS}$	VCC-SRN rising hysteresis	V_{VCC} rising above V_{SRN}	70	120	170	mV
HIGH SIDE IFAULT COMPARATOR (IFAULT_HI)[1]						
$V_{IFAULT_HI_RISE}$	ACP to PHASE rising threshold	ChargeOption() bit [8:7] = 00	200	300	450	mV
		ChargeOption() bit [8:7] = 01	330	500	700	
		ChargeOption() bit [8:7] = 10 (default)	450	700	1000	
		ChargeOption() bit [8:7] = 11	600	900	1250	
LOW SIDE IFAULT COMPARATOR (IFAULT_LOW)						
$V_{IFAULT_LOW_RISE}$	PHASE to GND rising threshold		40	110	160	mV
INPUT OVER-CURRENT COMPARATOR (ACOC)[1]						
V_{ACOC}	Adapter over current rising threshold with respect to input current limit, voltage across input sense resistor rising edge	ChargeOption() bit [2:1] = 01	120%	133%	145%	
		ChargeOption() bit [2:1] = 10 (default)	150%	166%	180%	
		ChargeOption() bit [2:1] = 11	200%	222%	240%	
V_{ACOC_min}	Min ACOC threshold clamp voltage	ChargeOption() bit [2:1] = 01 (133%), InputCurrent() = 0x0400H (10.24mV)	40	45	50	mV
V_{ACOC_max}	Max ACOC threshold clamp voltage	ChargeOption() bit [2:1] = 11 (222%), InputCurrent() = 0x1F80H (80.64mV)	140	150	160	mV
t_{ACOC_DEG}	ACOC deglitch time (specified by design)	Voltage across input sense resistor rising to disable charge	1.7	2.5	3.3	ms
BAT OVER-VOLTAGE COMPARATOR (BAT_OVP)						
V_{OVP_RISE}	Over voltage rising threshold as percentage of V_{BAT_REG}	V_{SRN} rising	103%	104%	106%	
V_{OVP_FALL}	Over voltage falling threshold as percentage of V_{BAT_REG}	V_{SRN} falling		102%		
CHARGE OVERCURRENT COMPARATOR (CHG_OCP)						
V_{OCP_RISE}	Charge over current rising threshold, measure voltage drop across current sensing resistor	ChargeCurrent() = 0x0xxxH	54	60	66	mV
		ChargeCurrent() = 0x1000H – 0x17C0H	80	90	100	mV
		ChargeCurrent() = 0x1800 H– 0x1FC0H	110	120	130	mV

(1) User can adjust threshold via SMBus ChargeOption() REG0x12.

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V ≤ $V_{(VCC)}$ ≤ 24 V, 0°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE UNDER-CURRENT COMPARATOR (CHG_UCP)						
V_{UCP_FALL}	Charge under current falling threshold	V_{SRP} falling towards V_{SRN}	1	5	9	mV
LIGHT LOAD COMPARATOR (LIGHT_LOAD)						
V_{LL_FALL}	Light load falling threshold	Measure voltage drop across current sensing resistor		1.25		mV
$V_{LL_RISE_HYST}$	Light load rising hysteresis	Measure voltage drop across current sensing resistor		1.25		mV
BATTERY LOWV COMPARATOR (BAT_LOWV)						
V_{BATLV_FALL}	Battery LOWV falling threshold	V_{SRN} falling	2.4	2.5	2.6	V
V_{BATLV_RHYST}	Battery LOWV rising hysteresis	V_{SRN} rising		200		mV
I_{BATLV}	Battery LOWV charge current limit	10mΩ current sensing resistor		0.5		A
THERMAL SHUTDOWN COMPARATOR (TSHUT)						
T_{SHUT}	Thermal shutdown rising temperature	Temperature rising		155		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis, falling	Temperature falling		20		°C
ILIM COMPARATOR						
V_{ILIM_FALL}	ILIM as CE falling threshold	V_{ILIM} falling	60	75	90	mV
V_{ILIM_RISE}	ILIM as CE rising threshold	V_{ILIM} rising	90	105	120	mV
LOGIC INPUT (SDA, SCL)						
V_{IN_LO}	Input low threshold				0.8	V
V_{IN_HI}	Input high threshold		2.1			V
I_{IN_LEAK}	Input bias current	V = 7 V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN ($\overline{ACOK}$, SDA, $\overline{IFAULT}$, CMPOUT)						
V_{OUT_LO}	Output saturation voltage	5 mA drain current			500	mV
I_{OUT_LEAK}	Leakage current	V = 7 V	–1		1	µA
ANALOG INPUT (ACDET, ILIM)						
I_{IN_LEAK}	Input bias current	V = 7 V	–1		1	µA
ANALOG INPUT (CMPIN has 50kΩ series resistor and 2000kΩ pull down resistor)						
I_{IN_LEAK}	Input bias current	V = 7 V	1	3.5	7	µA
PWM OSCILLATOR						
F_{SW}	PWM switching frequency	ChargeOption() bit [9] = 0 (default)	600	750	900	kHz
F_{SW+}	PWM increase frequency	ChargeOption() bit [10:9] = 11	665	885	1100	kHz
F_{SW-}	PWM decrease frequency	ChargeOption() bit [10:9] = 01	465	615	765	kHz
PWM HIGH SIDE DRIVER (HIDRV)						
$R_{DS_HI_ON}$	High side driver (HSD) turn-on resistance	$V_{BTST} – V_{PH}$ = 5.5 V, I = 10mA		12	20	Ω
$R_{DS_HI_OFF}$	High side driver turn-off resistance	$V_{BTST} – V_{PH}$ = 5.5 V, I = 10mA		0.65	1.3	Ω
$V_{BTST_REFRESH}$	Bootstrap refresh comparator threshold voltage	$V_{BTST} – V_{PH}$ when low side refresh pulse is requested	3.85	4.3	4.7	V
PWM LOW SIDE DRIVER (LODRV)						
$R_{DS_LO_ON}$	Low side driver (LSD) turn-on resistance	V_{REGN} = 6 V, I = 10 mA		15	25	Ω
$R_{DS_LO_OFF}$	Low side driver turn-off resistance	V_{REGN} = 6 V, I = 10 mA		0.9	1.4	Ω
PWM DRIVER TIMING						
t_{LOW_HIGH}	Driver dead time from low side to high side			20		ns
t_{HIGH_LOW}	Driver dead time from high side to low side			20		ns
INTERNAL SOFT START						
I_{STEP}	Soft start step size	In CCM mode, 10mΩ current sense resistor		64		mA
t_{STEP}	Soft start step time	In CCM mode, 10mΩ current sense resistor		240		µs
INDEPENDENT COMPARATOR (2)						
V_{IC_REF1}	Comparator reference	ChargeOption() bit [4] = 0, rising edge (default)	0.585	0.6	0.615	V
V_{IC_REF2}	Comparator reference	ChargeOption() bit [4] = 1, rising edge	2.375	2.4	2.425	V
R_S	Series resistor			50		kΩ
R_{DOWN}	Pull down resistor			2000		kΩ

(2) User can adjust threshold via SMBus ChargeOption() REG0x12.

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V ≤ $V_{(VCC)}$ ≤ 24 V, 0°C ≤ T_J ≤ 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SMBus TIMING CHARACTERISTICS						
t_R	SCLK/SDATA rise time				1	µs
t_F	SCLK/SDATA fall time				300	ns
$t_{W(H)}$	SCLK pulse width high		4		50	µs
$t_{W(L)}$	SCLK pulse width low		4.7			µs
$t_{SU(STA)}$	Setup time for START condition		4.7			µs
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated		4			µs
$t_{SU(DAT)}$	Data setup time		250			ns
$t_{H(DAT)}$	Data hold time		300			ns
$t_{SU(STOP)}$	Setup time for STOP condition		4			µs
$t_{(BUF)}$	Bus free time between START and STOP condition		4.7			µs
$F_{S(CL)}$	Clock frequency		10		100	kHz
HOST COMMUNICATION FAILURE						
$t_{timeout}$	SMBus bus release timeout(3)		25		35	ms
t_{BOOT}	Deglitch for watchdog reset signal		10			ms
t_{WDI}	Watchdog timeout period, ChargeOption() bit [14:13] = 01(4)		35	44	53	s
t_{WDI}	Watchdog timeout period, ChargeOption() bit [14:13] = 10(4)		70	88	105	s
t_{WDI}	Watchdog timeout period, ChargeOption() bit [14:13] = 11(4) (default)		140	175	210	s

(3) Devices participating in a transfer timeout when any clock low exceeds the 25ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).
(4) User can adjust threshold via SMBus ChargeOption() REG0x12.

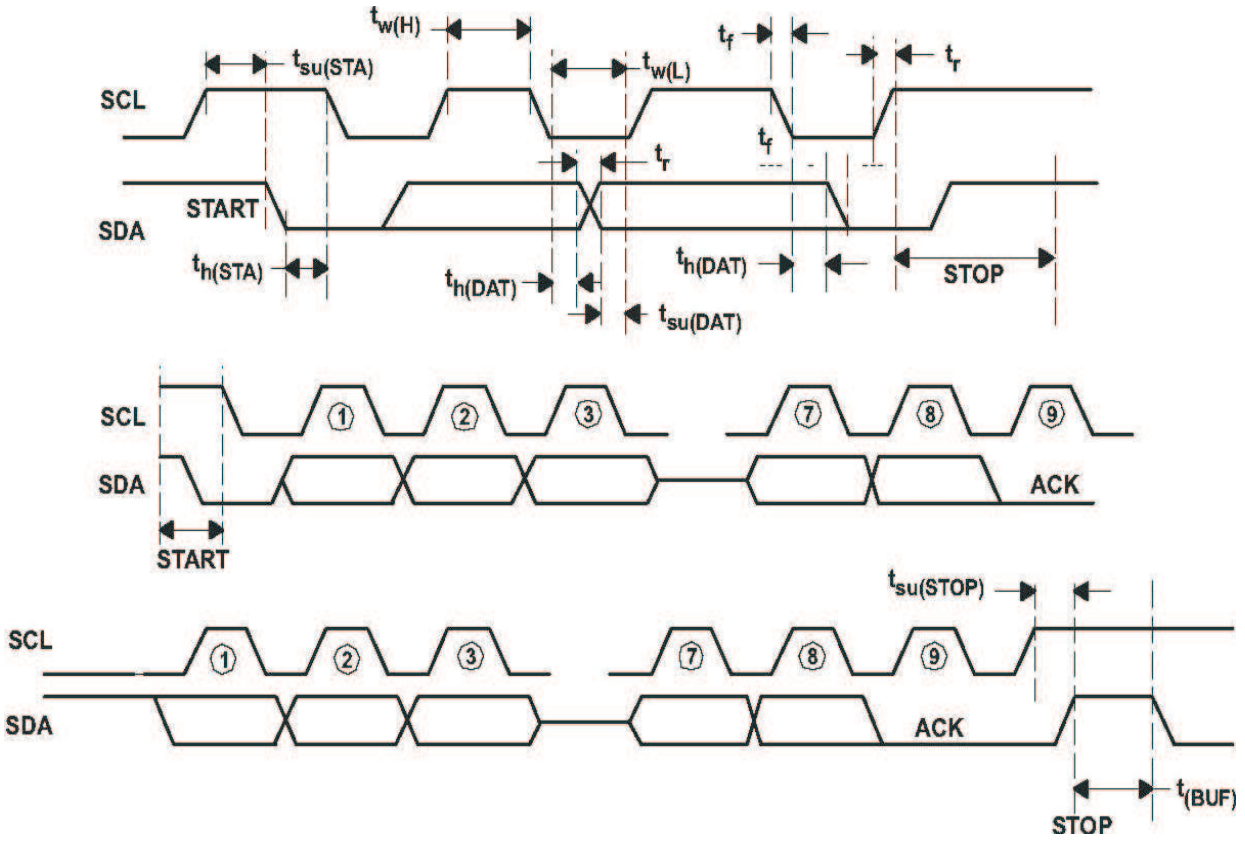
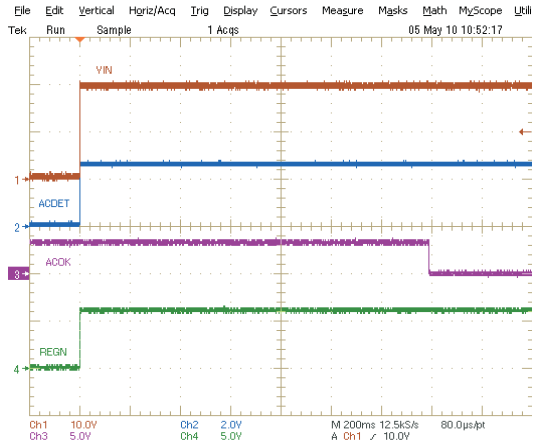


Figure 2. SMBus Communication Timing Waveforms

TYPICAL CHARACTERISTICS

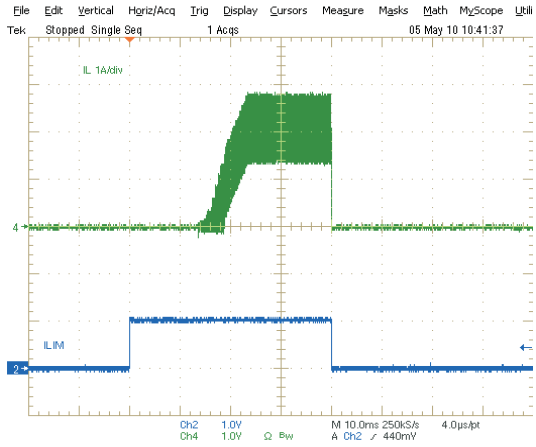
Table 1. Table of Graphs

	FIGURE NO.
VCC, ACDET, REGN and $\overline{\text{ACOK}}$ Power up (bq24707)	Figure 3
Charge Enable by ILIM	Figure 4
Current Soft-start	Figure 5
Charge Disable by ILIM	Figure 6
Continuous Conduction Mode Switching Waveforms	Figure 7
Cycle-by-Cycle Synchronous to Non-synchronous	Figure 8
100% Duty and Refresh Pulse	Figure 9
System Load Transient (Input DPM)	Figure 10
Battery Insertion	Figure 11
Battery to Ground Short Protection	Figure 12
Battery to Ground Short Transition	Figure 13
Efficiency vs Output Current	Figure 14



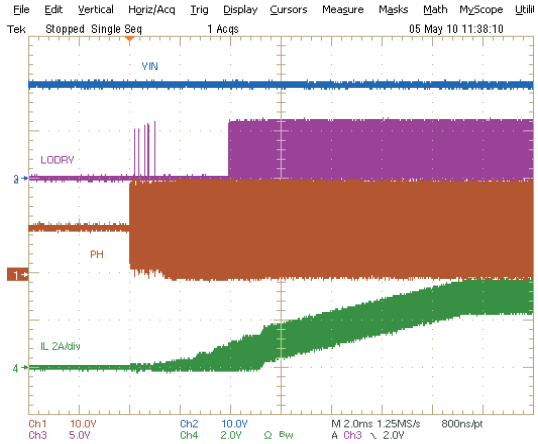
CH1: VCC, 10V/div, CH2: ACDET, 2V/div, CH3: $\overline{\text{ACOK}}$, 5V/div, CH4: REGN, 5V/div, 200ms/div

Figure 3. VCC, ACDET, REGN and $\overline{\text{ACOK}}$ Power Up (bq24707)



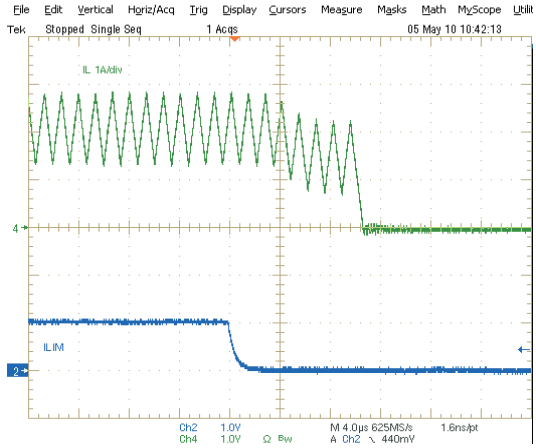
CH2: ILIM, 1V/div, CH4: inductor current, 1A/div, 10ms/div

Figure 4. Charge Enable by ILIM



CH1: PHASE, 10V/div, CH2: Vin, 10V/div, CH3: LODRV, 5V/div, CH4: inductor current, 2A/div, 2ms/div

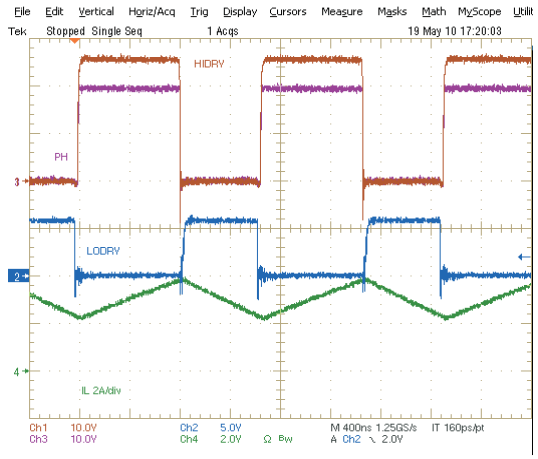
Figure 5. Current Soft-Start



CH2: ILIM, 1V/div, CH4: inductor current, 1A/div, 4us/div

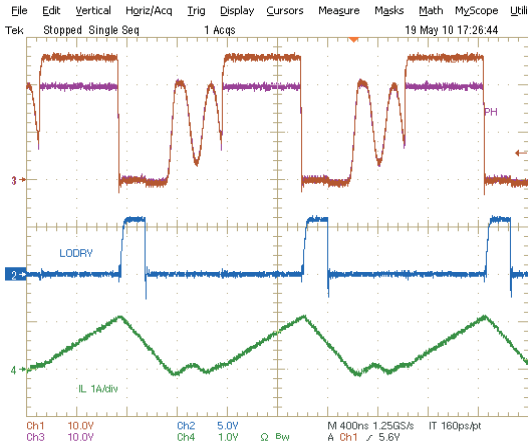
Figure 6. Charge Disable by ILIM

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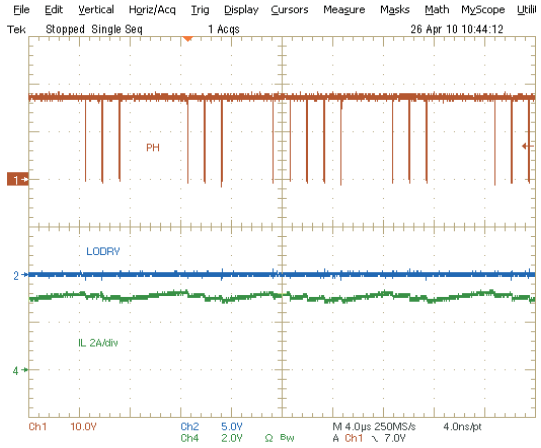
CH1: HIDRV, 10V/div, CH2: LODRV, 5V/div, CH3: PHASE, 10V/div, CH4: inductor current, 2A/div, 400ns/div

Figure 7. Continuous Conduction Mode Switching Waveforms



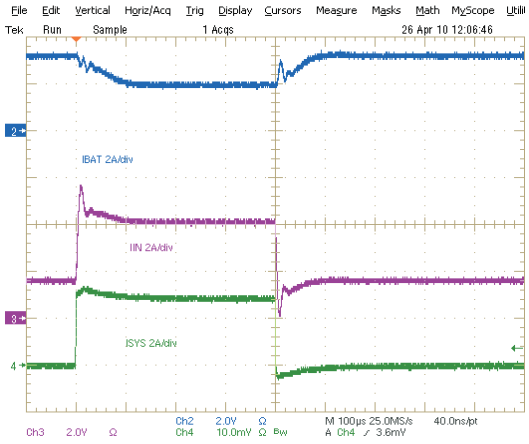
CH1: HIDRV, 10V/div, CH2: LODRV, 5V/div, CH3: PHASE, 10V/div, CH4: inductor current, 1A/div, 400ns/div

Figure 8. Cycle-by-Cycle Synchronous to Non-synchronous



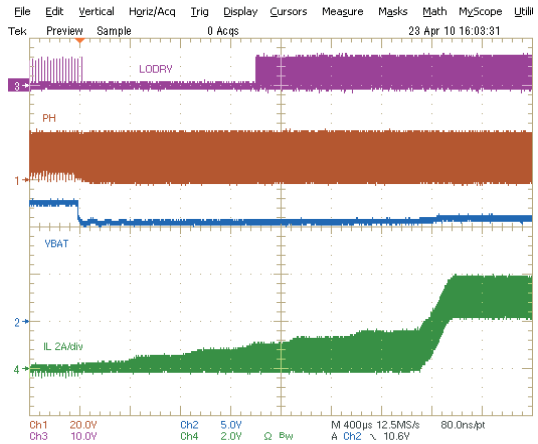
CH1: PHASE, 10V/div, CH2: LODRV, 5V/div, CH4: inductor current, 2A/div, 4us/div

Figure 9. 100% Duty and Refresh Pulse



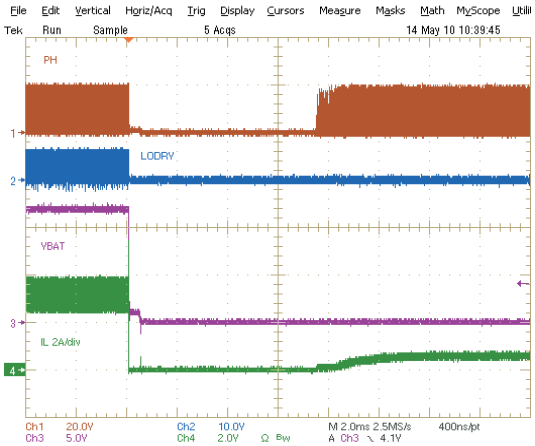
CH2: battery current, 2A/div, CH3: adapter current, 2A/div, CH4: system load current, 2A/div, 100us/div

Figure 10. System Load Transient (Input DPM)



CH1: PHASE, 20V/div, CH2: battery voltage, 5V/div, CH3: LODRV, 10V/div, CH4: inductor current, 2A/div, 400us/div

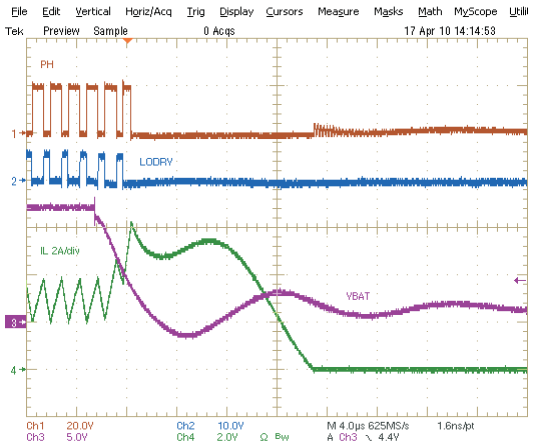
Figure 11. Battery Insertion



CH1: PHASE, 20V/div, CH2: LODRV, 10V/div, CH3: battery voltage, 5V/div, CH4: inductor current, 2A/div, 2ms/div

Figure 12. Battery to Ground Short Protection

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CH1: PHASE, 20V/div, CH2: LODRV, 10V/div, CH3: battery voltage, 5V/div, CH4: inductor current, 2A/div, 4us/div

Figure 13. Battery to Ground Short Transition

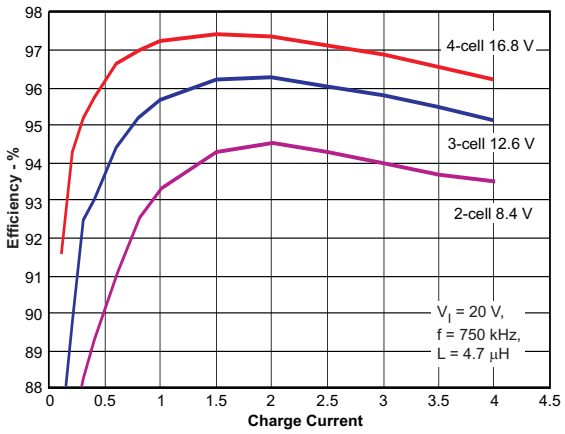


Figure 14. Efficiency vs Output Current

PIN FUNCTIONS – 20-PIN QFN

PIN		DESCRIPTION
NO.	NAME	
1	ACN	Input current sense resistor negative input. Place an optional 0.1µF ceramic capacitor from ACN to GND for common-mode filtering. Place a 0.1µF ceramic capacitor from ACN to ACP to provide differential mode filtering.
2	ACP	Input current sense resistor positive input. Place a 0.1µF ceramic capacitor from ACP to GND for common-mode filtering. Place a 0.1µF ceramic capacitor from ACN to ACP to provide differential-mode filtering.
3	CMPOUT	Open-drain output of independent comparator. Place a 10kΩ pull-up resistor from CMPOUT to pull-up supply rail. Internal reference is 0.6V or 2.4V, selectable by SMBus command ChargeOption(). When CMPIN is above the internal reference, CMPOUT goes HIGH. Place a resistor between CMPIN and CMPOUT to program hysteresis.
4	CMPIN	Input of independent comparator. It has one 50kΩ series resistor and one 2000kΩ pull-down resistor. Program CMPIN voltage by connecting a resistor divider from the IOUT pin to the CMPIN pin to the GND pin for adapter or charge current comparison or from the SRN pin to the CMPIN pin to the GND pin for battery voltage comparison. The internal reference is 0.6V or 2.4V, selectable by SMBus command ChargeOption(). When CMPIN is above the internal reference, CMPOUT goes HIGH. Place a resistor between CMPIN and CMPOUT to program hysteresis.
5	$\overline{\text{ACOK}}$	AC adapter detect open drain output. It is pulled LOW to GND by an internal MOSFET when the voltage on the ACDET pin is above 2.4V, voltage on the VCC pin is above UVLO and voltage on the VCC pin is 245mV above the voltage on the SRN pin, indicating a valid adapter is present to start charge. If any one of the above conditions cannot meet, it is pulled HIGH to the external pull-up supply rail by an external pull-up resistor. Connect a 10kΩ pull-up resistor from the $\overline{\text{ACOK}}$ pin to the pull-up supply rail.
6	ACDET	Adapter detection input. Program the adapter valid input threshold by connecting a resistor divider from the adapter input to the ACDET pin to the GND pin. When the ACDET pin is above 0.6V and VCC is above UVLO, REGN LDO is present, $\overline{\text{ACOK}}$ comparator and IOUT are both active.
7	IOUT	Buffered adapter or charge current output, selectable with SMBus command ChargeOption(). IOUT voltage is 20 times the differential voltage across the sense resistor. Place a 100pF or less ceramic decoupling capacitor from the IOUT pin to GND.
8	SDA	SMBus open-drain data I/O. Connect to the SMBus data line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to SMBus specifications.
9	SCL	SMBus open-drain clock input. Connect to the SMBus clock line from the host controller or smart battery. Connect a 10kΩ pull-up resistor according to SMBus specifications.
10	ILIM	Charge current limit input. Program ILIM voltage by connecting a resistor divider from the system reference 3.3V rail to the ILIM pin to the GND pin. The lower of the ILIM voltage or DAC limit voltage sets the charge current regulation limit. To disable control on ILIM, set ILIM above 1.6V. Once the voltage on the ILIM pin falls below 75mV, charge is disabled. Charge is enabled when the ILIM pin rises above 105mV.
11	$\overline{\text{IFAULT}}$	Open-drain output. It is pulled LOW by an internal MOSFET when ACOC or a short circuit is detected. It is pulled HIGH to the external pull-up supply rail by an external pull-up resistor in normal condition.
12	SRN	Charge current sense resistor negative input. The SRN pin is for battery voltage sensing as well. Connect SRN pin to a 7.5 Ω resistor first then from resistor another terminal connect a 0.1µF ceramic capacitor to GND for common-mode filtering and connect to current sensing resistor. Connect a 0.1µF ceramic capacitor between current sensing resistor to provide differential mode filtering. See application information about negative output voltage protection for hard shorts on battery to ground or battery reverse connection by adding small resistor.

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PIN FUNCTIONS – 20-PIN QFN (continued)

PIN		DESCRIPTION
NO.	NAME	
13	SRP	Charge current sense resistor positive input. Connect SRP pin to a 10 Ω resistor first then from resistor another terminal connect to current sensing resistor. Connect a 0.1μF ceramic capacitor between current sensing resistor to provide differential mode filtering. See application information about negative output voltage protection for hard shorts on battery to ground or battery reverse connection by adding small resistor.
14	GND	IC ground. On PCB layout, connect to the analog ground plane, and only connect to power ground plane through the PowerPAD underneath the IC.
15	LODRV	Low side power MOSFET driver output. Connect to low side n-channel MOSFET gate.
16	REGN	Linear regulator output. REGN is the output of the 6V linear regulator supplied from VCC. The LDO is active when the voltage on the ACDET pin is above 0.6V and voltage on VCC is above UVLO. Connect a 1uF ceramic capacitor from REGN to GND.
17	BTST	High side power MOSFET driver power supply. Connect a 0.047μF capacitor from BTST to PHASE, and a bootstrap Schottky diode from REGN to BTST.
18	HIDRV	High side power MOSFET driver output. Connect to the high side n-channel MOSFET gate.
19	PHASE	High side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.
20	VCC	Input supply, diode OR from adapter or battery voltage. Use 10Ω resistor and 1μF capacitor to ground as low pass filter to limit inrush current.
PowerPAD		Exposed pad beneath the IC. Analog ground and power ground star-connected only at the PowerPAD plane. Always solder PowerPAD to the board, and have vias on the PowerPAD plane connecting to analog ground and power ground planes. It also serves as a thermal pad to dissipate the heat.

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FUNCTIONAL BLOCK DIAGRAM

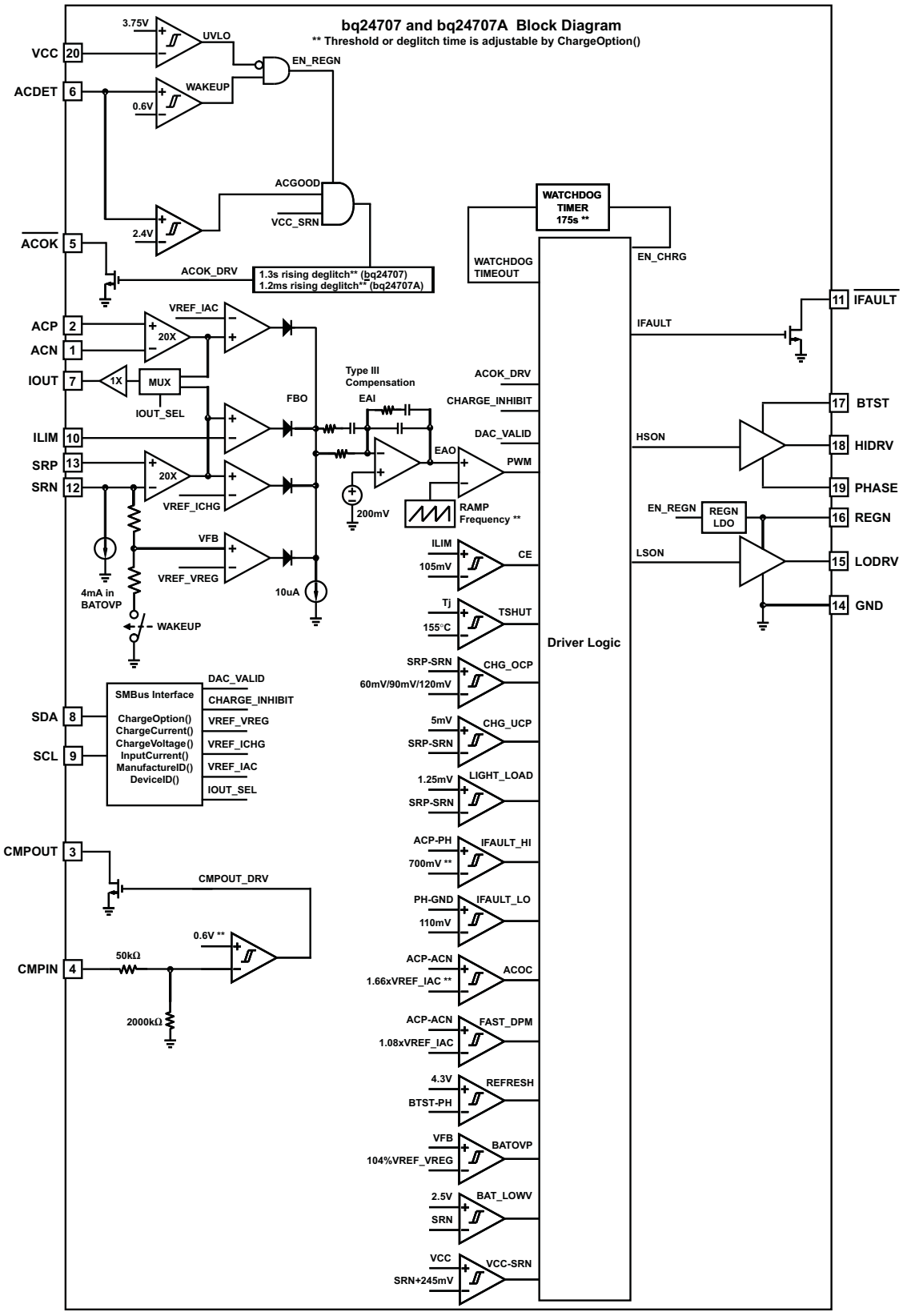


Figure 15. Functional Block Diagram for bq24707 and bq24707A

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DETAILED DESCRIPTION

SMBus Interface

The IC operates as a slave, receiving control inputs from the embedded controller host through the SMBus interface. The IC uses a simplified subset of the commands documented in System Management Bus Specification V1.1, which can be downloaded from www.smbus.org. The IC uses the SMBus Read-Word and Write-Word protocols (see Figure 16) to communicate with the smart battery. The IC performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus. In addition, the IC has two identification registers a 16-bit device ID register (0xFFH) and a 16-bit manufacturer ID register (0xFEH).

SMBus communication is enabled with the following conditions:

- V_{VCC} is above UVLO;
- V_{ACDET} is above 0.6V;

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors (10kΩ) for SDA and SCL to achieve rise times according to the SMBus specifications. Communication starts when the master signals a START condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figure 17 and Figure 18 show the timing diagrams for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. The SDA state changes only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the IC because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle. The IC supports the charger commands as described in Table 2.

a) Write-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	

Preset to 0b0001001 **ChargeCurrent() = 0x14H D7 D0 D15 D8**
ChargeVoltage() = 0x15H
InputCurrent() = 0x3FH
ChargeOption() = 0x12H

b) Read-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 BITS	1b	1b	8 BITS	1b		7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	

Preset to 0b0001001 **DeviceID() = 0xFFH** **Preset to 0b0001001** **D7 D0** **D15 D8**
ManufactureID() = 0xFEH
ChargeCurrent() = 0x14H
ChargeVoltage() = 0x15H
InputCurrent() = 0x3FH
ChargeOption() = 0x12H

LEGEND:
S = START CONDITION OR REPEATED START CONDITION
P = STOP CONDITION
ACK = ACKNOWLEDGE (LOGIC-LOW)
NACK = NOT ACKNOWLEDGE (LOGIC-HIGH)
W = WRITE BIT (LOGIC-LOW)
R = READ BIT (LOGIC-HIGH)

MASTER TO SLAVE
SLAVE TO MASTER

Figure 16. SMBus Write-Word and Read-Word Protocols

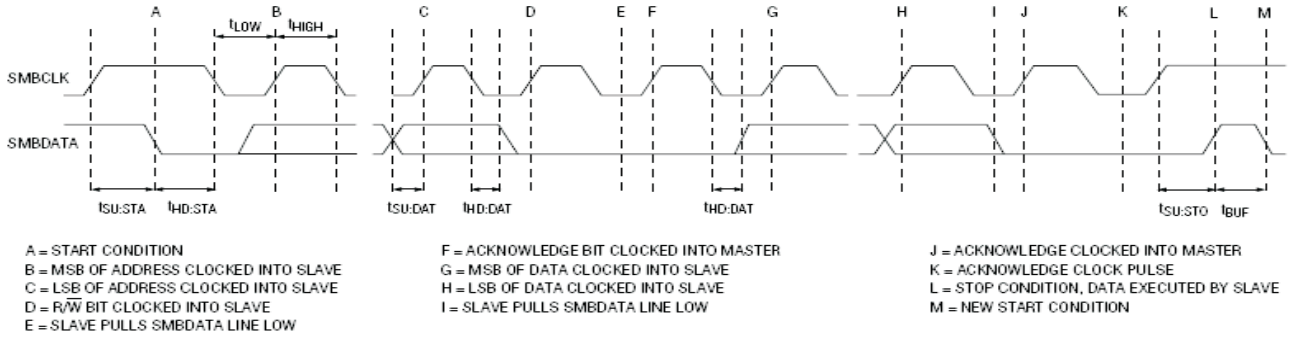


Figure 17. SMBus Write Timing

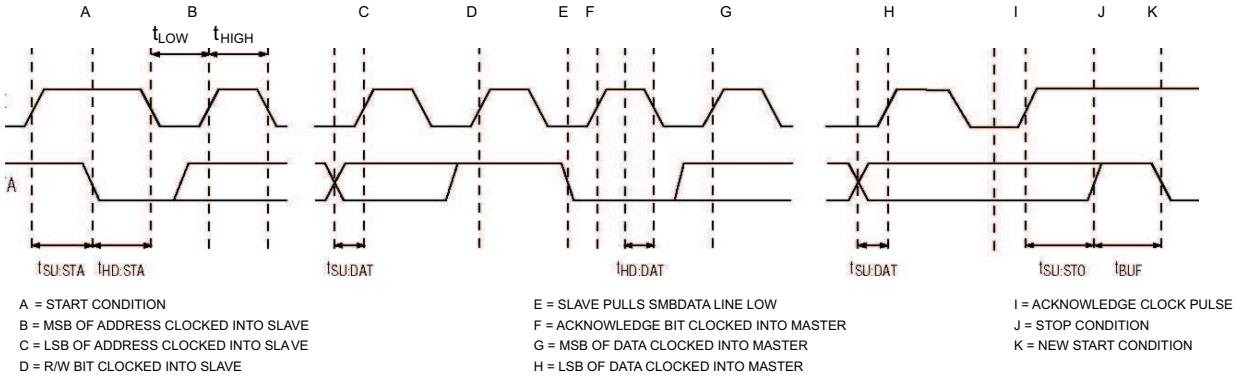


Figure 18. SMBus Read Timing

Battery-Charger Commands

The IC supports six battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 2. ManufacturerID() and DeviceID() can be used to identify the IC. The ManufacturerID() command always returns 0x0040H and the DeviceID() command always returns 0x000AH.

Table 2. Battery Charger Command Summary

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	DESCRIPTION	POR STATE
0x12H	ChargeOption()	Read or Write	Charger Options Control	0x7904H
0x14H	ChargeCurrent()	Read or Write	7-Bit Charge Current Setting	0x0000H
0x15H	ChargeVoltage()	Read or Write	11-Bit Charge Voltage Setting	0x0000H
0x3FH	InputCurrent()	Read or Write	6-Bit Input Current Setting	0x1000H
0XFEH	ManufacturerID()	Read Only	Manufacturer ID	0x0040H
0xFFH	DeviceID()	Read Only	Device ID	0x000AH

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Setting Charger Options

By writing ChargeOption() command (0x12H or 0b00010010), the IC allows users to change several charger options after POR (Power On Reset) as shown in Table 3.

Table 3. Charge Options Register (0x12H)

BIT	BIT NAME	DESCRIPTION
[15]	$\overline{\text{ACOK}}$ Deglitch Time Adjust	Adjust $\overline{\text{ACOK}}$ deglitch time. **0: $\overline{\text{ACOK}}$ deglitch time 1.3s for bq24707, 1.2ms for bq24707A <default at POR>** 1: $\overline{\text{ACOK}}$ deglitch time set to minimum (<50µs). To change this option, VCC pin voltage must be above UVLO and ACDET pin voltage must be above 0.6V to enable IC SMBus communication and set this bit to 1 to disable the $\overline{\text{ACOK}}$ deglitch timer. After POR the bit default value is 0 and $\overline{\text{ACOK}}$ deglitch time is 1.3s for bq24707 and 1.2ms for bq24707A.
[14:13]	WATCHDOG Timer Adjust	Set maximum delay between consecutive SMBus Write charge voltage or charge current command. The charge is suspended if the IC does not receive write charge voltage or write charge current command within the watchdog time period and watchdog timer is enabled. The charge is resumed after receive write charge voltage or write charge current command when watchdog timer expires and charge suspends. 00: Disable Watchdog Timer 01: Enabled, 44 sec 10: Enabled, 88 sec **11: Enable Watchdog Timer (175s) <default at POR>**
[12:11]	Not In Use	**11 at POR**
[10]	EMI Switching Frequency Adjust	**0: Reduce PWM switching frequency by 18% <default at POR>** 1: Increase PWM switching frequency by 18%
[9]	EMI Switching Frequency Enable	**0: Disable adjust PWM switching frequency <default at POR>** 1: Enable adjust PWM switching frequency
[8:7]	IFAULT_HI Comparator Threshold Adjust	Short circuit protection high side MOSFET voltage drop comparator threshold. 00: 300mV 01: 500mV **10: 700mV <default at POR>** 11: 900mV
[6]	Not In Use	**0 at POR**
[5]	IOUT Selection	**0: IOUT is the 20x adapter current amplifier output <default at POR>** 1: IOUT is the 20x charge current amplifier output
[4]	Comparator Threshold Adjust	**0: 0.6V <default at POR>** 1: 2.4V
[3]	Not In Use	**0 at POR**
[2:1]	ACOC Threshold Adjust	00: Disable ACOC 01: 1.33X of input current regulation limit **10: 1.66X of input current regulation limit <default at POR>** 11: 2.22X of input current regulation limit
[0]	Charge Inhibit	**0: Enable Charge <default at POR>** 1: Inhibit Charge

Setting the Charge Current

To set the charge current, write a 16-bit ChargeCurrent() command (0x14H or 0b00010100) using the data format listed in Table 4. With a 10mΩ sense resistor, the IC provides a charge current range of 128mA to 8.128A, with 64mA step resolution. Sending ChargeCurrent() below 128mA or above 8.128A clears the register and terminates charging. Upon POR, charge current is 0A. A 0.1µF capacitor between SRP and SRN for differential mode filtering, 0.1µF capacitor between SRN and ground for common mode filtering, and an optional 0.1µF capacitor between SRP and ground for common mode filtering is recommended. Meanwhile, the capacitance on SRP should not be higher than 0.1µF in order to properly sense the voltage across SRP and SRN for cycle-by-cycle under-current and over-current detection.

The SRP and SRN pins are used to sense R_{SR} with a default value of 10mΩ. However, resistors of other values

can also be used. With a larger sense resistor comes a larger sense voltage, and higher regulation accuracy; but, at the expense of higher conduction loss. If the current sensing resistor value is too high, it may trig over current protection threshold due to the current ripple voltage being too high. In such a case either a higher inductance value or a lower current sensing resistor value should be used to limit the current ripple voltage level. A current sensing resistor value of no more than 20mΩ is suggested.

To provide secondary protection, the IC has an ILIM pin with which the user can program the maximum allowed charge current. Internal charge current limit is the lower one between the voltage set by ChargeCurrent(), and voltage on the ILIM pin. To disable this function, the user can pull ILIM above 1.6V, which is the maximum charge current regulation limit. The following equation shows the voltage should add on the ILIM pin with respect to the preferred charge current limit:

$$V_{ILIM} = 20 \times \left(V_{SRP} - V_{SRN}\right) = 20 \times I_{CHG} \times R_{SR} \quad (1)$$

Table 4. Charge Current Register (0x14H), Using 10mΩ Sense Resistor

BIT	BIT NAME	DESCRIPTION
0	–	Not used.
1	–	Not used.
2	–	Not used.
3	–	Not used.
4	–	Not used.
5	–	Not used.
6	Charge Current, DACICHG 0	0 = Adds 0mA of charger current. 1 = Adds 64mA of charger current.
7	Charge Current, DACICHG 1	0 = Adds 0mA of charger current. 1 = Adds 128mA of charger current.
8	Charge Current, DACICHG 2	0 = Adds 0mA of charger current. 1 = Adds 256mA of charger current.
9	Charge Current, DACICHG 3	0 = Adds 0mA of charger current. 1 = Adds 512mA of charger current.
10	Charge Current, DACICHG 4	0 = Adds 0mA of charger current. 1 = Adds 1024mA of charger current.
11	Charge Current, DACICHG 5	0 = Adds 0mA of charger current. 1 = Adds 2048mA of charger current.
12	Charge Current, DACICHG 6	0 = Adds 0mA of charger current. 1 = Adds 4096mA of charger current.
13	–	Not used.
14	–	Not used.
15	–	Not used.

Setting the Charge Voltage

To set the output charge regulation voltage, write a 16bit ChargeVoltage() command (0x15H or 0b00010101) using the data format listed inTable 5. The IC provides a charge voltage range from 1.024V to 19.200V, with 16mV step resolution. Sending ChargeVoltage() below 1.024V or above 19.2V clears the register and terminates charging. Upon POR, the charge voltage limit is 0V.

The SRN pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, and directly place a decoupling capacitor (0.1μF recommended) as close to the IC as possible to decouple high frequency noise.

Table 5. Charge Voltage Register (0x15H)

BIT	BIT NAME	DESCRIPTION
0	-	Not used.
1	-	Not used.
2	-	Not used.
3	-	Not used.

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Table 5. Charge Voltage Register (0x15H) (continued)

BIT	BIT NAME	DESCRIPTION
4	Charge Voltage, DACV 0	0 = Adds 0mV of charger voltage. 1 = Adds 16mV of charger voltage.
5	Charge Voltage, DACV 1	0 = Adds 0mV of charger voltage. 1 = Adds 32mV of charger voltage.
6	Charge Voltage, DACV 2	0 = Adds 0mV of charger voltage. 1 = Adds 64mV of charger voltage.
7	Charge Voltage, DACV 3	0 = Adds 0mV of charger voltage. 1 = Adds 128mV of charger voltage.
8	Charge Voltage, DACV 4	0 = Adds 0mV of charger voltage. 1 = Adds 256mV of charger voltage.
9	Charge Voltage, DACV 5	0 = Adds 0mV of charger voltage. 1 = Adds 512mV of charger voltage.
10	Charge Voltage, DACV 6	0 = Adds 0mV of charger voltage. 1 = Adds 1024mV of charger voltage.
11	Charge Voltage, DACV 7	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
12	Charge Voltage, DACV 8	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
13	Charge Voltage, DACV 9	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
14	Charge Voltage, DACV 10	0 = Adds 0mV of charger voltage. 1 = Adds 16384mV of charger voltage.
15	-	Not used.

Setting Input Current

System current normally fluctuates as portions of the system are powered up or put to sleep. With the input current limit, the output-current requirement of the AC wall adapter can be lowered, reducing system cost.

The total input current, from a wall cube or other DC source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the set input current limit, the IC decreases the charge current to provide priority to system load current. As the system current rises, the available charge current drops linearly to zero. Thereafter, all input current goes to system load and input current increases.

During DPM regulation, the total input current is the sum of the device supply current I_{BIAS}, the charger input current, and the system load current I_{LOAD}, and can be estimated as follows:

$$I_{INPUT} = I_{LOAD} + \left[\frac{I_{BATTERY} \times V_{BATTERY}}{V_{IN} \times \eta} \right] + I_{BIAS} \quad (2)$$

where η is the efficiency of the charger buck converter (typically 85% to 95%).

To set the input current limit, write a 16-bit InputCurrent() command (0x3FH or 0b00111111) using the data format listed in Table 6. When using a 10mΩ sense resistor, the IC provides an input-current limit range of 128mA to 8.064A, with 128mA resolution. An input current limit set to no less than 512mA is suggested. Sending InputCurrent() below 128mA or above 8.064A clears the register and terminates charging. Upon POR, the default input current limit is 4096mA.

The ACP and ACN pins are used to sense R_{AC} with a default value of 10mΩ. However, resistors of other values can also be used. With a larger sense resistor, comes a larger sense voltage, and a higher regulation accuracy; but, at the expense of higher conduction loss.

Instead of using the internal DPM loop, the user can build up an external input current regulation loop and have the feedback signal on ILIM. To disable the internal DPM loop, set the input current limit register value to a maximum 8.064A or a value much higher than the external DPM set point.

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If input current rises above 108% of the input current limit set point, the charger shuts down immediately to let the input current fall fast. After stopping charge, the charger soft restarts to charge the battery if the adapter still has power left to charge the battery. This prevents overloading the adapter to crash when system has a high and fast loading transient. The wait time between shut down and restart charging is a natural response time of the input current limit loop.

Table 6. Input Current Register (0x3FH), Using 10mΩ Sense Resistor

BIT	BIT NAME	DESCRIPTION
0	–	Not used.
1	–	Not used.
2	–	Not used.
3	–	Not used.
4	–	Not used.
5	–	Not used.
6	–	Not used.
7	Input Current, DACIIN 0	0 = Adds 0mA of input current. 1 = Adds 128mA of input current.
8	Input Current, DACIIN 1	0 = Adds 0mA of input current. 1 = Adds 256mA of input current.
9	Input Current, DACIIN 2	0 = Adds 0mA of input current. 1 = Adds 512mA of input current.
10	Input Current, DACIIN 3	0 = Adds 0mA of input current. 1 = Adds 1024mA of input current.
11	Input Current, DACIIN 4	0 = Adds 0mA of input current. 1 = Adds 2048mA of input current.
12	Input Current, DACIIN 5	0 = Adds 0mA of input current. 1 = Adds 4096mA of input current.
13	–	Not used.
14	–	Not used.
15	–	Not used.

Adapter Detect and $\overline{\text{ACOK}}$ Output

The IC uses an $\overline{\text{ACOK}}$ comparator to determine the source of power on the VCC pin, either from the battery or adapter. An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. The adapter detect threshold should typically be programmed to a value greater than the maximum battery voltage but lower than the maximum allowed adapter voltage.

The open drain $\overline{\text{ACOK}}$ output requires an external pull-up resistor to the system digital rail for a high level. It can be pulled to ground under the following conditions:

- V_{VCC} > UVLO;
- 2.4V < V_{ACDET} (not in low input voltage condition);
- V_{VCC}–V_{SRN} > 245mV (not in sleep mode);

The default delay is 1.3s for bq24707 and 1.2ms for bq24707A after ACDET has valid voltage to make $\overline{\text{ACOK}}$ pull low. It can be reduced by a SMBus command (ChargeOption() bit[15] = 0 $\overline{\text{ACOK}}$ delay 1.3s for bq24707 and 1.2ms for bq24707A, bit[15] = 1 $\overline{\text{ACOK}}$ no delay). To change this option, the VCC pin voltage must be above UVLO and the ACDET pin voltage must be above 0.6V to enable IC SMBus communication and set ChargeOption() bit[15] to 1 to disable the $\overline{\text{ACOK}}$ deglitch timer.

Enable and Disable Charging

In Charge mode, the following conditions have to be valid to start charge:

- Charge is enabled via SMBus (ChargeOption() bit [0] = 0, default is 0, charge enabled);
- ILIM pin voltage higher than 105mV;
- All three regulation limit DACs have a valid value programmed;

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- $\overline{ACOK}$ is valid (See the Adapter Detect and ACOK Output section for details);
- V_{SRN} does not exceed BATOVP threshold;
- IC temperature does not exceed TSHUT threshold;
- Not in ACOC condition (see the Input Over Current Protection (ACOC) section for details);

One of the following conditions stops on-going charging:

- Charge is inhibited via SMBus (ChargeOption() bit[0] = 1);
- ILIM pin voltage lower than 75mV;
- One of three regulation limit DACs is set to 0 or out of range;
- $\overline{ACOK}$ is pulled high (see the Adapter Detect and ACOK Output section for details);
- V_{SRN} exceeds BATOVP threshold;
- TSHUT IC temperature threshold is reached;
- ACOC is detected (see the Input Over Current Protection (ACOC) section for details);
- Short circuit is detected (see the Inductor Short, MOSFET Short Protection section for details);
- Watchdog timer expires if watchdog timer is enabled (see the Charger Timeout section for details);

Automatic Internal Soft-Start Charger Current

Every time charge is enabled, the charger automatically applies soft-start on charge current to avoid any overshoot or stress on the output capacitors or the power converter. The charge current starts at 128mA, and the step size is 64mA in CCM mode for a 10mΩ current sensing resistor. Each step lasts around 240µs in CCM mode, until it reaches the programmed charge current limit. No external components are needed for this function. During DCM mode, the soft-start current step size is larger and each step lasts for a longer time period due to the intrinsic slow response of DCM mode.

High Accuracy Current Sense Amplifier

As an industry standard, a high accuracy current sense amplifier (CSA) is used to monitor the input current or the charge current, selectable via SMBus (ChargeOption() bit[5] = 0 selects the input current, bit[5] = 1 selects the charge current) by the host. The CSA senses voltage across the sense resistor by a factor of 20 through the IOUT pin. Once VCC is above UVLO and ACDET is above 0.6V, CSA turns on and the IOUT output becomes valid. To lower the voltage on current monitoring, a resistor divider from IOUT to GND can be used and accuracy over temperature can still be achieved.

A 100pF capacitor connected on the output is recommended for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay.

Charge Timeout

The IC includes a watchdog timer to terminate charging if the charger does not receive a write ChargeVoltage() or write ChargeCurrent() command within 175s (adjustable via ChargeOption() command). If a watchdog timeout occurs all register values stay unchanged but charge is suspended. Write ChargeVoltage() or write ChargeCurrent() commands must be re-sent to reset the watchdog timer and resume charging. The watchdog timer can be disabled, or set to 44s, 88s, or 175s via a SMBus command (ChargeOption() bit[14:13]). After watchdog timeout write ChargeOption() bit[14:13] to disable the watchdog timer also resume charging.

Converter Operation

The synchronous buck PWM converter uses a fixed frequency voltage mode control scheme and internal type III compensation network. The LC output filter generates the following characteristic resonant frequency:

$$f_o = \frac{1}{2\pi \sqrt{L_o C_o}} \tag{3}$$

The resonant frequency f_o is used to determine the compensation to ensure there is sufficient phase margin and gain margin for the target bandwidth. The LC output filter should be selected to generate a resonant frequency of 10–20 kHz nominal for the best performance. The suggested component values per charge current with a 750kHz default switching frequency is shown in Table 7.

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Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

Table 7. Suggested Component Values per Charge Current with a Default 750kHz Switching Frequency

Charge Current	2A	3A	4A	6A	8A
Output inductor Lo (μH)	6.8 or 8.2	5.6 or 6.8	3.3 or 4.7	3.3	2.2
Output capacitor Co (μF)	20	20	20	30	40
Sense resistor (mΩ)	10	10	10	10	10

The IC has three loops of regulation: input current, charge current, and charge voltage. The three loops are brought together internally at the error amplifier. The maximum voltage of the three loops appears at the output of the error amplifier EAO (see Figure 15). An internal saw-tooth ramp is compared to the internal error control signal EAO to vary the duty-cycle of the converter. The ramp has an offset of 200mV in order to allow 0% duty-cycle.

When the battery charge voltage approaches the input voltage, the EAO signal is allowed to exceed the saw-tooth ramp peak in order to get a 100% duty-cycle. If voltage across the BTST and PHASE pins falls below 4.3V, a refresh cycle starts and the low-side n-channel power MOSFET is turned on to recharge the BTST capacitor. It can achieve a duty-cycle of up to 99.5%.

Continuous Conduction Mode (CCM)

With sufficient charge current the IC inductor current never crosses zero, which is defined as continuous conduction mode. The controller starts a new cycle with ramp coming up from 200mV. As long as EAO voltage is above the ramp voltage, the high-side MOSFET (HSFET) stays on. When the ramp voltage exceeds EAO voltage, the HSFET turns off and the low-side MOSFET (LSFET) turns on. At the end of the cycle, the ramp gets reset and the LSFET turns off, ready for the next cycle. There is always break-before-make logic during the transition to prevent cross-conduction and shoot-through. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM mode, the inductor current is always flowing and creates a fixed two-pole system. Having the LSFET turn-on keeps the power dissipation low and allows safely charging at high currents.

Discontinuous Conduction Mode (DCM)

During the HSFET off time when LSFET is on, the inductor current decreases. If the current goes to zero, the converter enters Discontinuous Conduction Mode. Every cycle, when the voltage across SRP and SRN falls below 5mV (0.5A on 10mΩ), the under-current-protection comparator (UCP) turns off LSFET to avoid negative inductor current, which may boost the system via the body diode of HSFET.

During the DCM mode the loop response automatically changes. It changes to a single pole system and the pole is proportional to the load current.

Both CCM and DCM are synchronous operation with LSFET turn-on every clock cycle. If the average charge current goes below 125mA on 10mΩ current sensing resistor or the battery voltage falls below 2.5V, the LSFET keeps turn-off. The battery charger operates in non-synchronous mode and the current flows through the LSFET body diode. During non-synchronous operation, the LSFET turns on only for refreshing pulse to charge BTST capacitor. If the average charge current goes above 250mA on 10mΩ current sensing resistor, the LSFET exits non-synchronous mode and enters synchronous mode to reduce LSFET power loss.

Input Over Current Protection (ACOC)

The IC cannot maintain the input current level if the charge current has been already reduced to zero. After the system current continues increasing to the 1.66X of input current DAC set point (with 2.5ms blank out time), $\overline{\text{IFAULT}}$ is pulled to low and the charge is disabled for 1.3s and will soft start again for charge if ACOC condition goes away. If such failure is detected seven times in 90 seconds, charge will be latched off and an adapter removal and system shut down (make ACDET < 0.6V to reset IC) is required to start charge again. After 90 seconds, the failure counter will be reset to zero to prevent latch off.

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The ACOC function can be disabled or the threshold can be set to 1.33X, 1.66X or 2.22X of input DPM current via SMBus command (ChargeOption() bit [2:1]).

Charge Over Current Protection (CHGOCP)

The IC has a cycle-by-cycle peak over-current protection. It monitors the voltage across SRP and SRN, and prevents the current from exceeding of the threshold based on the DAC charge current set point. The high-side gate drive turns off for the rest of the cycle when the over-current is detected, and resumes when the next cycle starts.

The charge OCP threshold is automatically set to 6A, 9A, and 12A on a 10mΩ current sensing resistor based on charge current register value. This prevents the threshold to be too high which is not safe or too low which can be triggered in normal operation. Proper inductance should be selected to prevent OCP triggered in normal operation due to high inductor current ripple.

Battery Over Voltage Protection (BATOVP)

The IC will not allow the high-side and low-side FET to turn-on when the battery voltage at SRN exceeds 104% of the regulation voltage set-point. If BATOVP last over 30ms, charger is completely disabled. This allows quick response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected. A 4mA current sink from SRN to GND is on only during BATOVP and allows discharging the stored output inductor energy that is transferred to the output capacitors.

Some battery pack gas gauges will set the ChargeVoltage() and ChargeCurrent() registers to 0V and 0A after the battery pack is fully charged. If the ChargeVoltage() register is set to 0V, the bq24707 triggers BATOVP, and the 4mA current discharges the battery pack. The recommendation for bq24707 is to set the ChargeVoltage() register to full scale charge voltage (12.592V for 3S battery for example) after the battery is fully charged. The bq24707A will not trigger BATOVP, and there is no 4mA current to discharge the battery pack if the ChargeVoltage() register is set 0V. The recommendation for bq24707A is to set the ChargeVoltage() register to 0V after the battery is fullycharged.

Battery Shorted to Ground (BATLOWV)

The IC will disable charge for 1ms if the battery voltage on SRN falls below 2.5V. After 1ms reset, the charge is resumed with soft-start if all the enable conditions in the Enable and Disable Charging sections are satisfied. This prevents any overshoot current in inductor which can saturate inductor and may damage the MOSFET. The charge current is limited to 0.5A on 10mΩ current sensing resistor when BATLOWV condition persists and LSFET keeps off. The LSFET turns on only for refreshing pulse to charge BTST capacitor.

Thermal Shutdown Protection (TSHUT)

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off for self-protection whenever the junction temperature exceeds the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shut down, the REGN LDO current limit is reduced to 16mA. Once the temperature falls below 135°C, charge can be resumed with soft start.

EMI Switching Frequency Adjust

The charger switching frequency can be adjusted ±18% to solve EMI issue via SMBus command. ChargeOption() bit [9]=0 disable the frequency adjust function. To enable frequency adjust function, set ChargeOption() bit[9]=1. Set ChargeOption() bit [10]=0 to reduce switching frequency, set bit[10]=1 to increase switching frequency.

If frequency is reduced, for a fixed inductor the current ripple is increased. Inductor value must be carefully selected so that it will not trig cycle-by-cycle peak over current protection even for the worst condition such as higher input voltage, 50% duty cycle, lower inductance and lower switching frequency.

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Inductor Short, MOSFET Short Protection

The IC has a unique short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across $R_{DS(on)}$ of the MOSFETs after a certain amount of blanking time. In case of MOSFET short or inductor short circuit, the over current condition is sensed by two comparators and two counters will be triggered. After seven times of short circuit events, the charger will be latched off. To reset the charger from latch-off status, the IC VCC pin must be pulled down below UVLO or ACDET pin must be pulled down below 0.6V. This can be achieved by removing the adapter and shut down the operation system. The low side MOSFET short circuit voltage drop threshold is fixed to typical 110mV. The high side MOSFET short circuit voltage drop threshold can be adjusted via SMBus command. ChargeOption() bit[8:7] = 00, 01, 10, 11 set the threshold 300mV, 500mV, 700mV and 900mV respectively.

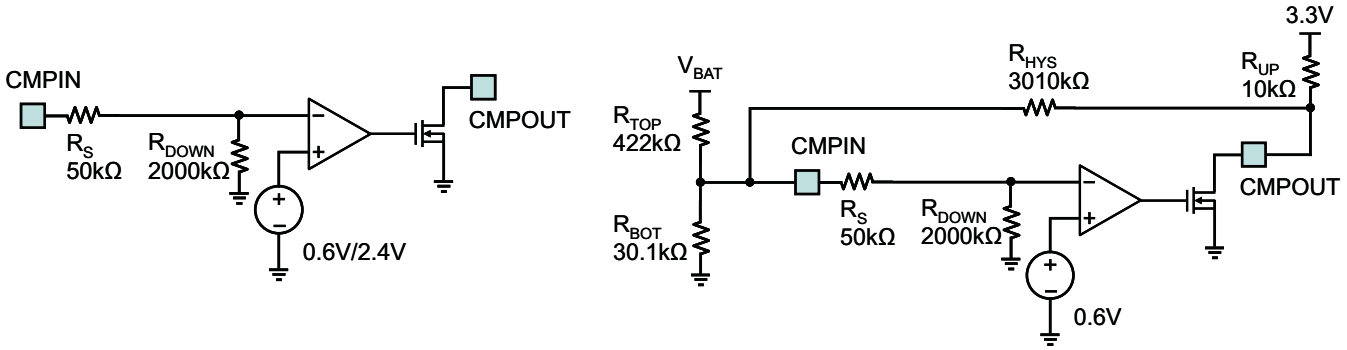
Due to the certain amount of blanking time to prevent noise when MOSFET just turns on, the cycle-by-cycle charge over-current protection may detect high current and turn off MOSFET first before the short circuit protection circuit can detect short condition because the blanking time has not finished. In such a case the charge may not be able to detect shorts circuit and counter may not be able to count to seven then latch off. Instead the charge may continuously keep switching with very narrow duty cycle to limit the cycle-by-cycle current peak value. However, the charger should still be safe and will not cause failure because the duty cycle is limited to a very short of time and MOSFET should be still inside the safety operation area. During a soft start period, it may takes long time instead of just seven switching cycles to detect short circuit based on the same blanking time reason.

Independent Comparator

The IC has an independent comparator can be used to compare input current, charge current or battery voltage with internal reference . Program CMPIN voltage by connecting a resistor divider from IOUT pin to CMPIN pin to GND pin for adapter or charge current comparison or from SRN pin to CMPIN pin to GND pin for battery voltage comparison. When CMPIN is above internal reference, CMPOUT is pulled to external pull up rail by external pull up resistor. When CMPIN is below internal reference, CMPOUT is pulled to GND by internal MOSFET. Place a resistor between CMPIN and CMPOUT to program hysteresis. The internal reference can be set to 0.6V or 2.4V via SMBus command (ChargeOption() bit[4]=0 set internal reference 0.6V, bit[4]=1 set 2.4V).

There is one 50kΩ series resistor R_S and one 2000kΩ pull down resistor R_{DOWN} for CMPIN pin as shown in Figure 19. To get the accurate comparison set point, these two resistors must be included in the calculation. A spreadsheet calculation tool has been developed to simplify the design work. User can down load from the TI Web site at www.ti.com under the IC product folder.

Figure 19 also shows one application circuit using this comparator for battery voltage comparison. After using the superposition principle and fill the components value into the spreadsheet the battery voltage threshold is 9.45V for rising edge and 8.99V for falling edge.



(a) Internal Circuit showing the series resistor and pull down resistor

(b) Application Circuit, 9.45V rising edge and 8.99V falling edge for 3cell battery

Figure 19. IC Comparator Internal Circuit and Application Circuit

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Table 8. Component List for Typical System Circuit of Figure 1

PART DESIGNATOR	QTY	DESCRIPTION
C1, C2, C3, C13, C14	5	Capacitor, Ceramic, 0.1µF, 25V, 10%, X7R, 0603
C4	1	Capacitor, Ceramic, 100pF, 25V, 10%, X7R, 0603
C5, C6	2	Capacitor, Ceramic, 1µF, 25V, 10%, X7R, 0603
C7	1	Capacitor, Ceramic, 0.047µF, 25V, 10%, X7R, 0603
C8, C9, C10, C11	4	Capacitor, Ceramic, 10µF, 25V, 10%, X7R, 1206
Ci	1	Capacitor, Ceramic, 2.2µF, 25V, 10%, X7R, 1210
Csys	1	Capacitor, Electrolytic, 220µF, 25V
D1	1	Diode, Schottky, 30V, 200mA, SOT-23, Fairchild, BAT54
D2	1	Diode, Schottky, 40V, 120mA, SOD-323, NXP, RB751V40
Q1, Q2, Q5	3	P-channel MOSFET, –30V, –9.4A, SO-8, Vishay Siliconix, Si4435DDY
Q3, Q4	2	N-channel MOSFET, 30V, 12A, PowerPAK 1212-8, Vishay Siliconix, SiS412DN
L1	1	Inductor, SMT, 4.7µH, 5.5A, Vishay Dale, IHLP2525CZER4R7M01
R1	1	Resistor, Chip, 430kΩ, 1/10W, 1%, 0603
R2	1	Resistor, Chip, 66.5kΩ, 1/10W, 1%, 0603
R3, R4, R5, R6, R10	5	Resistor, Chip, 10kΩ, 1/10W, 1%, 0603
R7	1	Resistor, Chip, 316kΩ, 1/10W, 1%, 0603
R8, R12	2	Resistor, Chip, 100kΩ, 1/10W, 1%, 0603
R9	1	Resistor, Chip, 10Ω, 1/4W, 1%, 1206
R11	1	Resistor, Chip, 39.2kΩ, 1/10W, 1%, 0603
R13	1	Resistor, Chip, 3.01MΩ, 1/10W, 1%, 0603
R14	1	Resistor, Chip, 10 Ω, 1/10W, 5%, 0603
R15	1	Resistor, Chip, 7.5 Ω, 1/10W, 5%, 0603
RAC, RSR	2	Resistor, Chip, 0.01Ω, 1/2W, 1%, 1206
Ri	1	Resistor, Chip, 2Ω, 1/2W, 1%, 1210
U1	1	Charger controller, 20 pin VQFN, TI, bq24707RGR or bq24707ARGR

APPLICATION INFORMATION

Negative Output Voltage Protection

Reversely insert the battery pack into the charger output during production or hard shorts on battery to ground will generate negative output voltage on SRP and SRN pin. IC internal electrostatic-discharge (ESD) diodes from GND pin to SRP or SRN pins and two anti-parallel (AP) diodes between SRP and SRN pins can be forward biased and negative current can pass through the ESD diodes and AP diodes when output has negative voltage. Insert two small resistors for SRP and SRN pins to limit the negative current level when output has negative voltage. Suggest resistor value is 10Ω for SRP pin and 7-8Ω for SRN pin. After adding small resistors, the suggested pre-charge current is at least 192mA for a 10mΩ current sensing resistor.

Inductor Selection

The IC has three selectable fixed switching frequencies. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (4)$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (f_S) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \quad (5)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9V to 12.6V for 3-cell battery pack. For 20V adapter voltage, 10V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12V to 16.8V, and 12V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

The IC has charge under current protection (UCP) by monitoring charging current sensing resistor cycle-by-cycle. The typical cycle-by-cycle UCP threshold is 5mV falling edge corresponding to 0.5A falling edge for a 10mΩ charging current sensing resistor. When the average charging current is less than 125mA for a 10mΩ charging current sensing resistor, the low side MOSFET is off until BTST capacitor voltage needs to refresh charge. As a result, the converter relies on low side MOSFET body diode for the inductor freewheeling current.

Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by Equation 6:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{6}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred for 19-20V input voltage. 10-20µF capacitance is suggested for typical of 3-4A charging current.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{7}$$

The IC has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 10 kHz and 20 kHz. The preferred ceramic capacitor is 25V X7R or X5R for output capacitor. 10-20µF capacitance is suggested for typical of 3-4A charging current. Place capacitors after charging current sensing resistor to get the best charge current regulation accuracy.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

Power MOSFETs Selection

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6V of gate drive voltage. 30V or higher voltage rating MOSFETs are preferred for 19-20V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD}; \; FOM_{bottom} = R_{DS(on)} \times Q_G \tag{8}$$

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The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance ®$_{DS(ON)}$), input voltage (V_{IN}), switching frequency (f_S), turn on time (t_{on}) and turn off time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_{on} + t_{off}) \times f_s \quad (9)$$

The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100°C junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}} \quad (10)$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current and I_{off} is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \quad (11)$$

Gate driving current can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}) and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \quad (12)$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

$$P_{bottom} = (1 - D) \times I_{CHG}^2 \times R_{DS(on)} \quad (13)$$

When charger operates in non-synchronous mode, the bottom-side MOSFET is off. As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The body diode power loss depends on its forward voltage drop (V_F), non-synchronous mode charging current ($I_{NONSYNC}$), and duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D) \quad (14)$$

The maximum charging current in non-synchronous mode can be up to 0.25A for a 10mΩ charging current sensing resistor or 0.5A if battery voltage is below 2.5V. The minimum duty cycle happens at lowest battery voltage. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at VCC pin maybe beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent over voltage event on VCC pin.

There are several methods to damping or limit the over voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over voltage level to an IC safe level. However these two solutions may not have low cost or small size.

A cost effective and small size solution is shown in Figure 20. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result the over voltage spike is limited to a safe level. D1 is used for reverse voltage protection for VCC pin. C2 is VCC pin decoupling capacitor and it should be place to VCC pin as close as possible. C2 value should be less than C1 value so R1 can dominant the equivalent ESR value to get enough damping effect. R2 is used to limit inrush current of D1 to prevent D1 getting damage when adapter hot plug-in. R2 and C2 should have 10us time constant to limit the dv/dt on VCC pin to reduce inrush current when adapter hot plug in. R1 has high inrush current. R1 package must be sized enough to handle inrush current power loss according to resistor manufacturer's datasheet. The filter components value always need to be verified with real application and minor adjustments may need to fit in the real application circuit.

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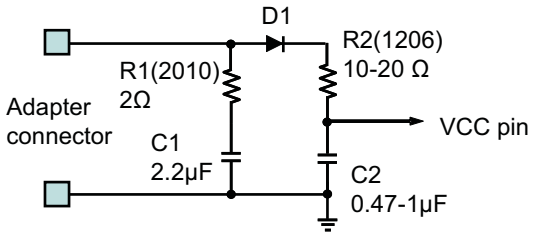


Figure 20. Input Filter

IC Design Guideline

The IC has a unique short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across Rdson of the MOSFETs after a certain amount of blanking time. In case of MOSFET short or inductor short circuit, the over current condition is sensed by two comparators and two counters will be triggered. After seven times of short circuit events, the charger will be latched off. The way to reset the charger from latch-off status is reconnect adapter. Figure 21 shows the IC short circuit protection block diagram.

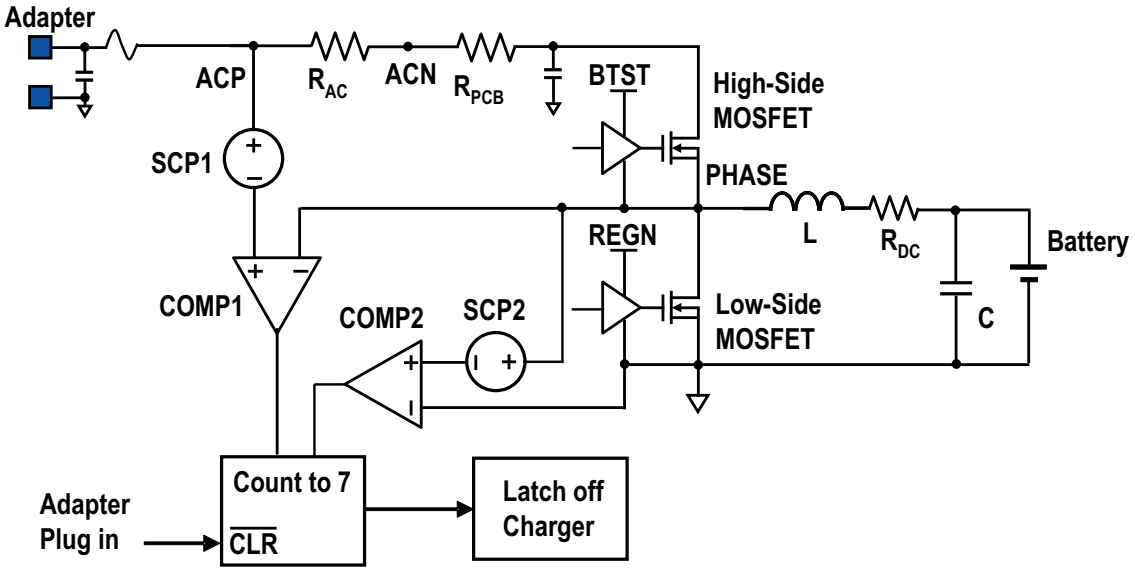


Figure 21. Block Diagram of IC Short Circuit Protection

In normal operation, low side MOSFET current is from source to drain which generates negative voltage drop when it turns on, as a result the over current comparator can not be triggered. When high side switch short circuit or inductor short circuit happens, the large current of low side MOSFET is from drain to source and can trig low side switch over current comparator. IC senses low side switch voltage drop by PHASE pin and GND pin.

The high-side FET short is detected by monitoring the voltage drop between ACP and PHASE. As a result, it not only monitors the high side switch voltage drop, but also the adapter sensing resistor voltage drop and PCB trace voltage drop from ACN terminal of RAC to charger high side switch drain. Usually, there is a long trance between input sensing resistor and charger converting input, a careful layout will minimize the trace effect.

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To prevent unintentional charger shut down in normal operation, MOSFET $R_{DS(on)}$ selection and PCB layout is very important. Figure 22 shows a need improve PCB layout example and its equivalent circuit. In this layout, system current path and charger input current path is not separated, as a result, the system current causes voltage drop in the PCB copper and is sensed by IC. The worst layout is when a system current pull point is after charger input; as a result all system current voltage drops are counted into over current protection comparator. The worst case for IC is the total system current and charger input current sum equals DPM current. When system pull more current, the charger IC try to regulate R_{AC} current as a constant current by reducing charging current.

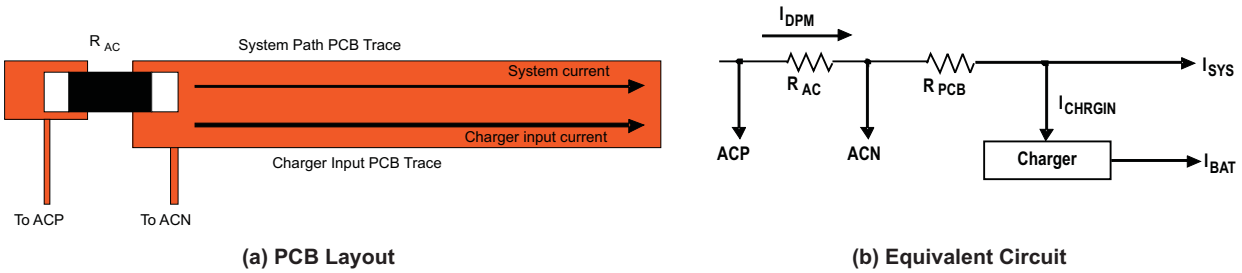


Figure 22. Need Improve PCB Layout Example

Figure 23 shows the optimized PCB layout example. The system current path and charge input current path is separated, as a result the IC only senses charger input current caused PCB voltage drop and minimized the possibility of unintentional charger shut down in normal operation. This also makes PCB layout easier for high system current application.

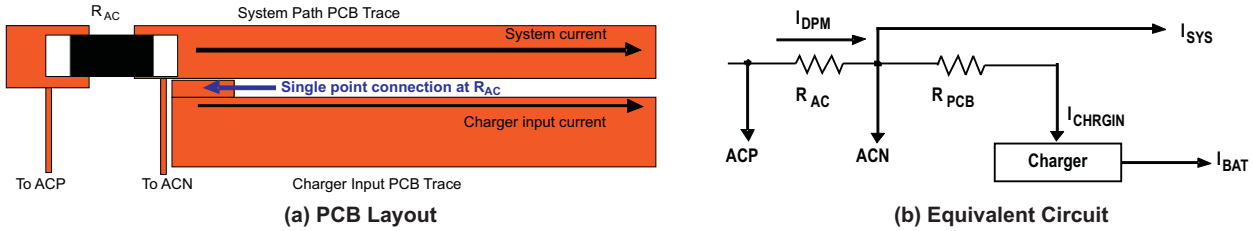


Figure 23. Optimized PCB Layout Example

The total voltage drop sensed by IC can be express as the following equation.

$$V_{top} = R_{AC} \times I_{DPM} + R_{PCB} \times (I_{CHRGIN} + (I_{DPM} - I_{CHRGIN}) \times k) + R_{DS(on)} \times I_{PEAK} \quad (15)$$

where the R_{AC} is the AC adapter current sensing resistance, I_{DPM} is the DPM current set point, R_{PCB} is the PCB trace equivalent resistance, I_{CHRGIN} is the charger input current, k is the PCB factor, $R_{DS(on)}$ is the high side MOSFET turn on resistance and I_{PEAK} is the peak current of inductor. Here the PCB factor k equals 0 means the best layout shown in Figure 23 where the PCB trace only goes through charger input current while k equals 1 means the worst layout shown in Figure 22 where the PCB trace goes through all the DPM current. The total voltage drop must below the high side short circuit protection threshold to prevent unintentional charger shut down in normal operation.

The low side MOSFET short circuit voltage drop threshold is fixed to typical 110mV. The high side MOSFET short circuit voltage drop threshold can be adjusted via SMBus command. ChargeOption() bit[8:7] = 00, 01, 10, 11 set the threshold 300mV, 500mV, 700mV and 900mV respectively. For a fixed PCB layout, host should set proper short circuit protection threshold level to prevent unintentional charger shut down in normal operation.

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PCB Layout

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 24) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to switching MOSFET's supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
2. The IC should be placed close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching MOSFETs.
3. Place inductor input terminal to switching MOSFET's output terminal as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 25 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC
5. Place output capacitor next to the sensing resistor output and ground
6. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling
8. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground (power pad should tie to analog ground in this case if possible).
9. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible
10. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
11. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the QFN information, See SCBA017 and SLUA271.

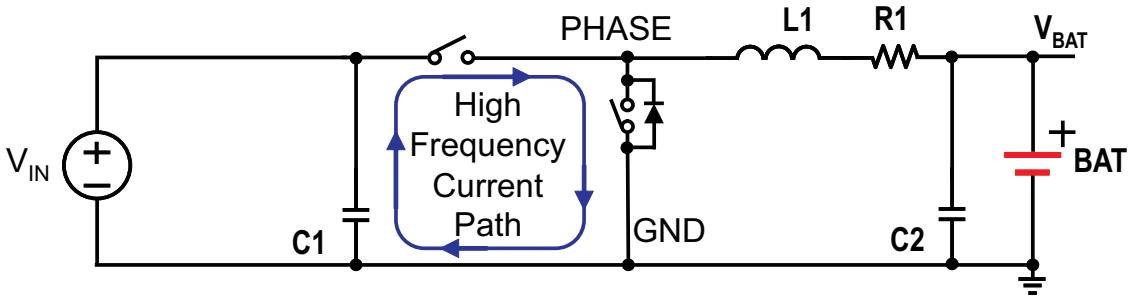


Figure 24. High Frequency Current Path

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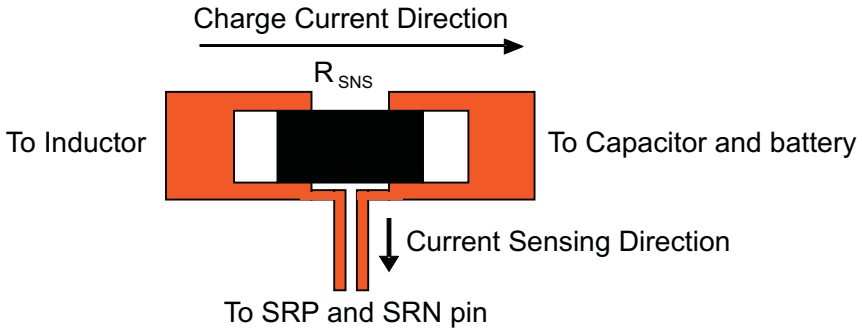


Figure 25. Sensing Resistor PCB Layout

REVISION HISTORY

Changes from Original (July 2010) to Revision A **Page**

- Changed the Functional Block Diagram, Figure 1 2
- Updated the description for the SRN and SRP pins 10
- Deleted C12, added R14 and R15 in Table 8 23
- Added Added section: Negative Output Voltage Protection 23

Changes from Revision A (November 2010) to Revision B **Page**

- Added Features for the bq24707 and bq24707A 1
- Added device bq24707A to this data sheet 1
- Added bq24707A to the ORDERING INFORMATION table 2
- Added the COMPARISON TABLE 2
- Added bq24707 only to the test condition of $t_{ACOK_FALL_DEG}$ first row 5
- Added bq24707A only to the test condition of $t_{ACOK_FALL_DEG}$ second row 5
- Added (bq24707) to the title of Figure 3 8
- Changed the Description of the $\overline{ACOK}$ Deglitch Time Adjust bit in Table 3 15
- Changed the Adapter Detect and $\overline{ACOK}$ Output section. included 1.3s for bq24707 and 1.2ms for bq24707A 18
- Added a new paragraph in the Battery Over Voltage Protection (BATOVP) section 21
- Changed the Description of item U1 in Table 8 23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ24707ARGRR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ07A	Samples
BQ24707ARGRT	ACTIVE	VQFN	RGR	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ07A	Samples
BQ24707RGRR	ACTIVE	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ707	Samples
BQ24707RGRT	ACTIVE	VQFN	RGR	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ707	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

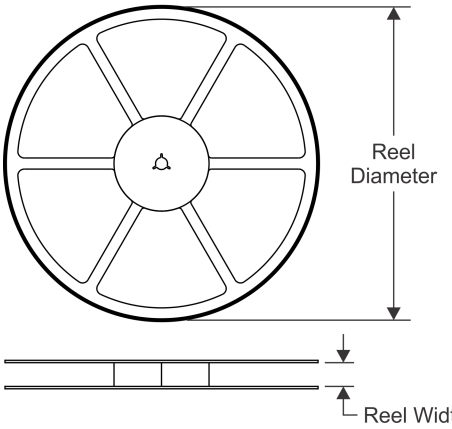
(4) Only one of markings shown within the brackets will appear on the physical device.

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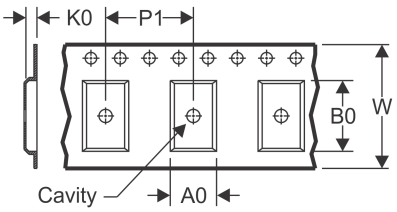
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

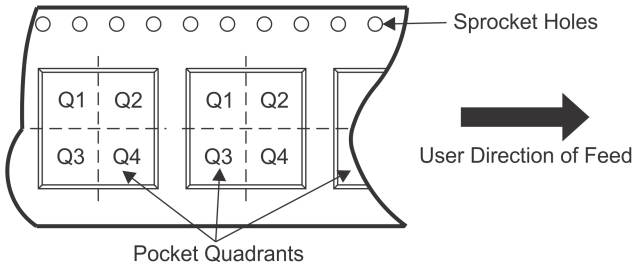


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

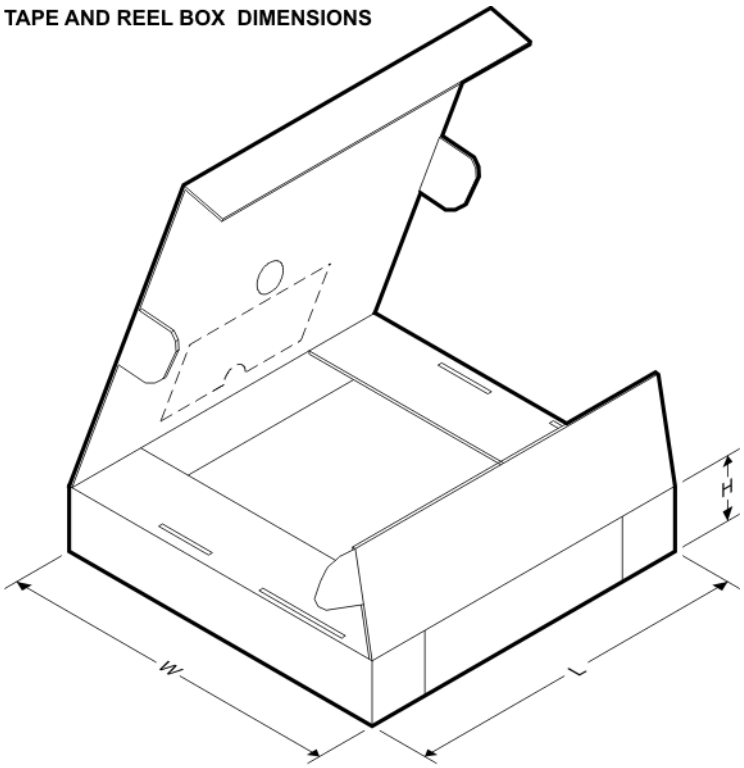
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24707ARGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24707ARGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24707ARGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24707ARGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24707RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24707RGRR	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24707RGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24707RGRT	VQFN	RGR	20	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

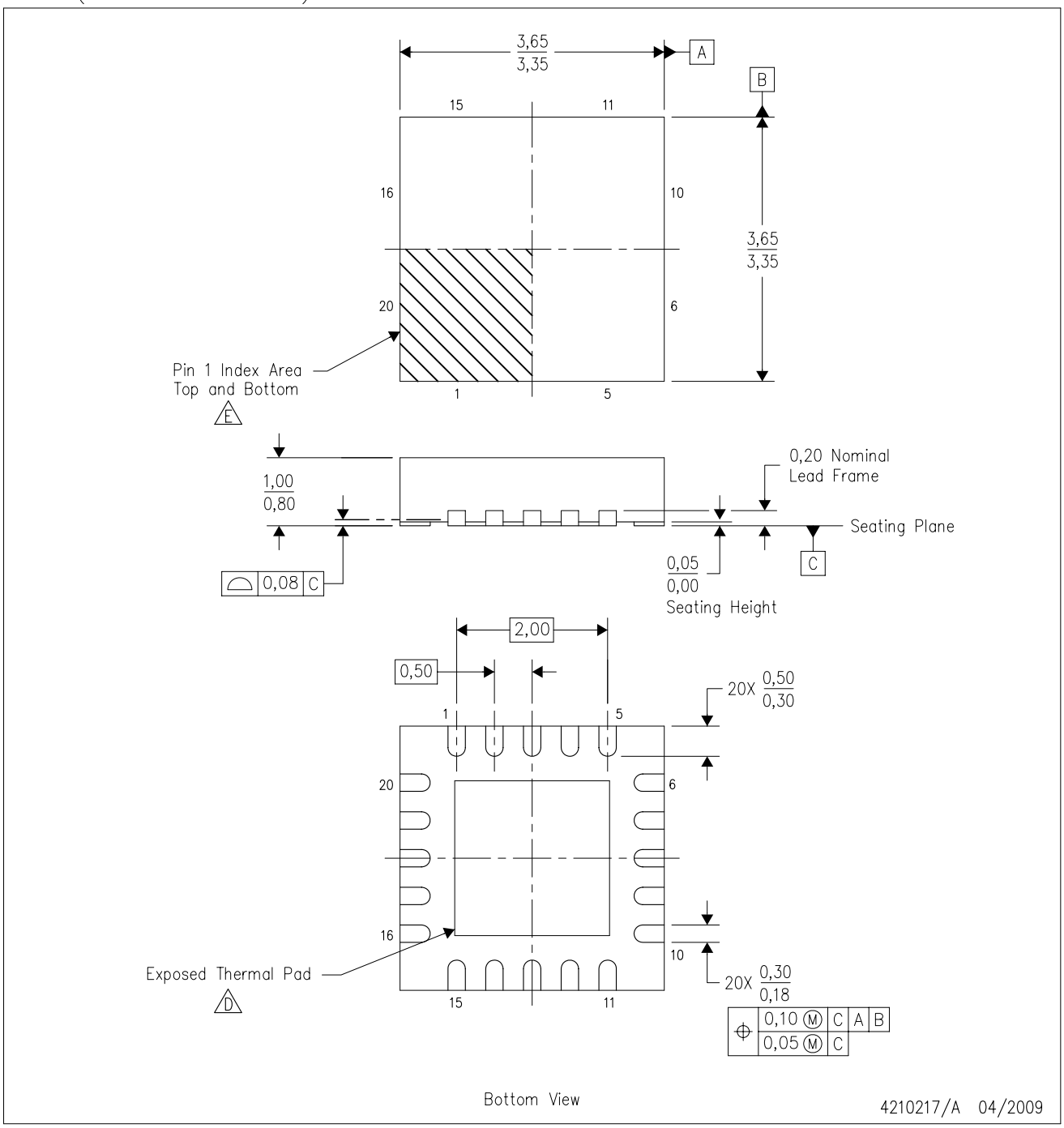
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24707ARGRR	VQFN	RGR	20	3000	552.0	367.0	36.0
BQ24707ARGRR	VQFN	RGR	20	3000	367.0	367.0	35.0
BQ24707ARGRT	VQFN	RGR	20	250	210.0	185.0	35.0
BQ24707ARGRT	VQFN	RGR	20	250	552.0	185.0	36.0
BQ24707RGRR	VQFN	RGR	20	3000	367.0	367.0	35.0
BQ24707RGRR	VQFN	RGR	20	3000	552.0	367.0	36.0
BQ24707RGRT	VQFN	RGR	20	250	210.0	185.0	35.0
BQ24707RGRT	VQFN	RGR	20	250	552.0	185.0	36.0

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

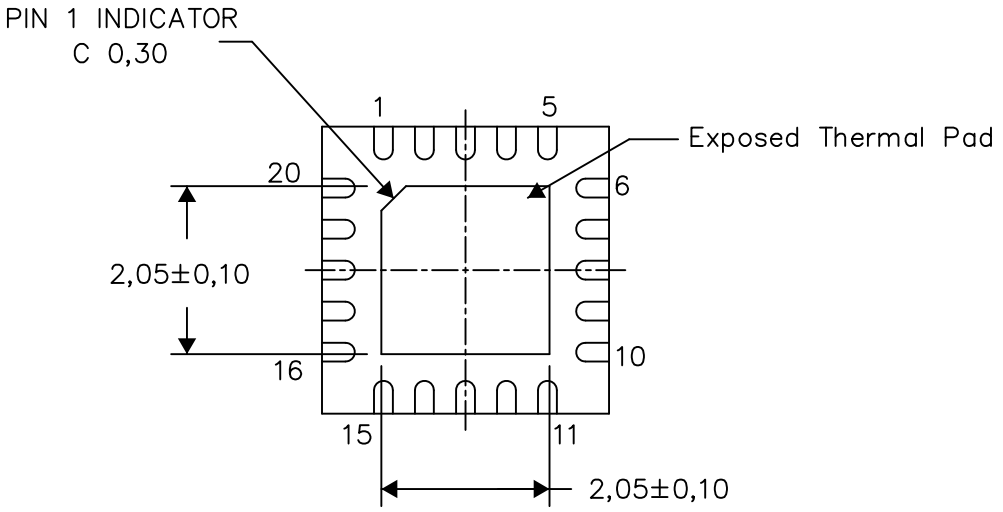
RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



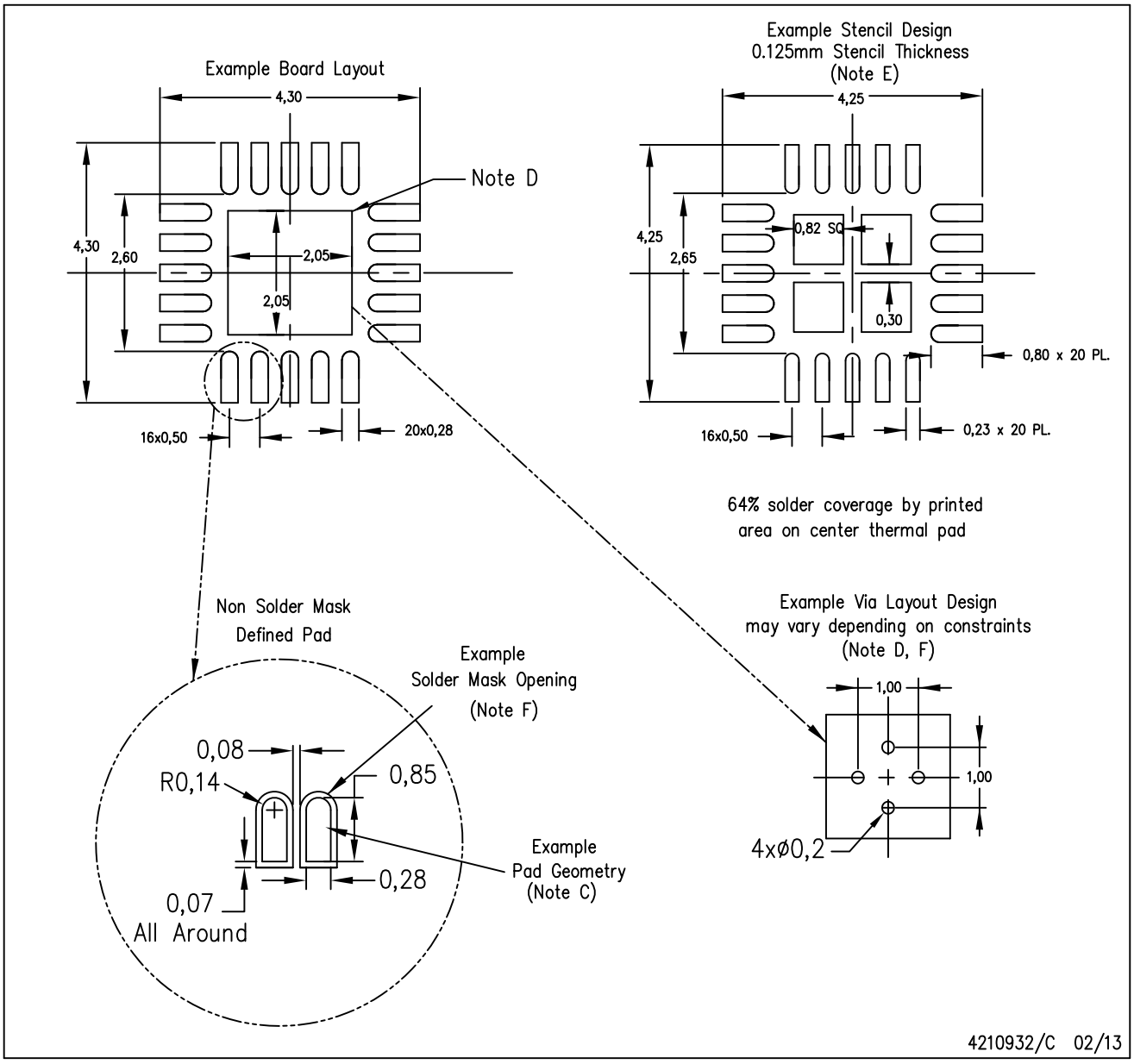
Bottom View

Exposed Thermal Pad Dimensions

4210218/D 02/13

NOTE: All linear dimensions are in millimeters

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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