N-Channel JFETs

J111 SST111
J112 SST112
J113 SST113

PRODUCT SUMMARY				
Part Number	**$V_{GS(off)}$ (V)**	**$r_{DS(on)}$ Max (Ω)**	**$I_{D(off)}$ Typ (pA)**	**t_{ON} Typ (ns)**
J/SST111	–3 to –10	30	5	4
J/SST112	–1 to –5	50	5	4
J/SST113	≤ –3	100	5	4

FEATURES

- Low On-Resistance: 111 < 30 Ω
- Fast Switching—t_{ON}: 4 ns
- Low Leakage: 5 pA
- Low Capacitance: 3 pF
- Low Insertion Loss

BENEFITS

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible “Off-Error,” Excellent Accuracy
- Good Frequency Response, Low Glitches
- Eliminates Additional Buffering

APPLICATIONS

- Analog Switches
- Choppers
- Sample-and-Hold
- Normally “On” Switches
- Current Limiters

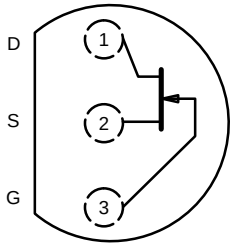
DESCRIPTION

The J/SST111 series consists of all-purpose analog switches designed to support a wide range of applications. The J/SST113 are useful in a high-gain amplifier mode.

The J series, TO-226AA (TO-92) plastic package, provides low cost, while the SST series, TO236 (SOT-23) package, provides surface-mount capability. Both the J and SST series are available in tape-and-reel for automated assembly (see Packaging Information).

For similar products in TO-206AA(TO-18) packaging, see the 2N/PN/SST4391 series, 2N4856A/4857A/4858A, and 2N5564/5565/5566 (duals) data sheets.

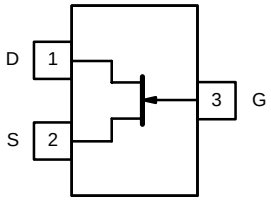
TO-226AA (TO-92)



Top View

J111
J112
J113

TO-236 (SOT-23)



Top View

SST111 (C1)*
SST112 (C2)*
SST113 (C3)*

*Marking Code for TO-236

ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage . . . . . –35 V
Gate Current . . . . . 50 mA
Lead Temperature ($^1/_{16}$” from case for 10 seconds) . . . . . 300 °C
Storage Temperature . . . . . –55 to 150°C
Operating Junction Temperature . . . . . –55 to 150°C

Power Dissipation[a]
(TO-236) . . . . . 350 mW
(TO-226AA) . . . . . 360 mW

Notes
a. Derate 2.8 mW/°C above 25°C

For applications information see AN105.

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

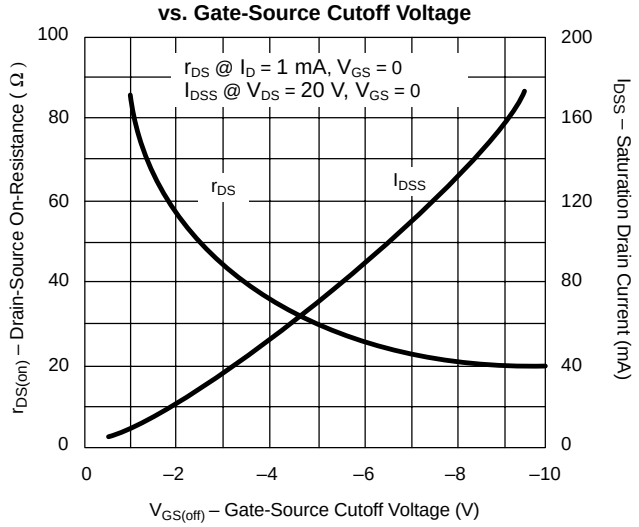
Parameter	Symbol	Test Conditions	Typ[a]	Limits J/SST111 Min	J/SST111 Max	J/SST112 Min	J/SST112 Max	J/SST113 Min	J/SST113 Max	Unit
Static										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 μA , V_{DS} = 0 V	–55	–35		–35		–35		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 5 V, I_D = 1 μA		–3	–10	–1	–5		–3	
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		20		5		2		mA
Gate Reverse Current	I_{GSS}	V_{GS} = –15 V, V_{DS} = 0 V	–0.005		–1		–1		–1	nA
		T_A = 125°C	–3							
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	–5							pA
Drain Cutoff Current	$I_{D(off)}$	V_{DS} = 5 V, V_{GS} = –10 V	0.005		1		1		1	nA
		T_A = 125°C	3							
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS} = 0 V, V_{DS} = 0.1 V			30		50		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V	0.7							V
Dynamic										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, I_D = 1 mA f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							μS
Drain-Source On-Resistance	$r_{ds(on)}$	V_{GS} = 0 V, I_D = 0 mA f = 1 kHz			30		50		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = –10 V f = 1 MHz	7		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		5		5		5	
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = 10 V, I_D = 1 mA f = 1 kHz	3							$\frac{nV}{\sqrt{Hz}}$
Switching										
Turn-On Time	$t_{d(on)}$	V_{DD} = 10 V, $V_{GS(H)}$ = 0 V See Switching Circuit	2							ns
	t_r		2							
Turn-Off Time	$t_{d(off)}$		6							
	t_f		15							

Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤300 μs duty cycle ≤3%.

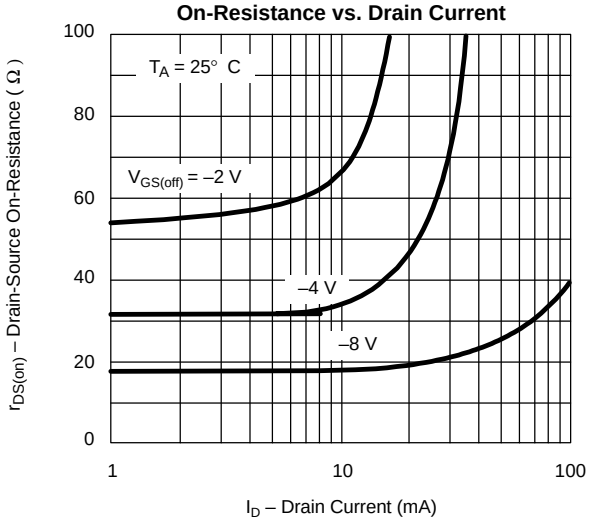
NCB

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

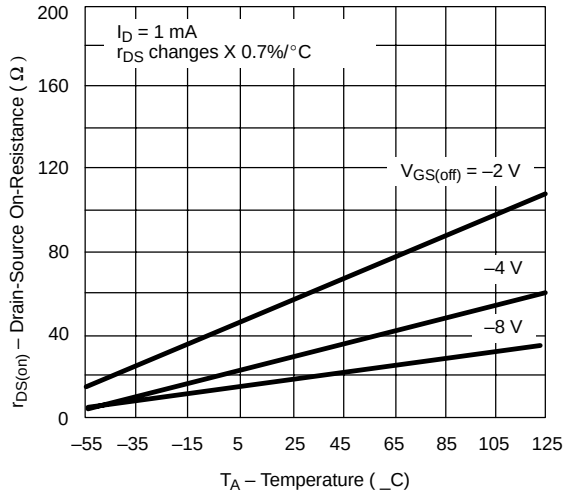
On-Resistance and Drain Current vs. Gate-Source Cutoff Voltage



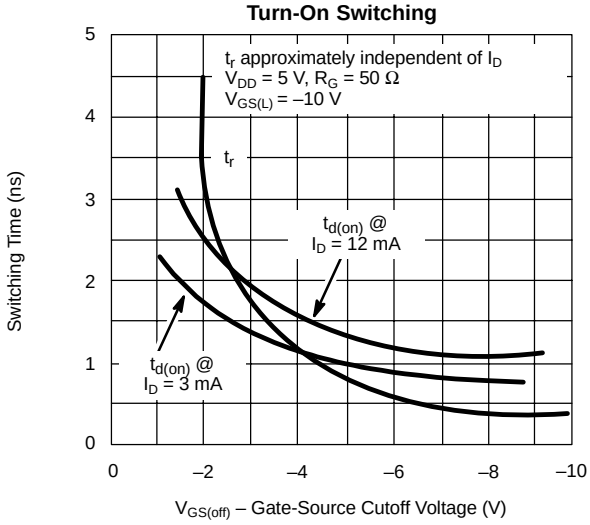
On-Resistance vs. Drain Current



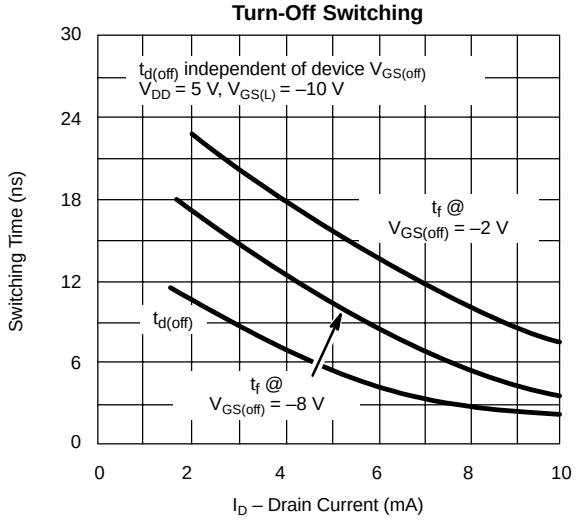
On-Resistance vs. Temperature



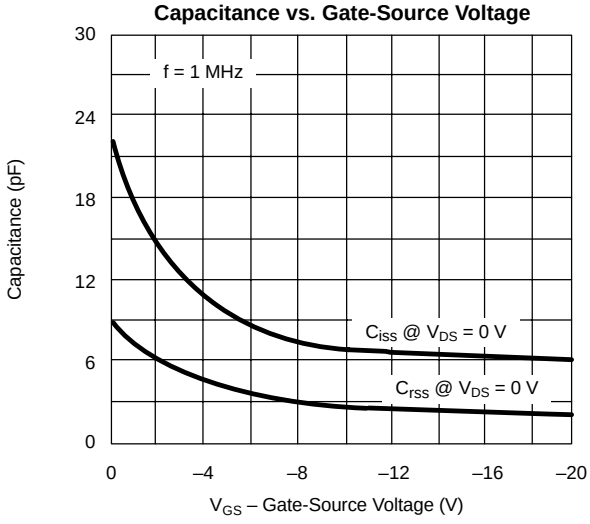
Turn-On Switching



Turn-Off Switching

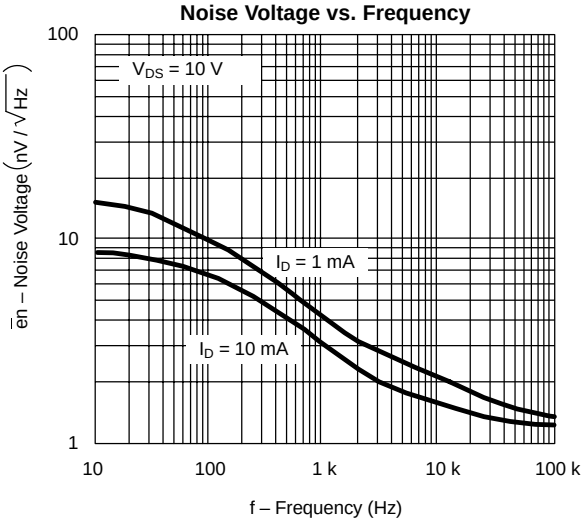


Capacitance vs. Gate-Source Voltage

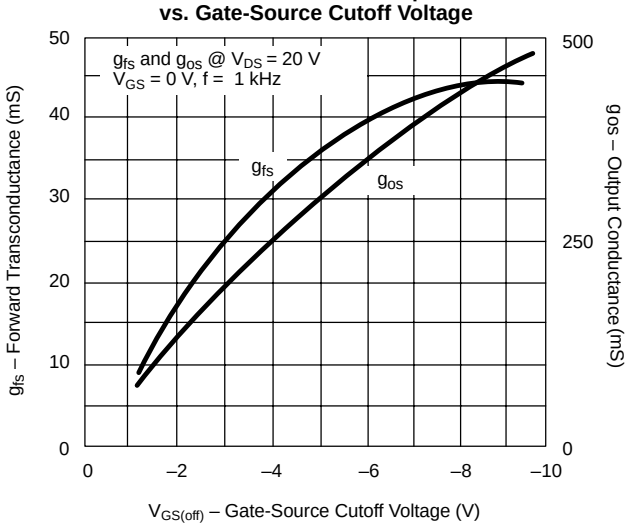


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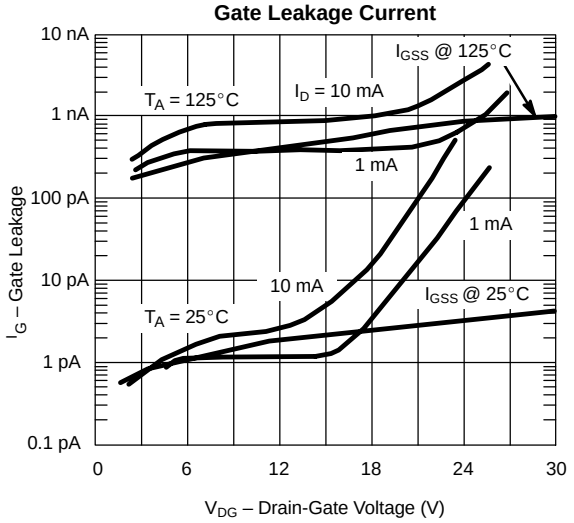
Noise Voltage vs. Frequency



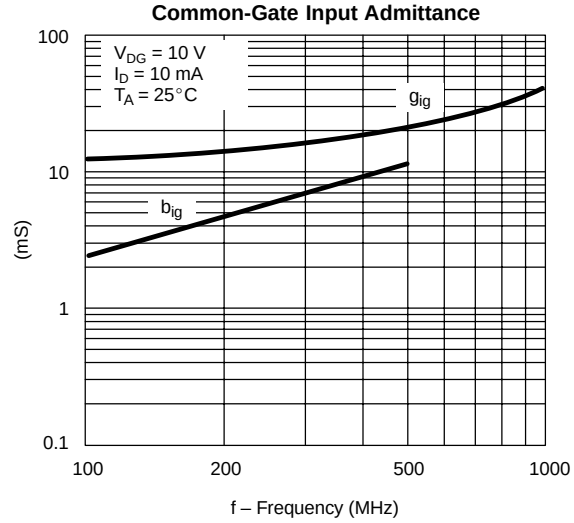
Forward Transconductance and Output Conductance vs. Gate-Source Cutoff Voltage



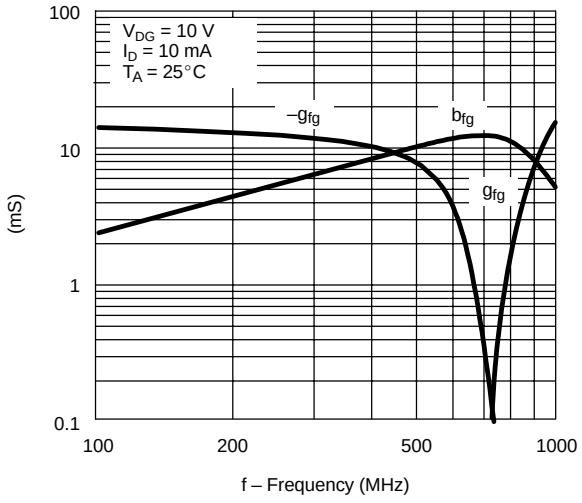
Gate Leakage Current



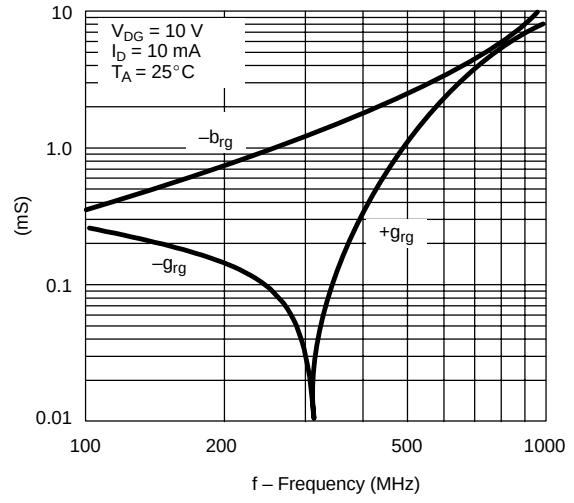
Common-Gate Input Admittance



Common-Gate Forward Admittance



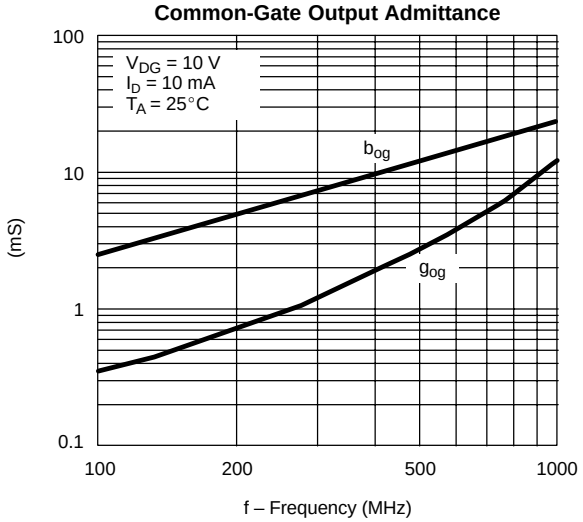
Common-Gate Reverse Admittance



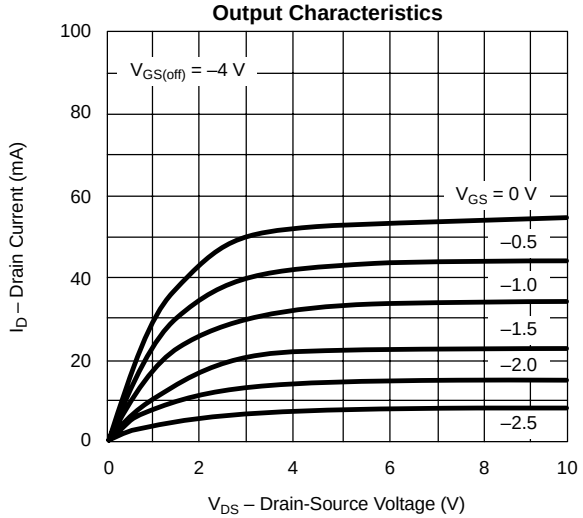
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S-04028—Rev. E, 04-Jun-01

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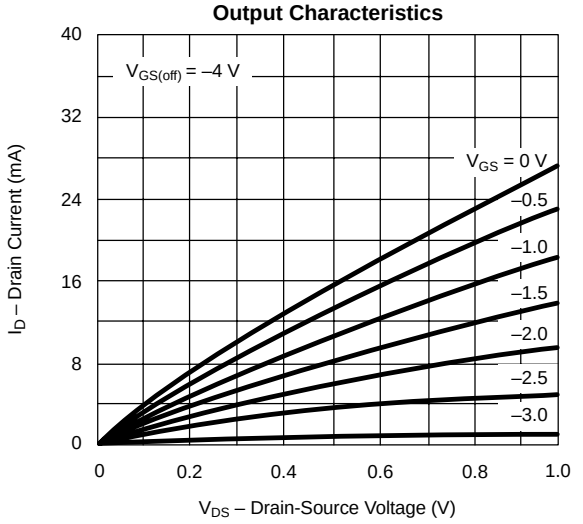
Common-Gate Output Admittance



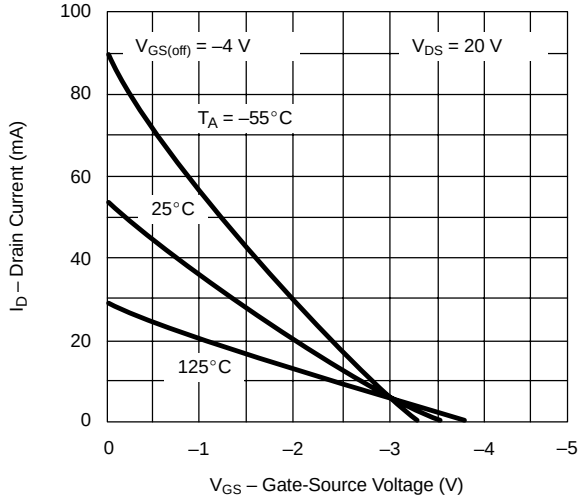
Output Characteristics



Output Characteristics

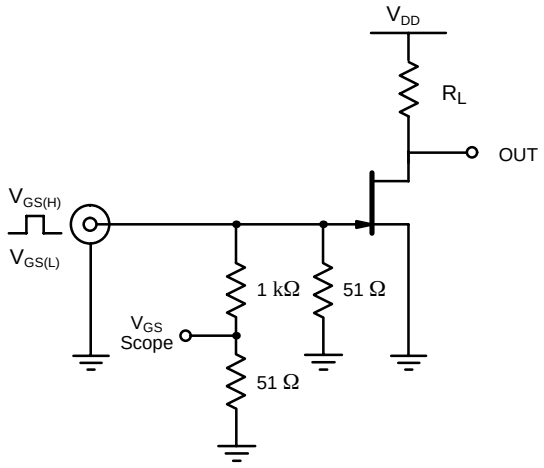


Transfer Characteristics



SWITCHING TIME TEST CIRCUIT			
	J/SST111	**J/SST112**	**J/SST113**
$V_{GS(L)}$	–12 V	–7 V	–5 V
R_L*	800 Ω	1600 Ω	3200 Ω
$I_{D(on)}$	12 mA	6 mA	3 mA

*Non-inductive



INPUT PULSE

Rise Time < 1 ns
Fall Time < 1 ns
Pulse Width 100 ns
PRF 1 MHz

SAMPLING SCOPE

Rise Time 0.4 ns
Input Resistance 10 MΩ
Input Capacitance 1.5 pF