# SN74LVC1G17 Single Schmitt-Trigger Buffer

## 1 Features

- Available in Ultra Small 0.64-mm$^2$ Package (DPW) With 0.5-mm Pitch
- Supports 5-V $V_{CC}$ Operation
- Inputs Accept Voltages to 5.5 V
- Max $t_{pd}$ of 4.6 ns at 3.3 V
- Low Power Consumption, 10-µA Max $I_{CC}$
- ±24-mA Output Drive at 3.3 V
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- MP3 Player/Recorder
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

## 3 Description

This single Schmitt-trigger buffer is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC1G17 device contains one buffer and performs the Boolean function Y = A.

The CMOS device has high output drive while maintaining low static power dissipation over a broad Vcc operating range.

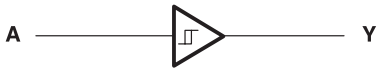
The SN74LVC1G17 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 mm × 0.8mm.

**Device Information(1)**

| DEVICE NAME | PACKAGE | BODY SIZE |
|---|---|---|
| SN74LVC1G17 | SOT-23 (5) | 2.9mm × 1.6mm |
| | SC70 (5) | 2.0mm × 1.25mm |
| | X2SON (4) | 0.8mm × 0.8mm |
| | SON (6) | 1.45mm × 1.0mm |
| | SON (6) | 1.0mm × 1.0mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Simplified Schematic




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 5 Revision History

**Changes from Revision U (February 2014) to Revision V** — **Page**

- Added Pin Functions table. ... 3
- Added Handling Ratings table. ... 4
- Added Thermal Information table. ... 5
- Added Typical Characteristics. ... 7
- Added Detailed Description section. ... 10
- Added Application and Implementation section. ... 11
- Added Power Supply Recommendations section. ... 12
- Added Layout section. ... 12

**Changes from Revision T (November 2012) to Revision U** — **Page**

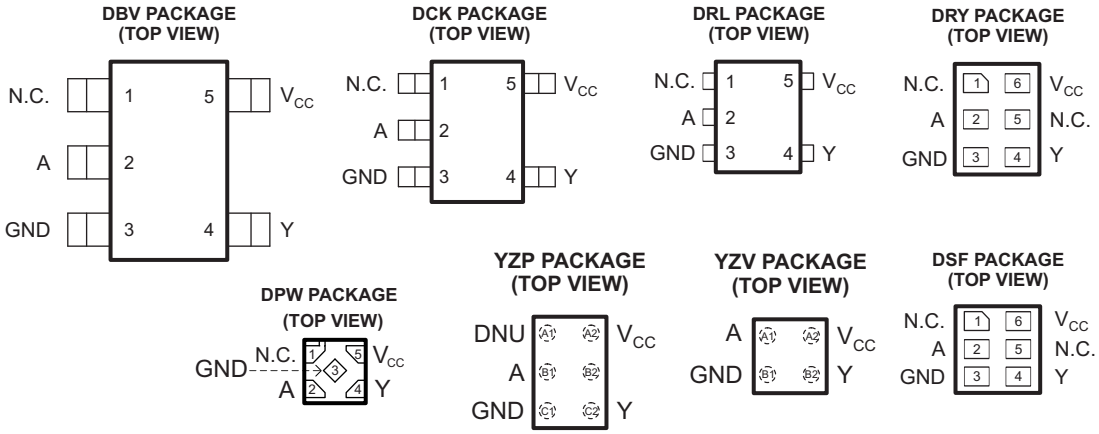
- Added Applications. ... 1
- Moved $T_{stg}$ to Handling Ratings table. ... 4
- Changed MAX operating free-air temperature from 85°C to 125°C. ... 5
- Added –40°C to 125°C to Electrical Characteristics table. ... 6
- Added Switching Characteristics table for –40°C to 125°C temperature range. ... 7

**Changes from Revision S (June 2011) to Revision T** — **Page**

- Removed Ordering Information table. ... 3


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# 6 Pin Configuration and Functions




N.C. – No internal connection
See mechanical drawings for dimensions.
DNU – Do not use

## Pin Functions

| PIN | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DBV, DCK, DRL, DPW | DRY, DSF | YZP | YZV | |
| NC | 1 | 1, 5 | A1, B2 | – | Not connected |
| A | 2 | 2 | B1 | A1 | Input |
| GND | 3 | 3 | C1 | B1 | Ground |
| Y | 4 | 4 | C2 | B2 | Output |
| $V_{CC}$ | 5 | 6 | A2 | A2 | Power terminal |

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# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions tables is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.

## 7.2 Handling Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | –65 | 150 | °C |
| $V_{ESD}$ (1) | Human-Body Model (HBM)(2) | 0 | 2 | kV |
| | Charged-Device Model (CDM)(3) | 0 | 1 | kV |

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 7.3 Recommended Operating Conditions(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 3 V | | –16 | |
| | | | | –24 | |
| | | $V_{CC}$ = 4.5 V | | –32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 7.4 Thermal Information

| THERMAL METRIC(1) | | SN74LVC1G17 | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | DBV | DCK | DRL | DRY | YZP | DPW | YZV | |
| | | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 5 PINS | 4 PINS | 4 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 229 | 280 | 350 | 608 | 130 | 340 | 181 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 164 | 66 | 121 | 432 | 54 | 215 | 1 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 62 | 67 | 171 | 446 | 51 | 294 | 39 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 44 | 2 | 11 | 191 | 1 | 41 | 8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 62 | 66 | 169 | 442 | 50 | 294 | 38 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | – | – | 198 | – | 250 | – | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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## 7.5 Electrical Characteristics—DC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | 25°C | | | –40°C TO 85°C | | | –40°C TO 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP(1) | MAX | MIN | TYP(1) | MAX | MIN | TYP | MAX | |
| $V_{T+}$ (Positive-going input threshold voltage) | | | 1.65 V | | | | 0.76 | | 1.13 | 0.76 | | 1.13 | V |
| | | | 2.3 V | | | | 1.08 | | 1.56 | 1.08 | | 1.56 | |
| | | | 3 V | | | | 1.48 | | 1.92 | 1.48 | | 1.92 | |
| | | | 4.5 V | | | | 2.19 | | 2.74 | 2.19 | | 2.74 | |
| | | | 5.5 V | | | | 2.65 | | 3.33 | 2.65 | | 3.33 | |
| $V_{T-}$ (Negative-going input threshold voltage) | | | 1.65 V | | | | 0.35 | | 0.59 | 0.35 | | 0.59 | V |
| | | | 2.3 V | | | | 0.56 | | 0.88 | 0.56 | | 0.88 | |
| | | | 3 V | | | | 0.89 | | 1.2 | 0.89 | | 1.2 | |
| | | | 4.5 V | | | | 1.51 | | 1.97 | 1.51 | | 1.97 | |
| | | | 5.5 V | | | | 1.88 | | 2.4 | 1.88 | | 2.4 | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | | 1.65 V | | | | 0.36 | | 0.64 | 0.36 | | 0.64 | V |
| | | | 2.3 V | | | | 0.45 | | 0.78 | 0.45 | | 0.78 | |
| | | | 3 V | | | | 0.51 | | 0.83 | 0.51 | | 0.83 | |
| | | | 4.5 V | | | | 0.58 | | 0.93 | 0.58 | | 0.93 | |
| | | | 5.5 V | | | | 0.69 | | 1.04 | 0.69 | | 1.04 | |
| $V_{OH}$ | $I_{OH}$ = –100 µA | | 1.65 V to 5.5 V | | | | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | | V |
| | $I_{OH}$ = –4 mA | | 1.65 V | | | | 1.2 | | | 1.2 | | | |
| | $I_{OH}$ = –8 mA | | 2.3 V | | | | 1.9 | | | 1.9 | | | |
| | $I_{OH}$ = –16 mA | | 3 V | | | | 2.4 | | | 2.4 | | | |
| | $I_{OH}$ = –24 mA | | | | | | 2.3 | | | 2.3 | | | |
| | $I_{OH}$ = –32 mA | | 4.5 V | | | | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | | 1.65 V to 5.5 V | | | | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 4 mA | | 1.65 V | | | | | | 0.45 | | | 0.45 | |
| | $I_{OL}$ = 8 mA | | 2.3 V | | | | | | 0.3 | | | 0.3 | |
| | $I_{OL}$ = 16 mA | | 3 V | | | | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 24 mA | | | | | | | | 0.55 | | | 0.55 | |
| | $I_{OL}$ = 32 mA | | 4.5 V | | | | | | 0.55 | | | 0.55 | |
| $I_I$ | A input | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | | | | ±5 | | | ±5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 5.5 V | 0 | | | | | | ±10 | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = 5.5 V or GND, $I_O$ = 0 | 1.65 V to 5.5 V | | | | | | 10 | | | 10 | µA |
| | | $V_I$ = 3.6 V or GND, $I_O$ = 0 | 3 V to 3.6 V | | 0.5 | 1.5 | | | | | | | |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 3 V to 5.5 V | | | | | | 500 | | | 500 | µA |
| $C_I$ | | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 4.5 | | | | | | | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.


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## 7.6 Switching Characteristics, $C_L$ = 15 pF

over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 3 )

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C TO 85°C | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 2.8 | 9.9 | 1.6 | 5.5 | 1.5 | 4.6 | 0.9 | 4.4 | ns |

## 7.7 Switching Characteristics AC Limit, –40°C TO 85°C

over recommended operating free-air temperature range, $C_L$ = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C TO 85°C | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 3.8 | 11 | 2 | 6.5 | 1.8 | 5.5 | 1.2 | 5 | ns |

## 7.8 Switching Characteristics AC Limit, –40°C TO 125°C

over recommended operating free-air temperature range, $C_L$ = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C TO 125°C | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 3.8 | 13 | 2 | 8 | 1.8 | 6.5 | 1.2 | 6 | ns |

## 7.9 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 20 | 21 | 22 | 26 | pF |

## 7.10 Typical Characteristics

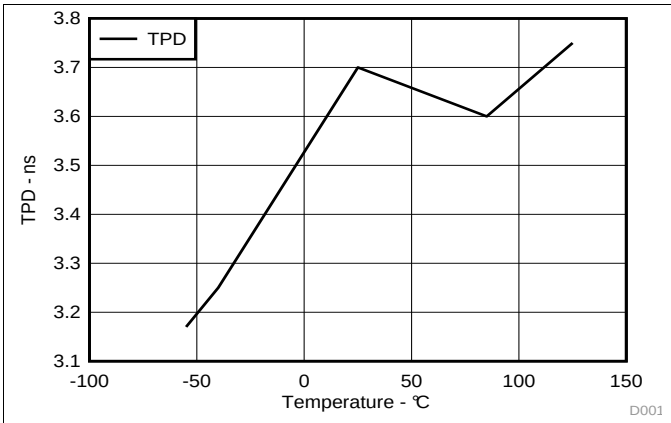



**Figure 1. Across Temperature at 3.3V Vcc**

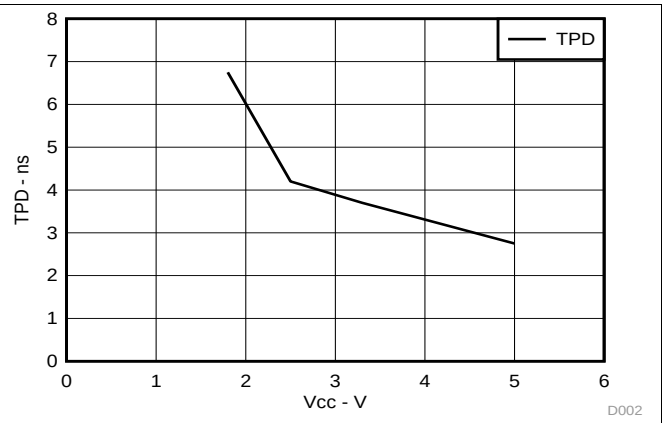
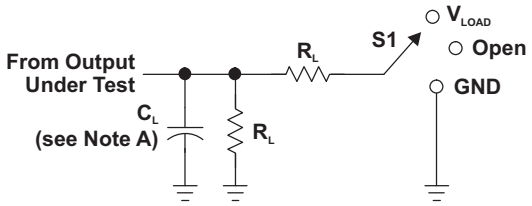



**Figure 2. Across Vcc at 25°C**

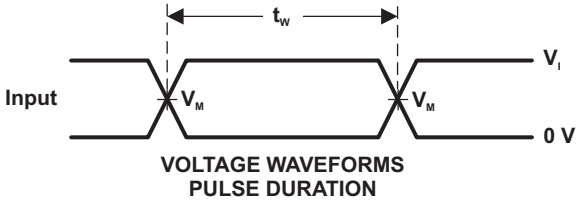
# 8 Parameter Measurement Information



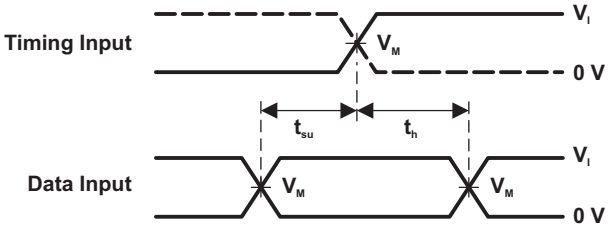

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

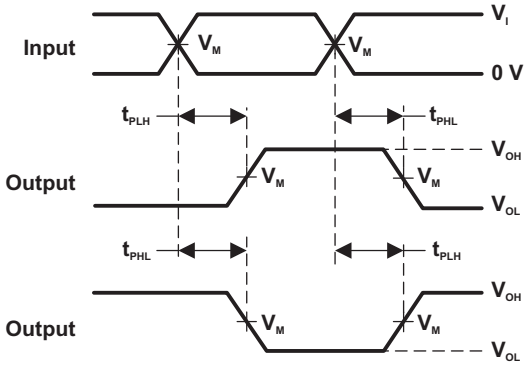
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 15 pF | 1 MΩ | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 15 pF | 1 MΩ | 0.3 V |



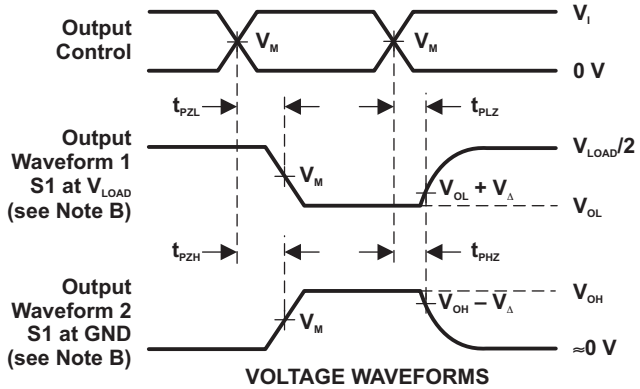

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



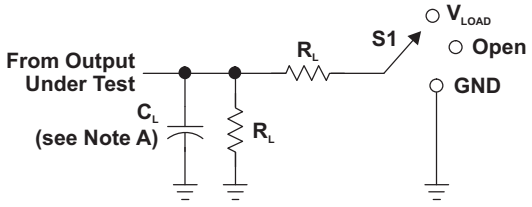

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**


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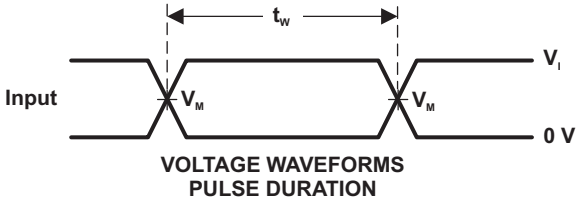
## Parameter Measurement Information (continued)



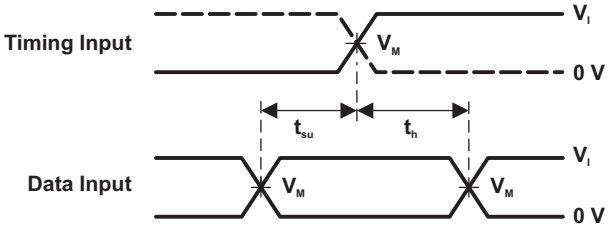

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

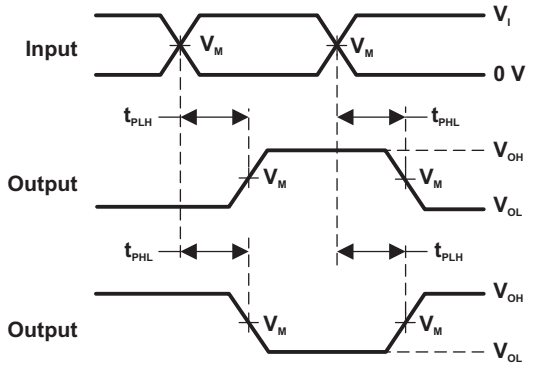
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



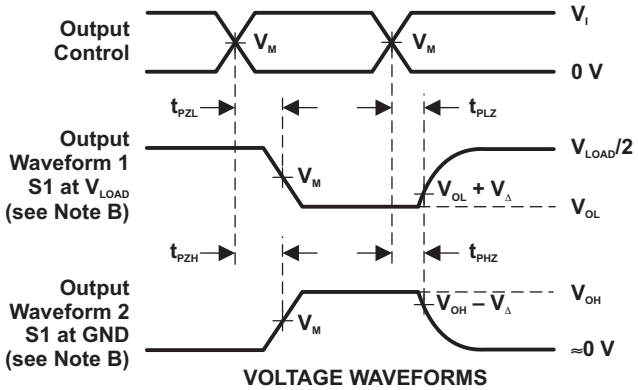

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit and Voltage Waveforms**

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# 9 Detailed Description

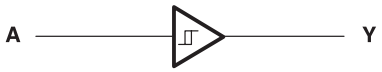
## 9.1 Overview

The SN74LVC1G17 device contains one Schmitt trigger buffer and performs the Boolean function Y = A. The device functions as an independent buffer, but because of Schmitt action, it will have different input threshold levels for a positive-going (VT+) and negative-going signals.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 9.2 Functional Block Diagram




## 9.3 Feature Description

- Wide operating voltage range.
  - Operates From 1.65 V to 5.5 V.
- Allows Down voltage translation.
- Inputs accept voltages to 5.5 V.
- $I_{off}$ feature allows voltages on the inputs and outputs, when $V_{CC}$ is 0 V.

## 9.4 Device Functional Modes

**Table 1. Function Table**

| INPUT A | OUTPUT Y |
|---|---|
| H | H |
| L | L |

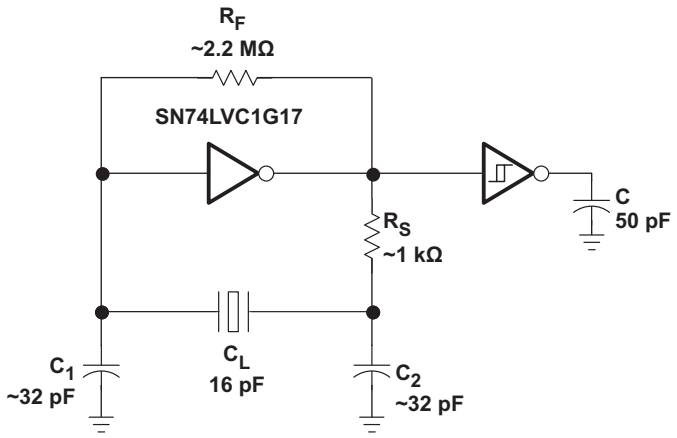

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# 10 Applications and Implementation

## 10.1 Application Information

The SN74LVC1G14 is a high drive CMOS device that can be used for a multitude of buffer type functions where the input is slow or noisy. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to $V_{CC}$.

## 10.2 Typical Application




### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See (Δt/ΔV) in the Recommended Operating Conditions table.
   - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in the Recommended Operating Conditions table.
   - Inputs are overvoltage tolerant allowing them to go as high as ($V_I$ max) in the Recommended Operating Conditions table at any valid $V_{CC}$ .
2. Recommend Output Conditions
   - Load currents should not exceed ($I_O$ max) per output and should not exceed (continuous current through $V_{CC}$ or GND) total current for the part. These limits are located in the Absolute Max Ratings table.
   - Outputs should not be pulled above $V_{CC}$.

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## Typical Application (continued)

### 10.2.3 Application Curves

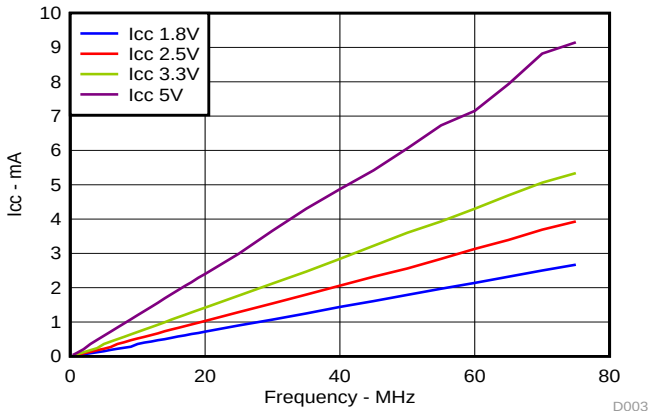



**Figure 5. ICC vs Frequency**

## 11 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

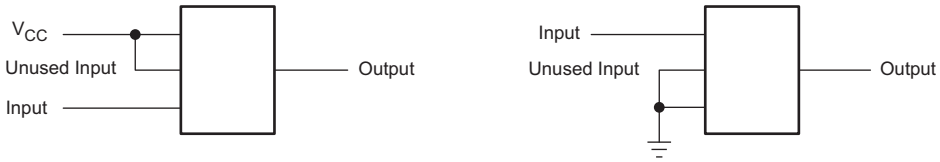
Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1-μF capacitor is recommended and if there are multiple Vcc pins then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input terminals should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or Vcc whichever make more sense or is more convenient.

### 12.2 Layout Example





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# 13 Device and Documentation Support

## 13.1 Trademarks

All trademarks are the property of their respective owners.

## 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

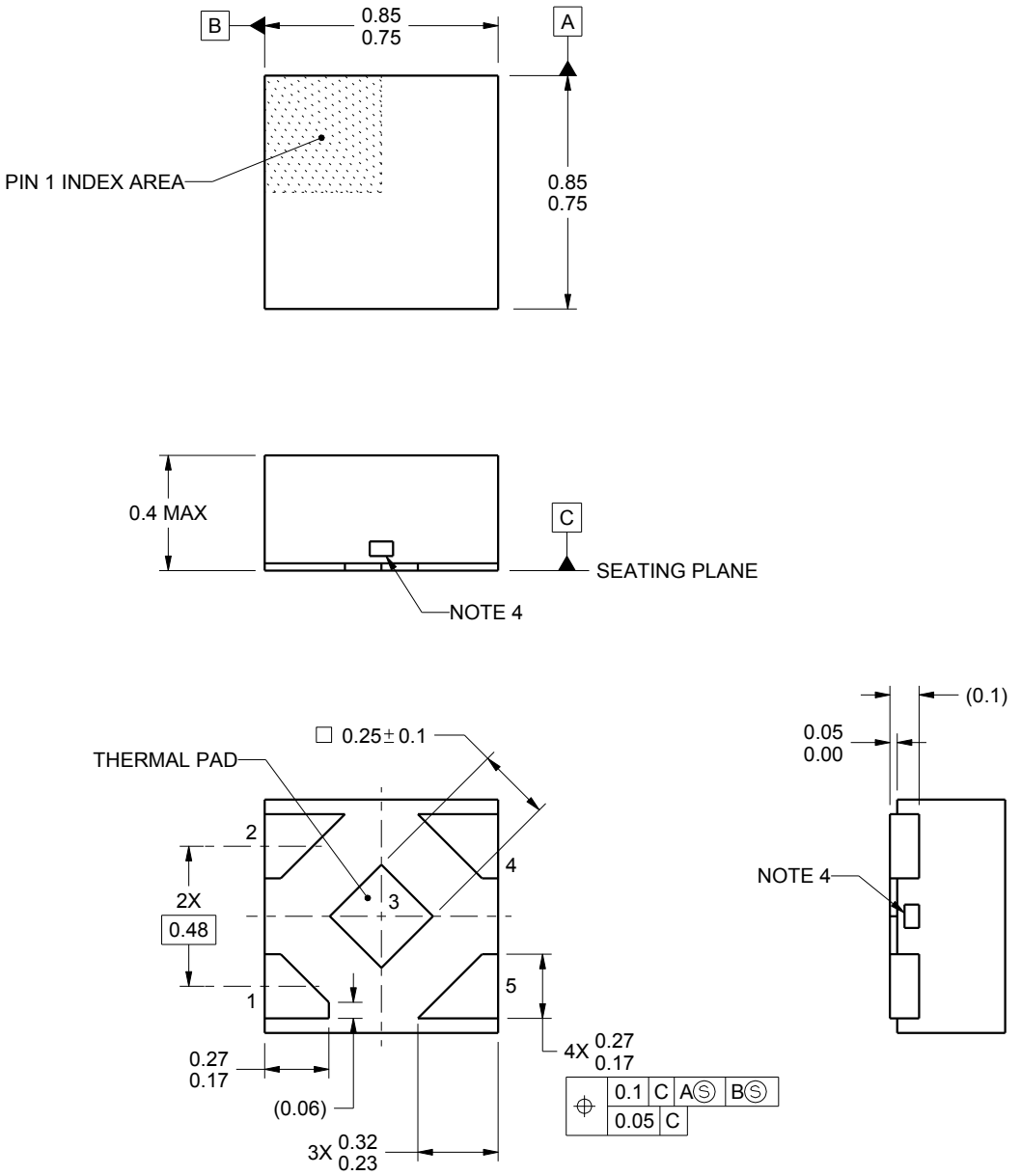
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# PACKAGE OUTLINE

## DPW0005A-C01

## X2SON - 0.4 mm max height

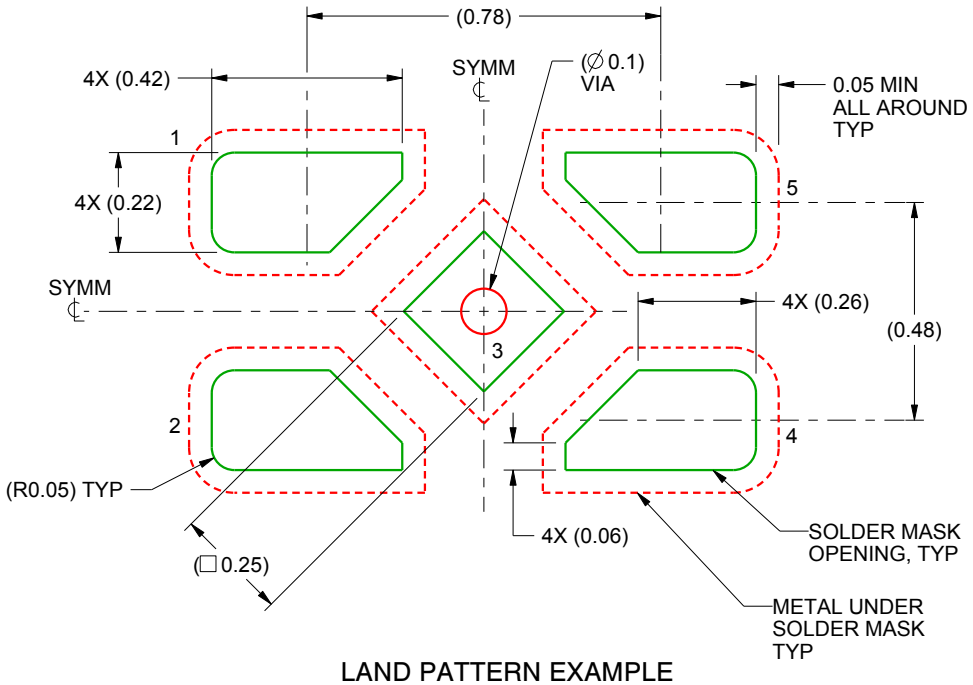
PLASTIC SMALL OUTLINE - NO LEAD




4221849/A 12/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.

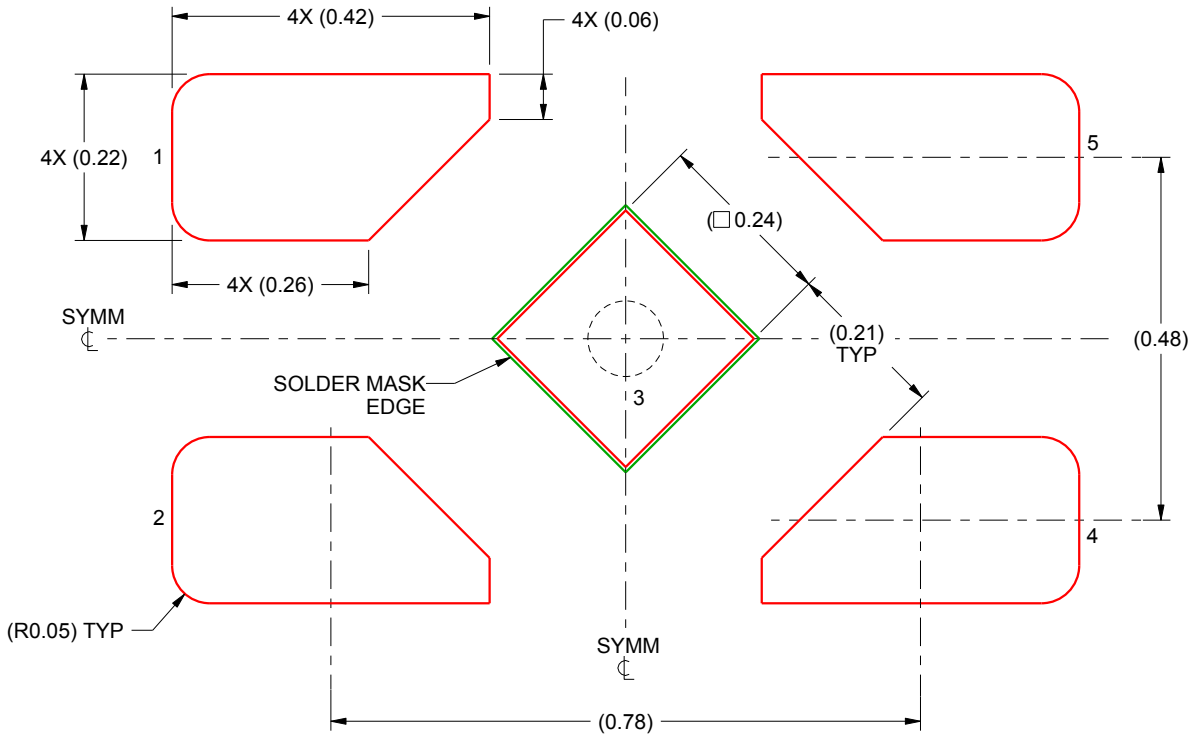



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4221849/A 12/2014

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4221849/A 12/2014

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G17DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C175 ~ C17F ~ C17K ~ C17R) (C17H ~ C17P ~ C17S) | Samples |
| SN74LVC1G17DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C17F | Samples |
| SN74LVC1G17DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C17F | Samples |
| SN74LVC1G17DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C175 ~ C17F ~ C17K ~ C17R) (C17H ~ C17P ~ C17S) | Samples |
| SN74LVC1G17DBVTE4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C17F | Samples |
| SN74LVC1G17DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C17F | Samples |
| SN74LVC1G17DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C75 ~ C7F ~ C7K ~ C7R ~ C7T) (C7H ~ C7P ~ C7S) | Samples |
| SN74LVC1G17DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C75 ~ C7F ~ C7K ~ C7R ~ C7T) (C7H ~ C7P ~ C7S) | Samples |
| SN74LVC1G17DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C75 ~ C7F ~ C7K ~ C7R ~ C7T) (C7H ~ C7P ~ C7S) | Samples |
| SN74LVC1G17DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C75 ~ C7F ~ C7K ~ C7R ~ C7T) (C7H ~ C7P ~ C7S) | Samples |
| SN74LVC1G17DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C75 ~ C7F ~ C7K ~ C7R ~ C7T) (C7H ~ C7P ~ C7S) | Samples |
| SN74LVC1G17DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C75 ~ C7F ~ C7K ~ C7R ~ C7T) (C7H ~ C7P ~ C7S) | Samples |
| SN74LVC1G17DPWR | ACTIVE | X2SON | DPW | 4 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | S4 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G17DRLR | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C77 ~ C7R) | Samples |
| SN74LVC1G17DRLRG4 | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C77 ~ C7R) | Samples |
| SN74LVC1G17DRY2 | PREVIEW | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7 | |
| SN74LVC1G17DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7 | Samples |
| SN74LVC1G17DSF2 | PREVIEW | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C7 | |
| SN74LVC1G17DSFR | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C7 | Samples |
| SN74LVC1G17YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (C77 ~ C7N) | Samples |
| SN74LVC1G17YZVR | ACTIVE | DSBGA | YZV | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C7 (7 ~ N) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC1G17 :**

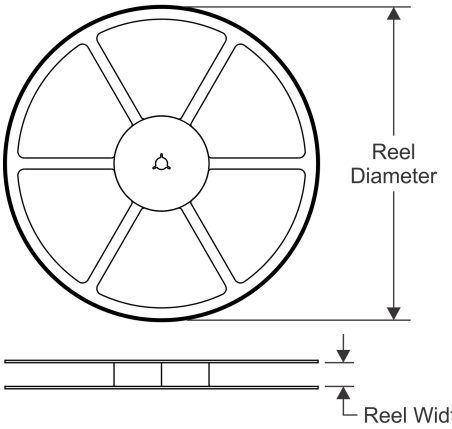
- Automotive: SN74LVC1G17-Q1
- Enhanced Product: SN74LVC1G17-EP

NOTE: Qualified Version Definitions:

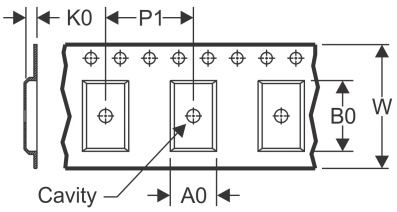
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

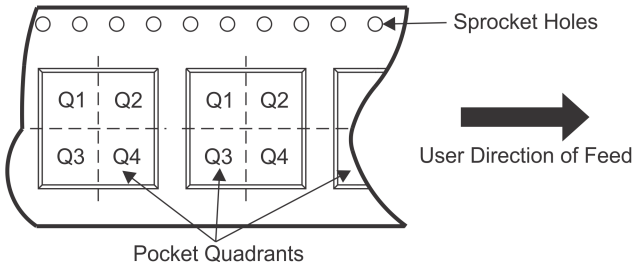



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

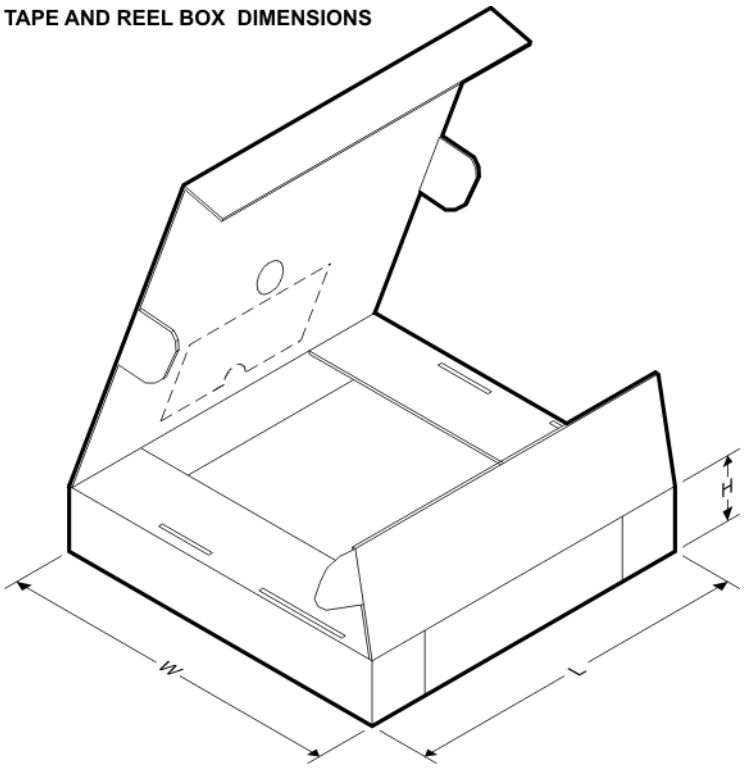
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G17DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.2 | 3.17 | 3.23 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DCKT | SC70 | DCK | 5 | 250 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DRLR | SOT | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G17DRYR | SON | DRY | 6 | 5000 | 179.0 | 8.4 | 1.2 | 1.65 | 0.7 | 4.0 | 8.0 | Q1 |
| SN74LVC1G17DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G17YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |
| SN74LVC1G17YZVR | DSBGA | YZV | 4 | 3000 | 178.0 | 9.2 | 1.0 | 1.0 | 0.63 | 4.0 | 8.0 | Q1 |

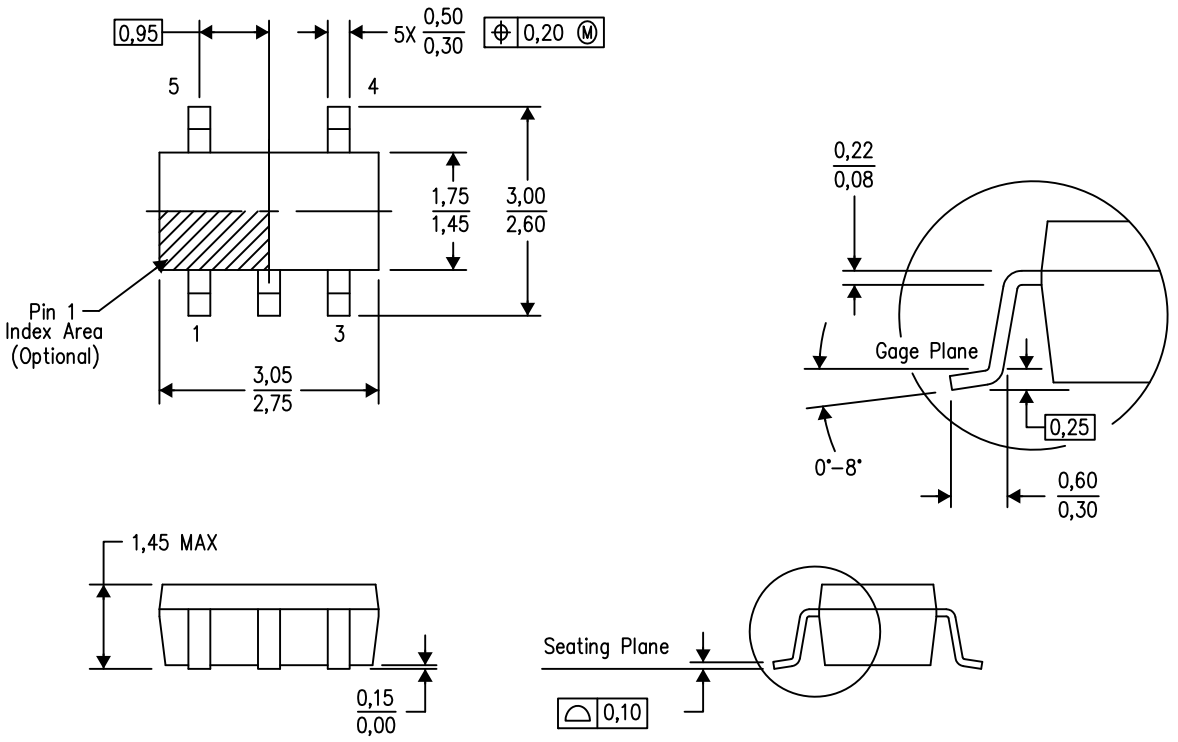
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1G17DBVR | SOT-23 | DBV | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G17DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G17DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G17DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G17DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G17DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G17DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G17DCKT | SC70 | DCK | 5 | 250 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G17DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G17DRLR | SOT | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G17DRYR | SON | DRY | 6 | 5000 | 203.0 | 203.0 | 35.0 |
| SN74LVC1G17DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G17YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74LVC1G17YZVR | DSBGA | YZV | 4 | 3000 | 220.0 | 220.0 | 35.0 |

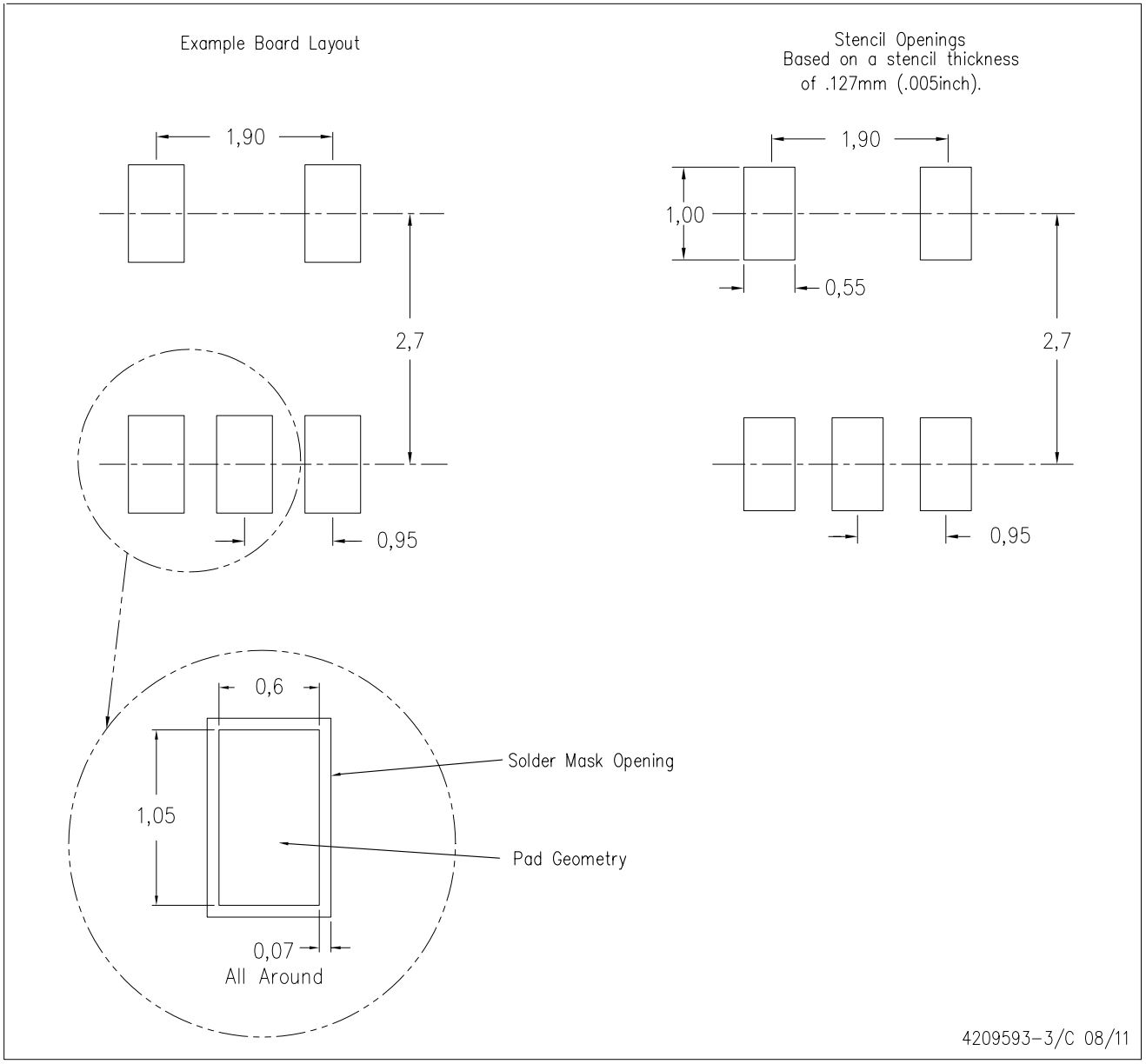
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/N 12/14

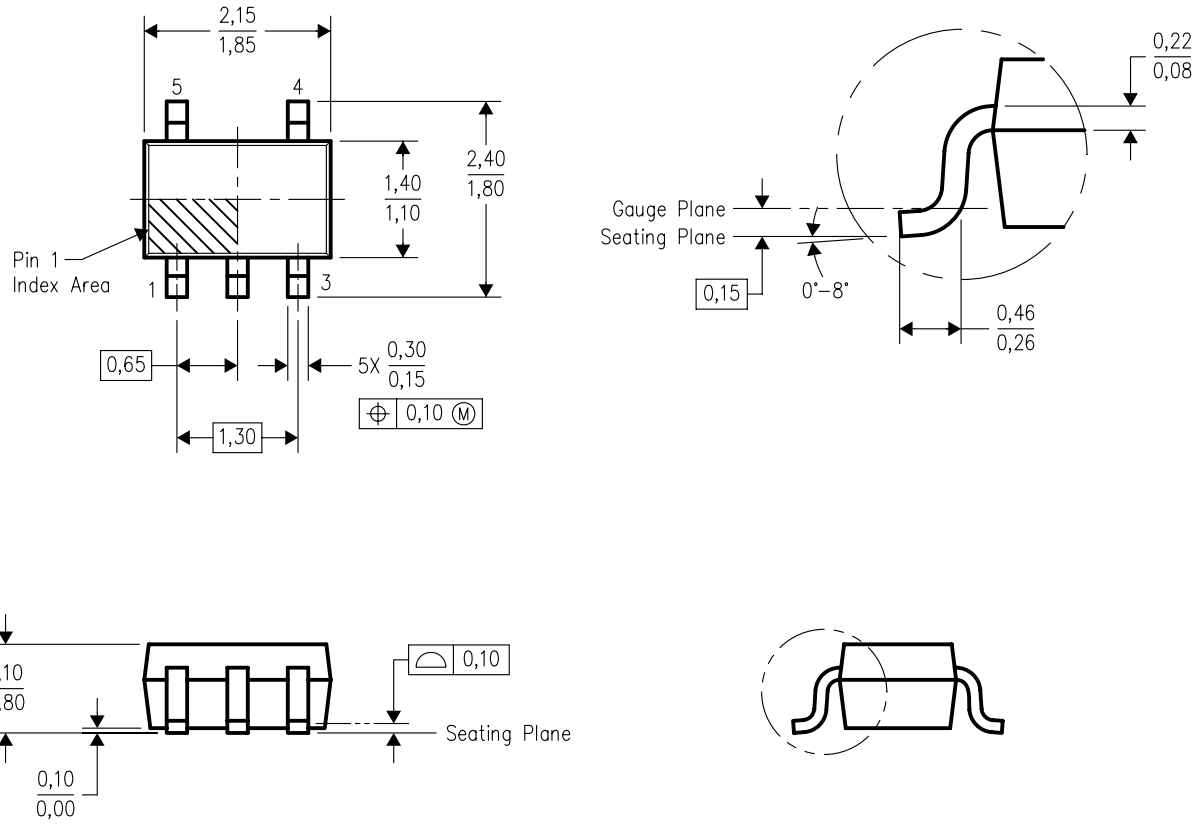
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

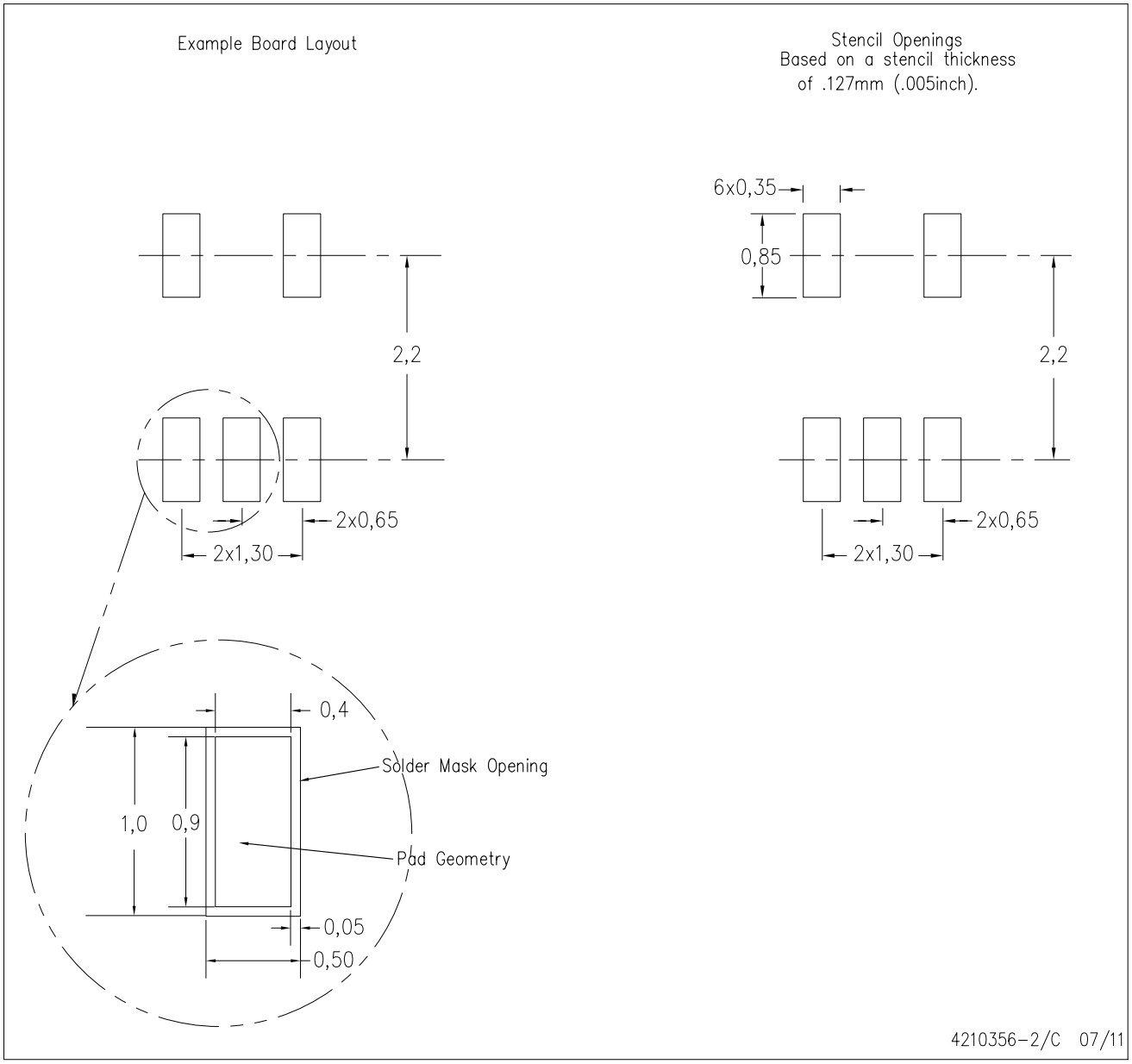
## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



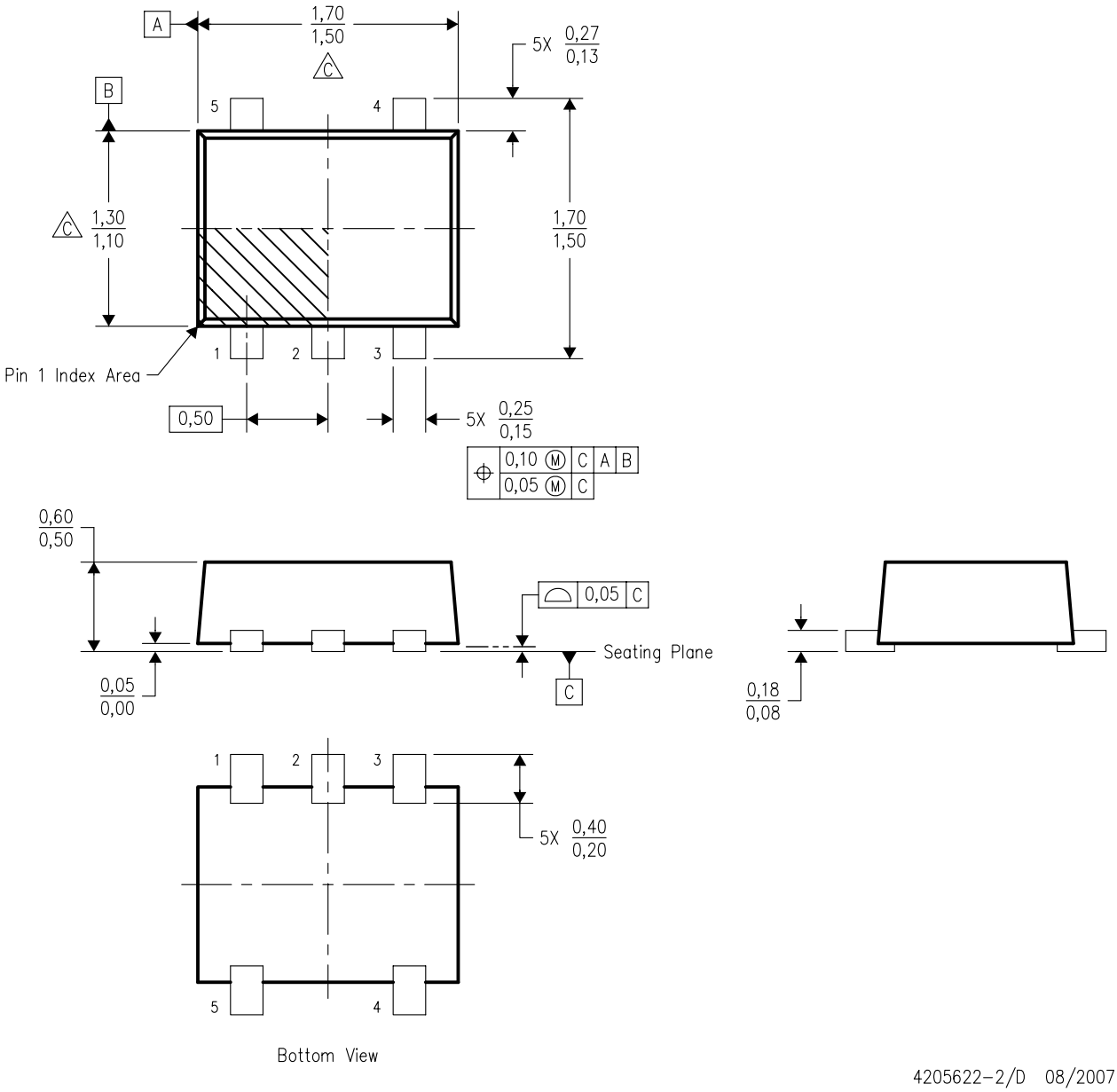

4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



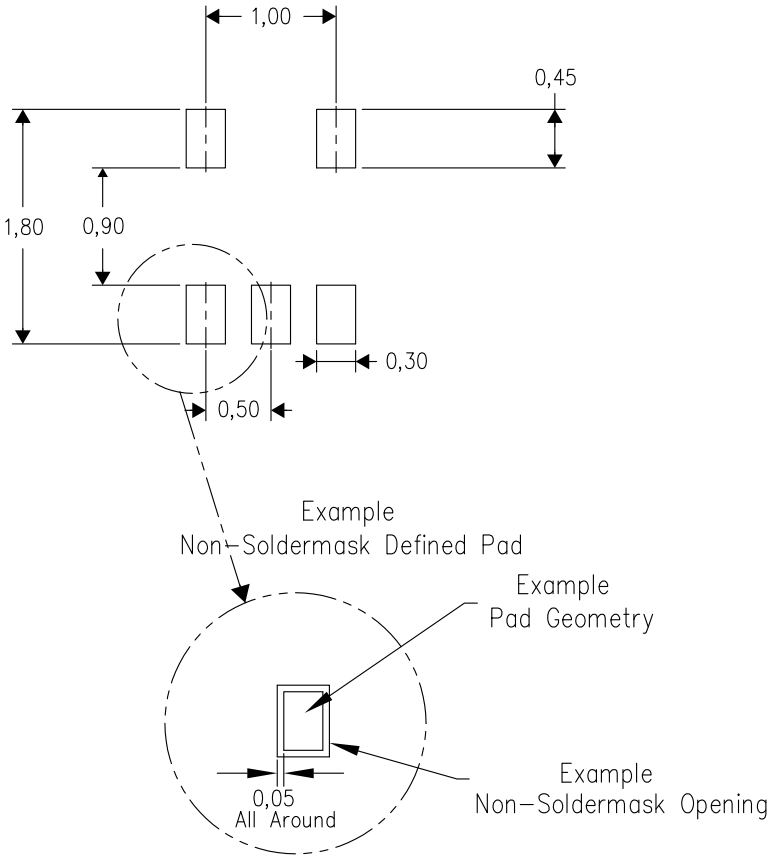

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



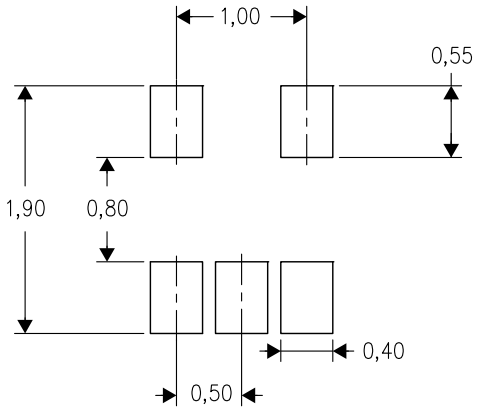

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



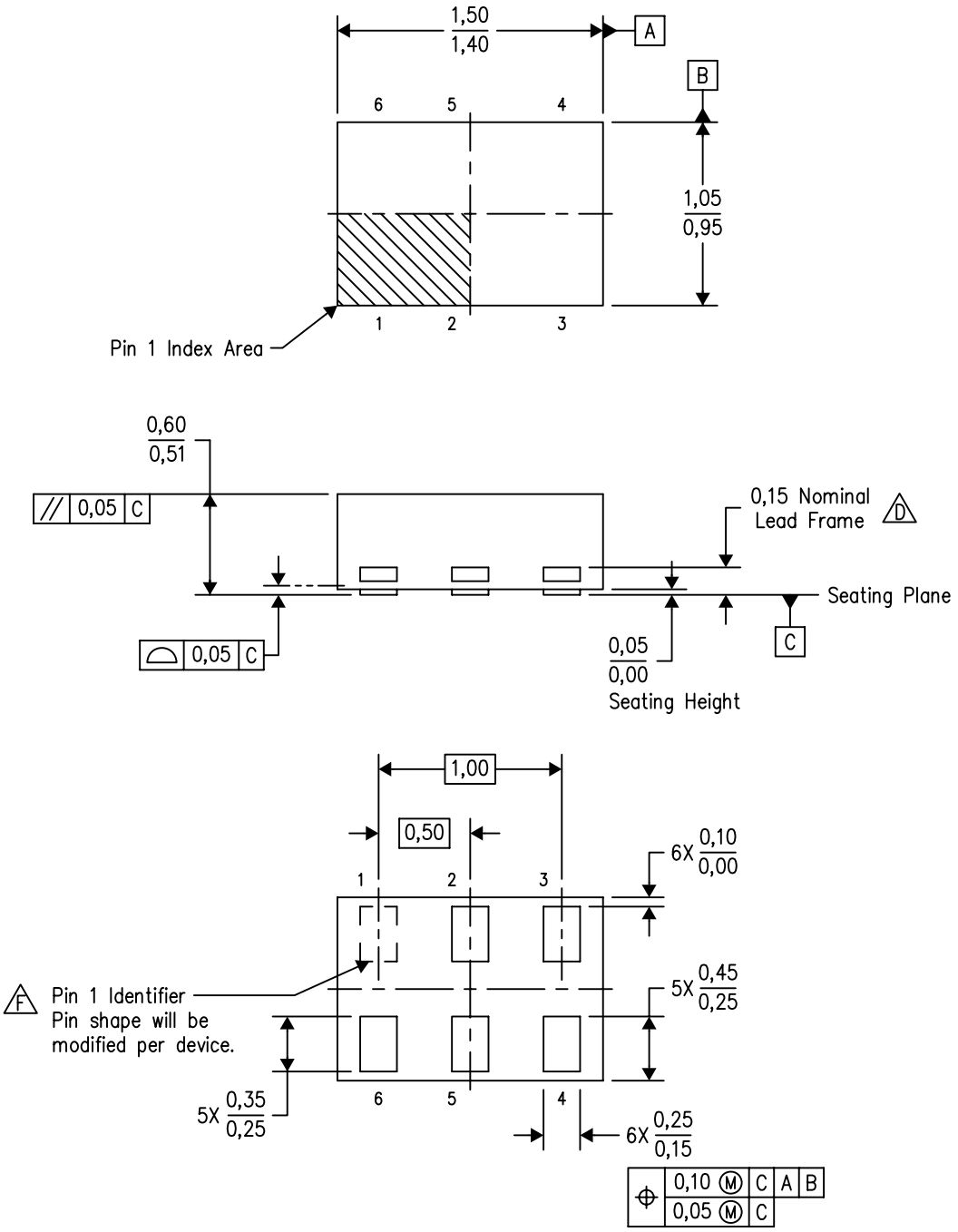

Example Stencil Design
(Note E)




4208207–2/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

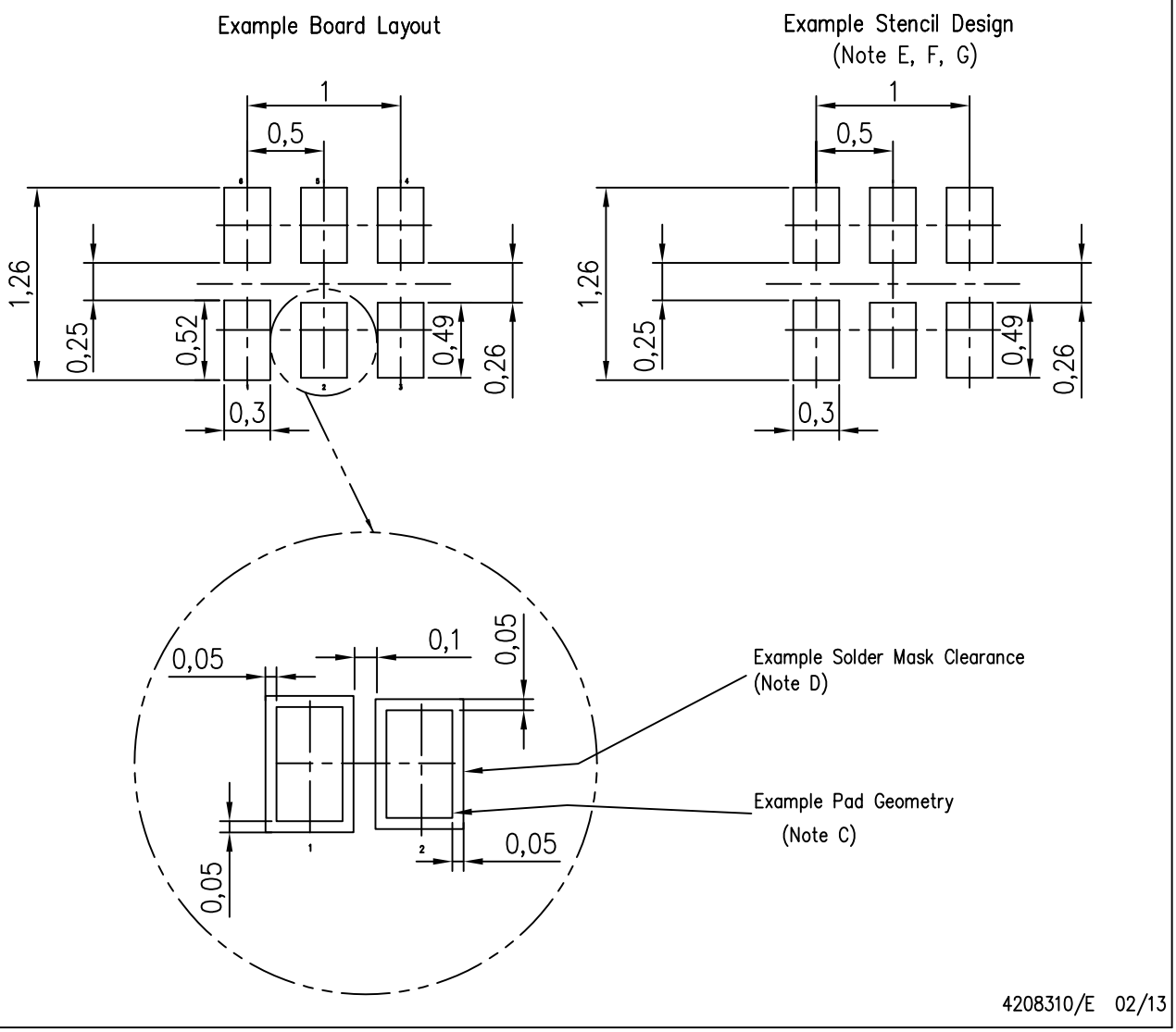
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4207181/F 12/11

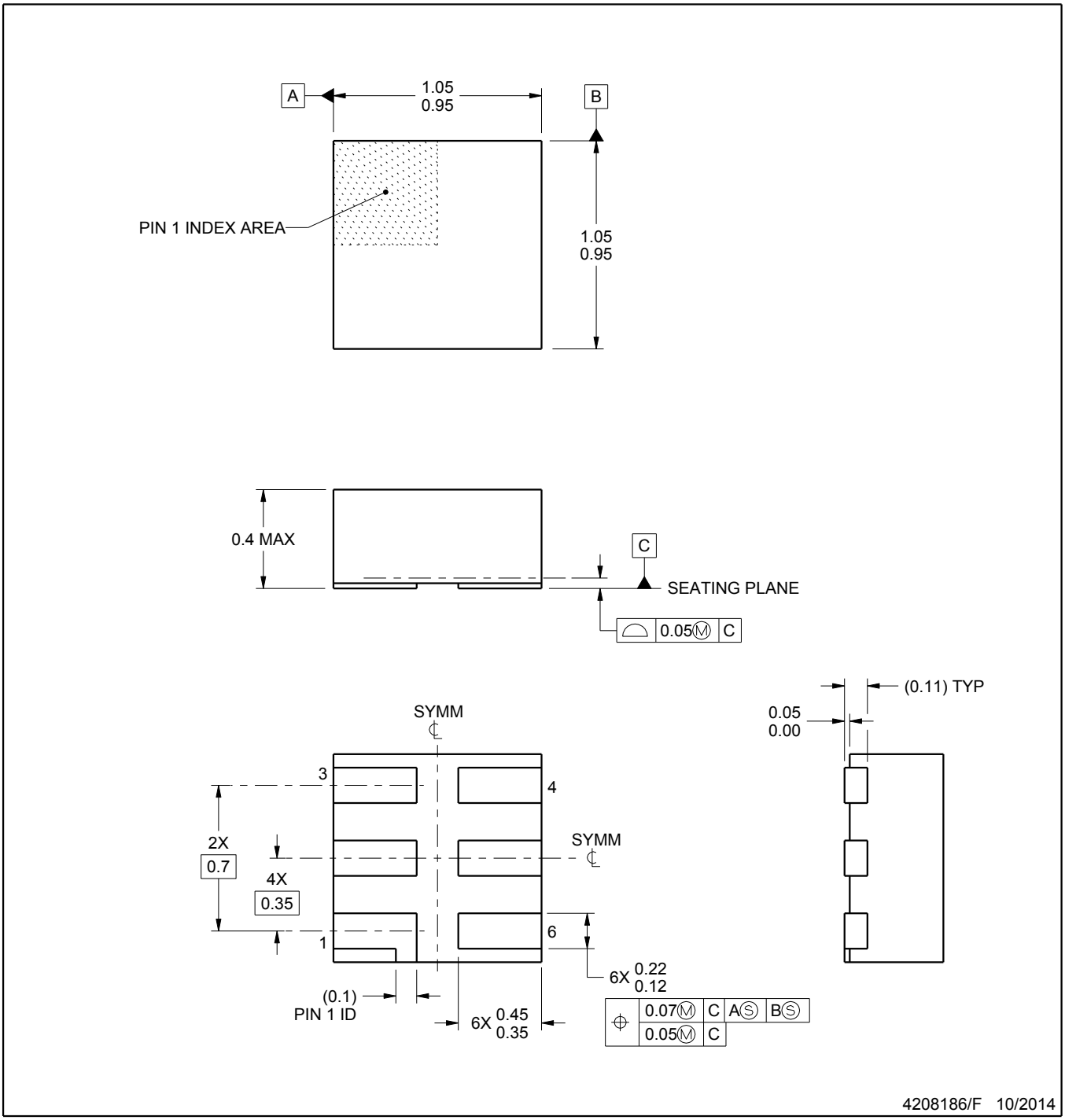
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

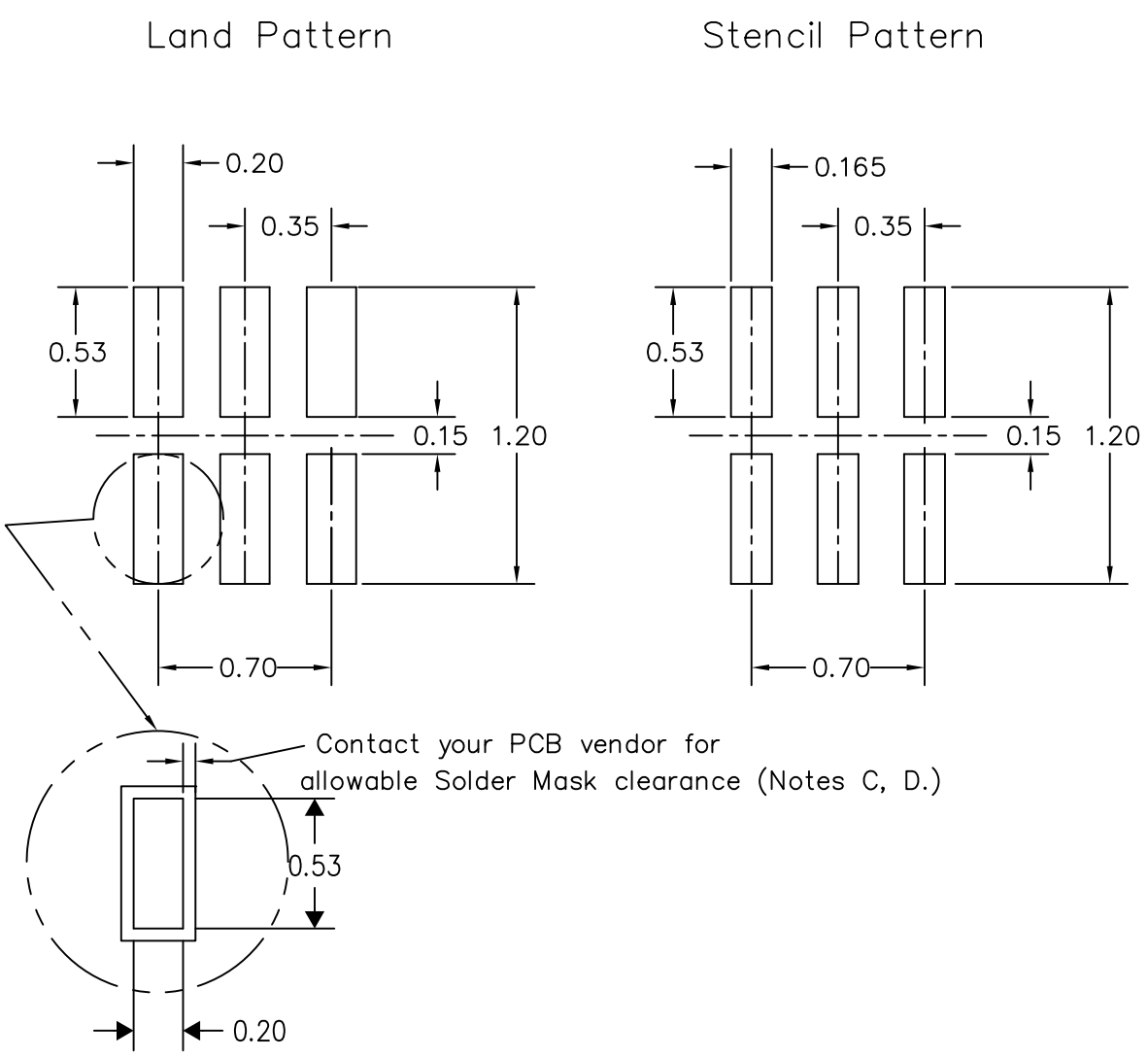
DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

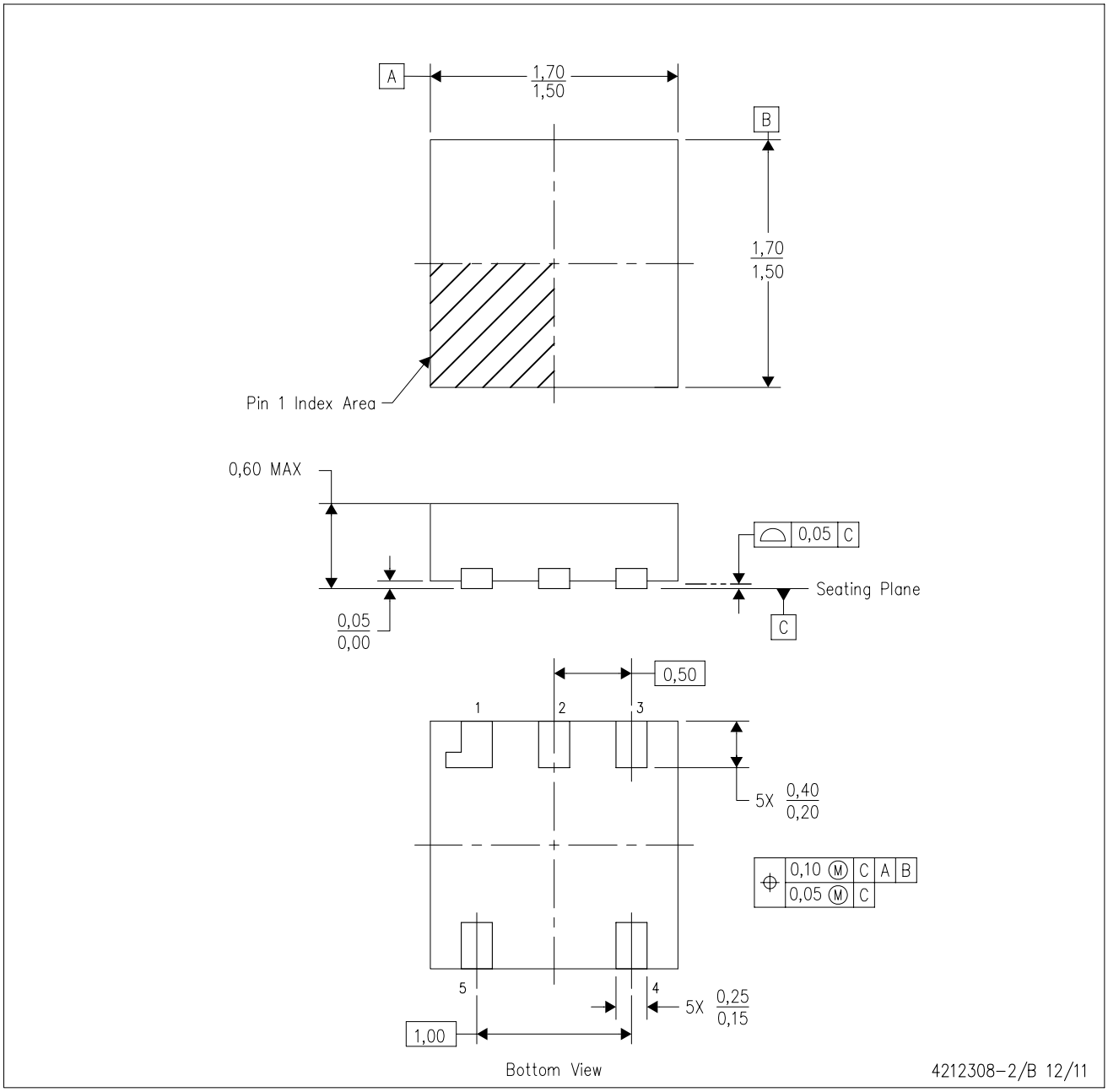
DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4210277/D 05/12

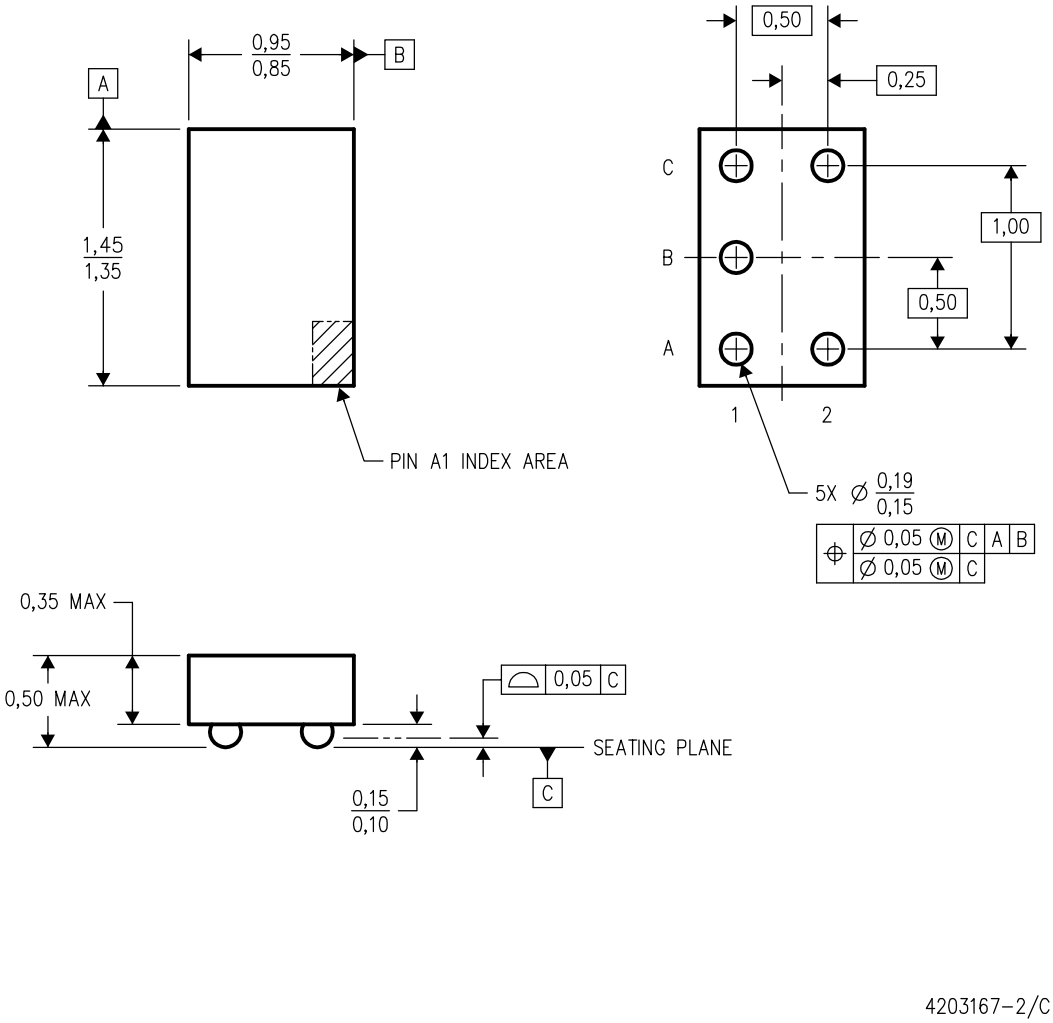
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
H. Component placement force should be minimized to prevent excessive paste block deformation.

DPK (S–PUSON–N5) PLASTIC SMALL OUTLINE NO–LEAD




NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.

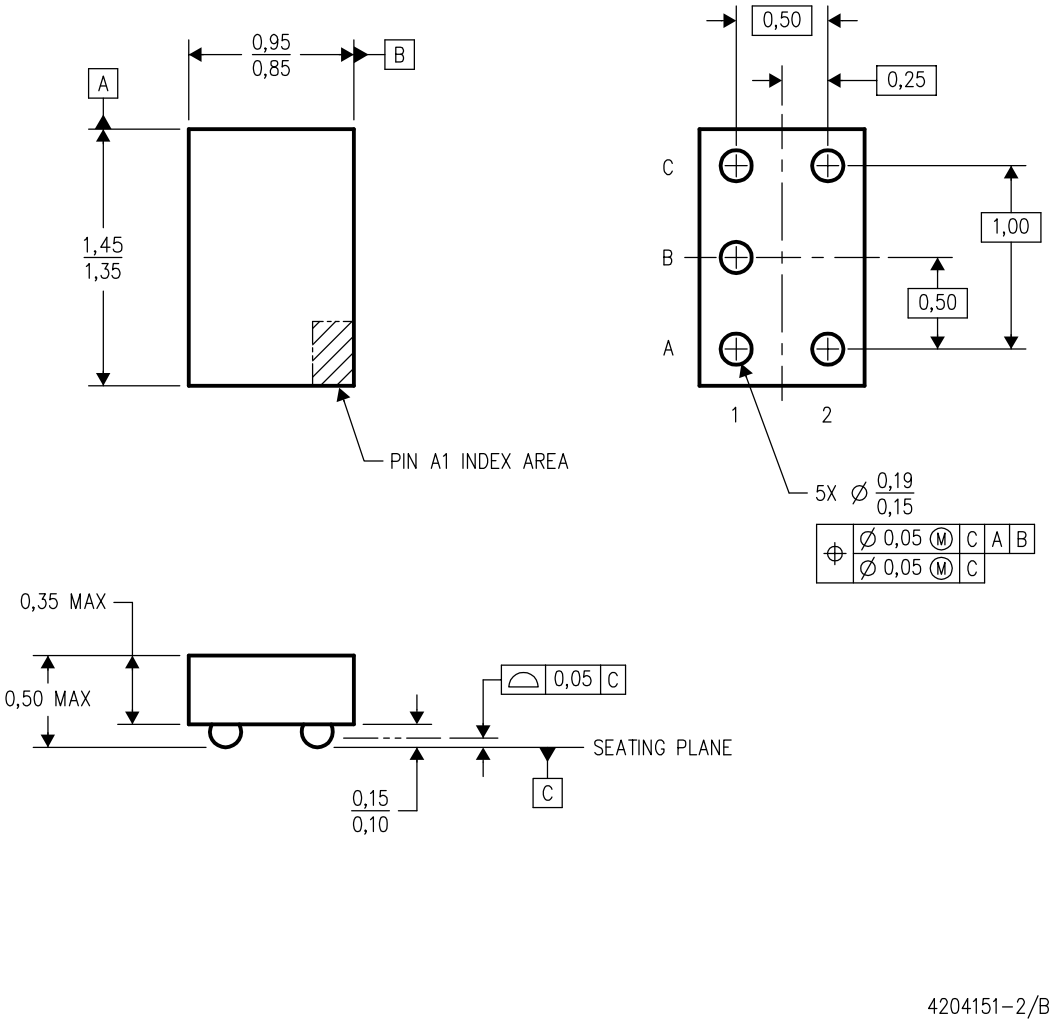
## YEA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. Package complies to JEDEC MO–211 variation EA.
E. This package is tin–lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead–free.

**NanoStar is a trademark of Texas Instruments.**

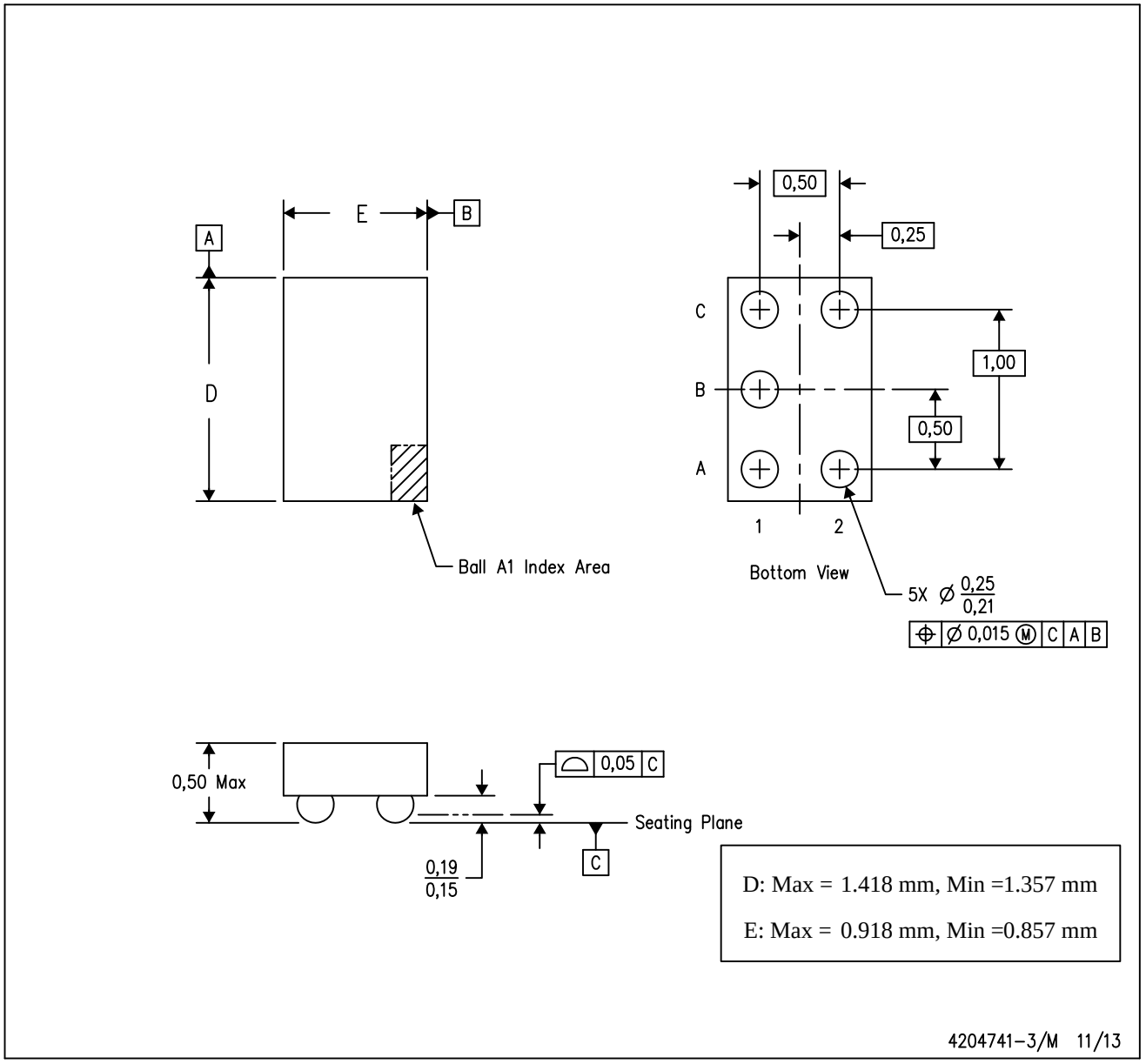
## YZA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Package complies to JEDEC MO–211 variation EA.
E. This package is lead–free. Refer to the 5 YEA package (drawing 4203167) for tin–lead (SnPb).

**NanoFree is a trademark of Texas Instruments.**

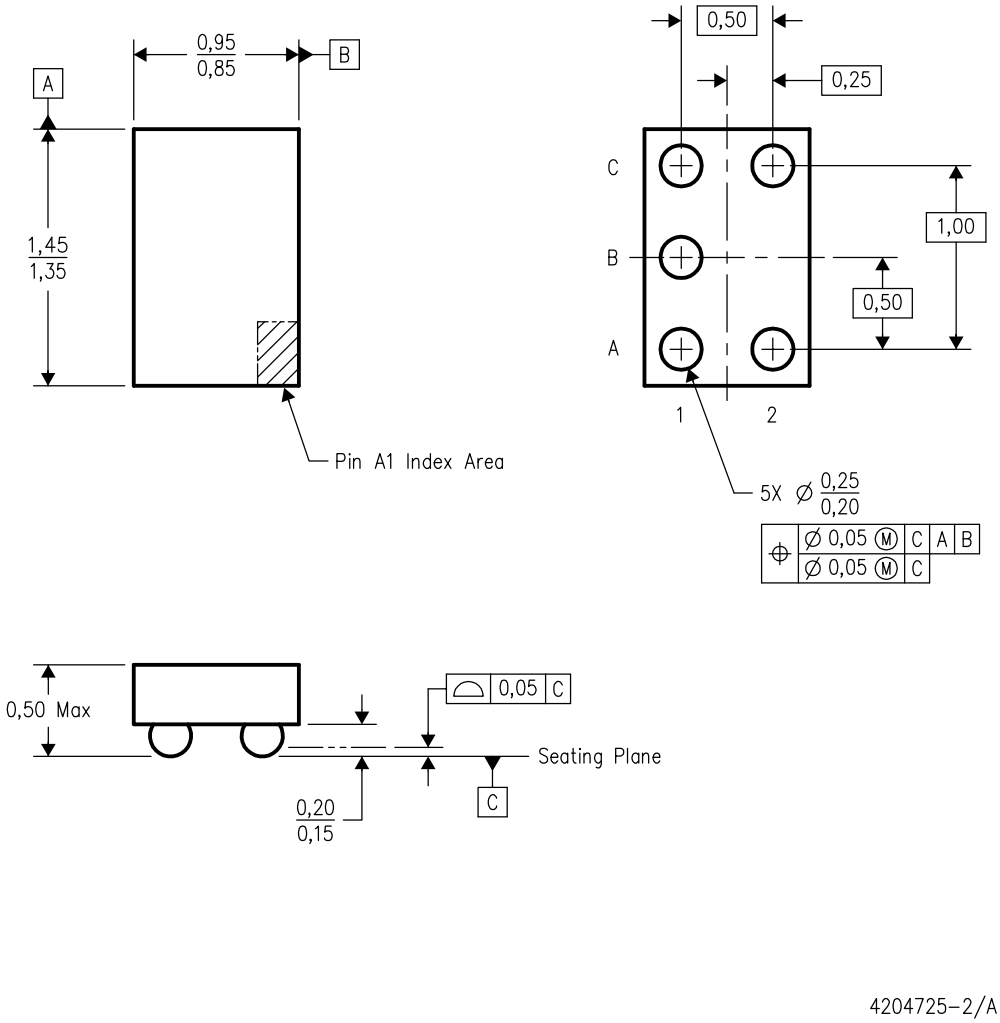
YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

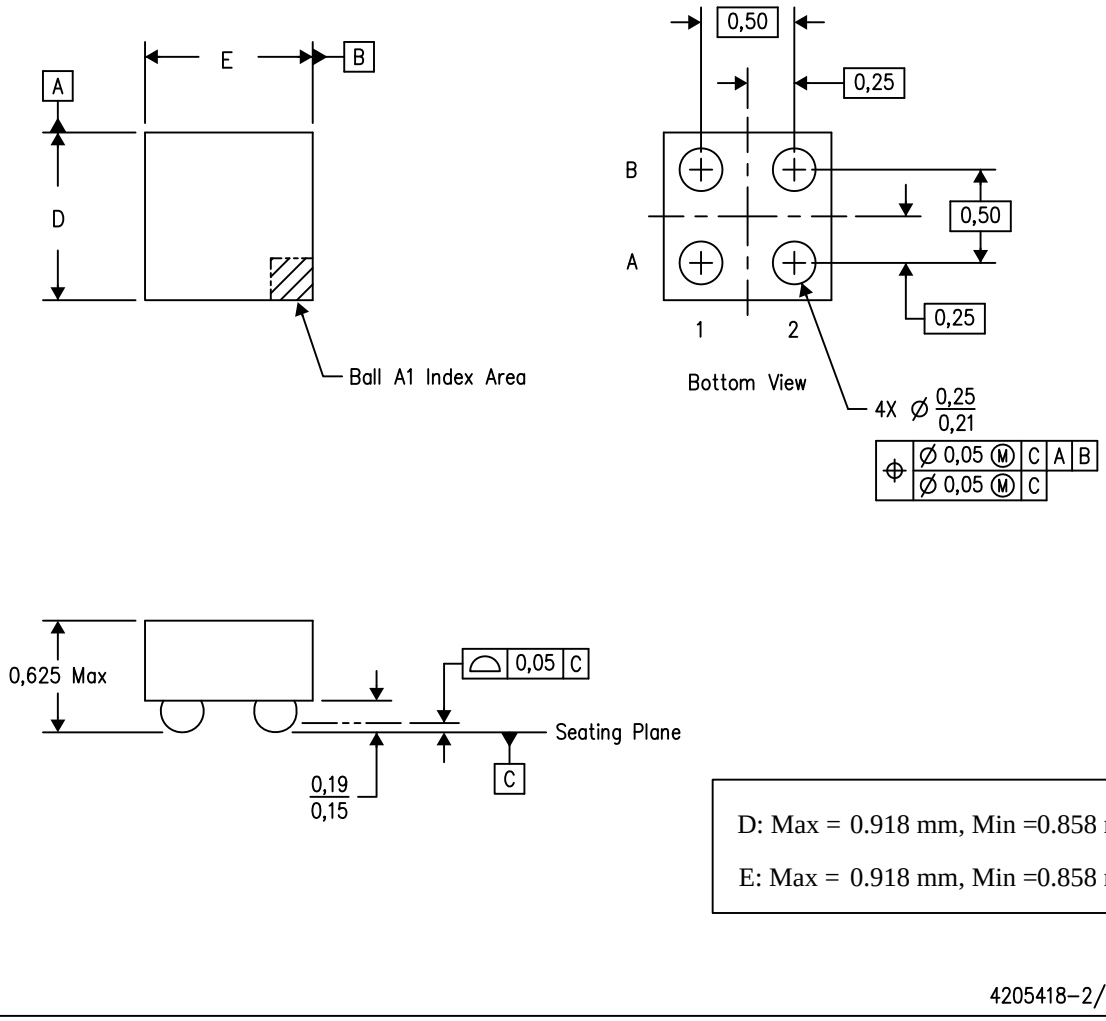
YEP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead–free.

**NanoStar is a trademark of Texas Instruments.**

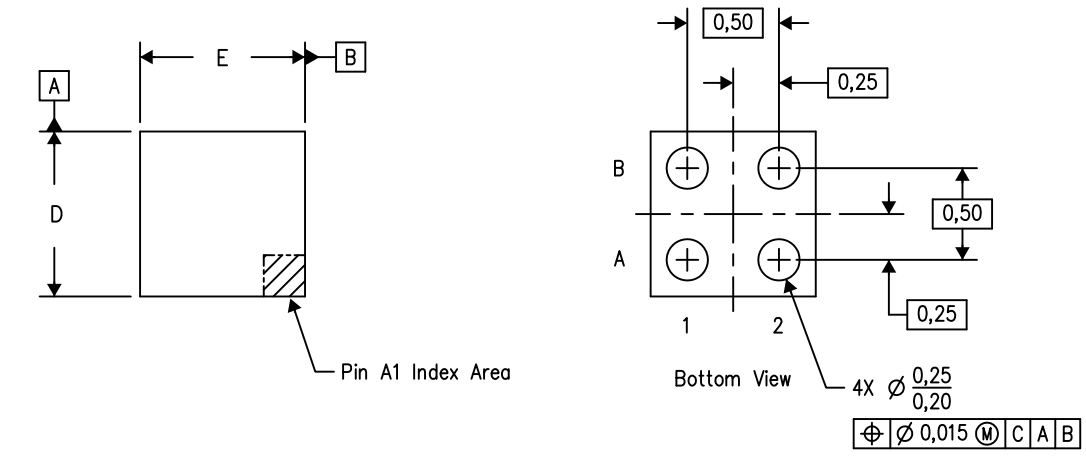
YZT (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY

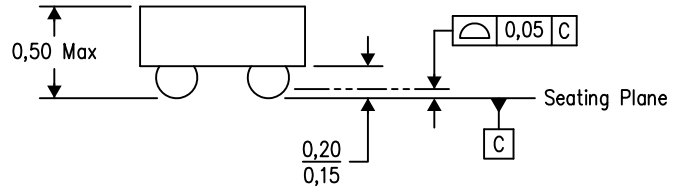



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY




D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/C 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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