Application Note: AN_SY6280

Low Loss Power Distribution Switch
TARGET DESIGN SPECIFICATION
Preliminary Spec

General Description

The SY6280 develops ultra-low Rds(on) switch with programmable current limiting to protect the power source from over current and short circuit conditions. It integrates the over temperature protection and discharges the output capacitor during the shutdown. In case the output is pulled higher than the input voltage under the shutdown, the SY6280 can block the current flowing from the output to the input.

Features

- Distribution voltages: 2.4V to 5.5V
- Programmable current limit
- Enable polarity: active high
- Over temperature shutdown and automatic retry
- Reverse blocking (no body diode)
- At shutdown, OUT can be forced higher than IN
- Automatic output discharge at shutdown
- Compact SOT23 packages minimize the board space.

Ordering Information

SY6280□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
SY6280AAC	SOT23-5	----

Applications

- USB 3G Datacard
- USB Dongle
- MiniPCI Accessories

Typical Applications

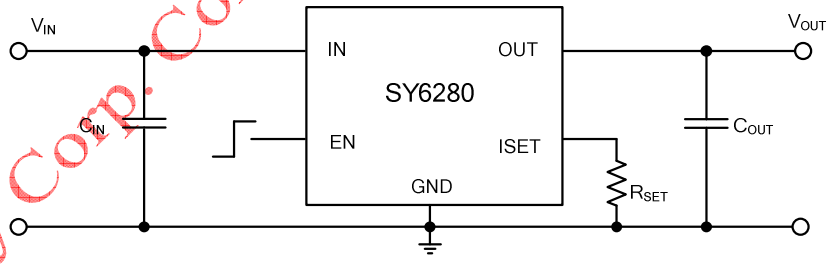
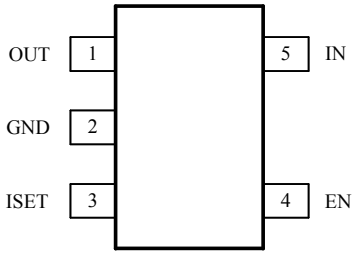


Figure 1. Schematic Diagram

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Pinout (top view)



(SOT23-5)

Top mark: **CO*xyz*** (Device code: CO, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin number	Pin Description
IN	5	Input pin
GND	2	Ground pin
OUT	1	Output pin
EN	4	ON/OFF control. Pull high to enable IC. Do not float.
ISET	3	Current limit programming pin. Connect a resistor Rset from this pin to GND to program the current limit: Ilim (A)=6800/Rset (ohm)

Absolute Maximum Ratings (Note 1)

All pins---------- 6V
Power Dissipation, P_D @ T_A = 25°C SOT23-5, ---------- 0.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 200°C/W
θ_{JC} ---------- 130°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

IN---------- 2.4V to 5.5V
All other pins ---------- 0-5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

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Electrical Characteristics

(V_{IN} = 5V, CL=1uF, per channel, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.4		5.5	V
Shutdown Input Current	I_{SHDN}	Open load, IC Disabled.		0.1	1	μA
Quiescent Supply Current	I_Q	Open load, IC Enabled.		25		μA
FET RON	$R_{DS(ON)1}$			80		mΩ
EN Rising Threshold	$V_{EN(H)}$		2			V
EN Falling Threshold	$V_{EN(L)}$				0.8	V
EN Leakage	I_{EN}	V_{EN}=5.5V			1	μA
IN UVLO Threshold	$V_{IN,UVLO}$				2.3	V
IN UVLO Hysteresis	$V_{IN,HYS}$			0.1		V
Over Current Limit	I_{LIM}	R_{SET}=6.8kΩ	0.75	1	1.25	A
	$I_{LIM(min)}$			0.4		A
	$I_{LIM(max)}$			2		A
Turn-ON Time	T_{ON}	R_L=10Ω		120		us
Turn-OFF Time	T_{OFF}	R_L=10Ω, C_L=1uF		10		us
OUT Shutdown Discharge Resistance	R_{DIS}			150		Ω
Thermal Shutdown Temperature	T_{SD}			130		℃
Thermal Shutdown Hysteresis				20		℃

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

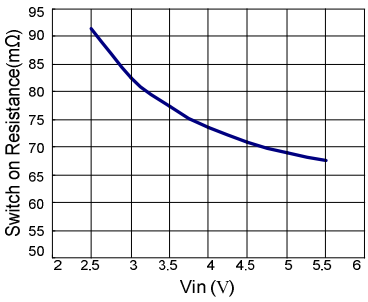
Note 2: θJA is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 2 of SOT23-5 packages is the case position for θJC measurement.

Note 3: The device is not guaranteed to function outside its operating conditions

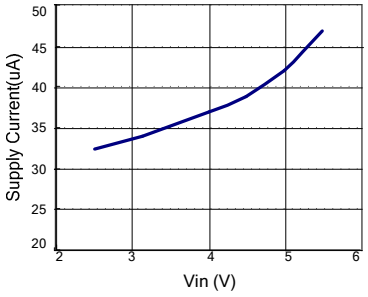
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Typical Operating Characteristics

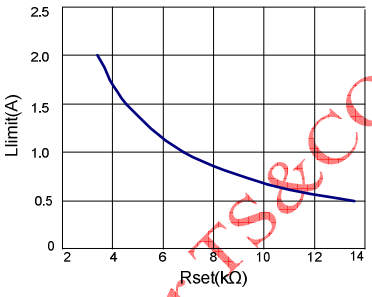
Switch on Resistance VS Input Voltage



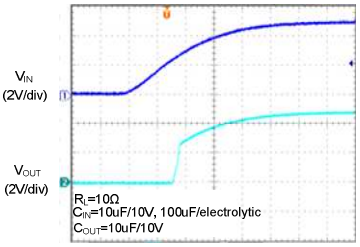
Supply Current VS Input Voltage



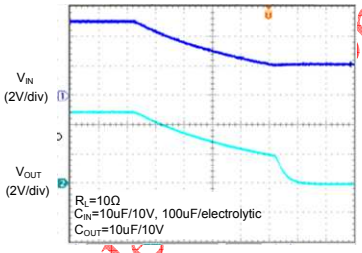
Llimit VS Rset



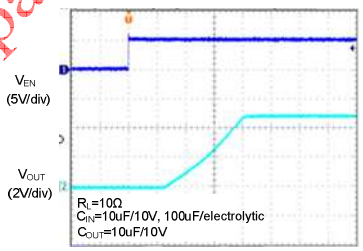
UVLO at Rising



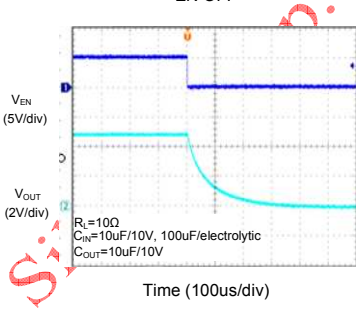
UVLO at Falling



EN ON



EN OFF



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Operation

The SY6280 is a current limited P-channel MOSFET power switch designed for high-side load-switching applications. There is no parasitic body diode between drain and source of the MOSFET, so the SY6280 prevents current flow from out to input when out being externally forced to a higher voltage than vin when chip is disabled.

Over-current protection

When the over-current condition is sensed, the gate of the pass switch is modulated to achieve constant output current. Under output short circuit conditions, the normal current limit folded back 50%. If the over current condition presists for a long enough time, the junction temperature may exceed 130C, and over-temperature protection will shut down the part. Once the chip temperature drops to 110C, the part will restart.

Supply Filter Capacitor

In order to prevent the input voltage drooping during hot-plug events, a 10uF ceramic capacitor form V_{IN} to GND is strongly recommended. However, higher capacitor values could reduce the voltage droop on the input further. Furthermore, an output short will cause ringing on the input without the input capacitor. It could destroy the internal circuitry when the input transient exceed 6V which is the absolute maximum supply voltage even for a short duration.

Current Limiting Setting

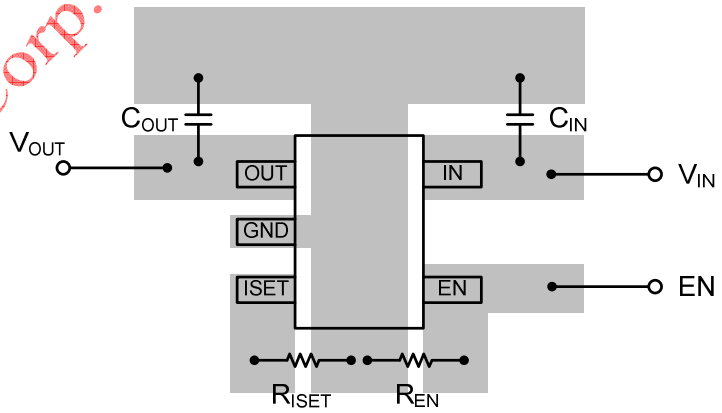
Current limiting is programmable to protect the power source from over current and short circuit conditions. Connect a resistor R_{SET} from this ISET pin to GND to program the current limit:

Ilim (A)=6800 / Rset (ohm).

PCB Layout Guide

For best performance of the SY6280 , the following guidelines must be strictly followed:

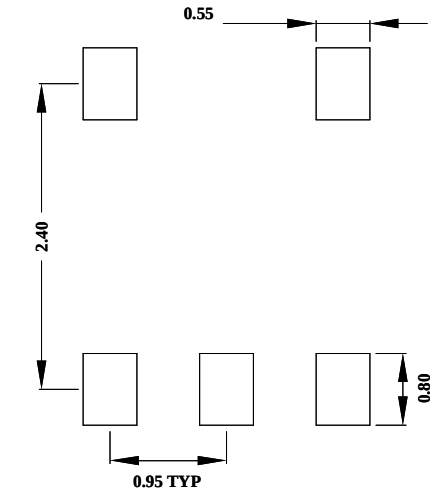
- Keep all V_{BUS} traces as short and wide as possible and use at least 2 ounce copper for all V_{BUS} traces.
- Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.
- Locate the output capacitor as close to the connectors as possible to lower impedance(mainly inductance) between the port and the capacitor and improve transient performance.
- Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.
- Locate the ceramic bypass capacitors as close as possible to the V_{IN} pins and V_{OUT} pins of SY6280.



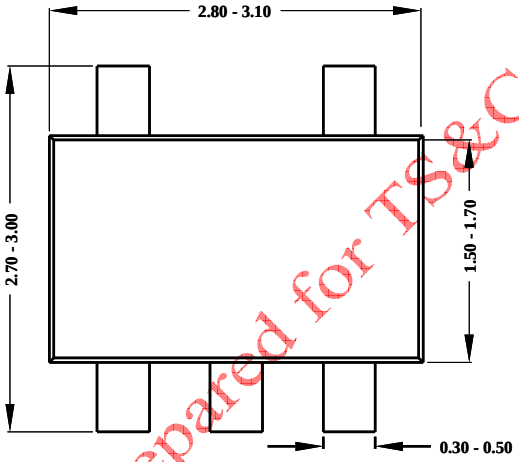
PCB Layout Guide(SOT23-5)

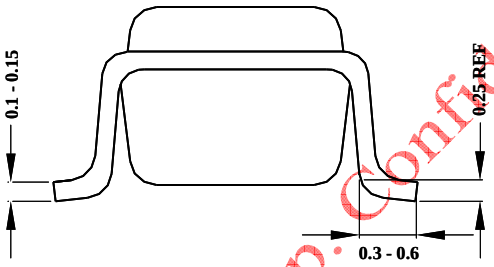
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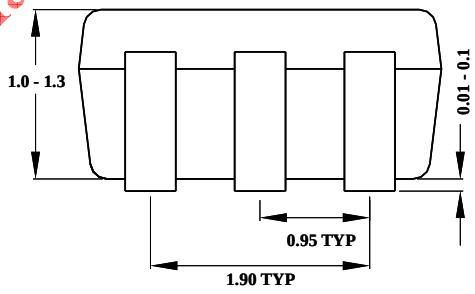
SOT23-5 Package outline & PCB layout design



Recommended Pad Layout







Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

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