Single Synchronous Buck PWM Controller

General Description

The RT8228A PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers.

The constant on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT8228A achieves high efficiency at a reduced cost by eliminating the current sense resistor found in traditional current mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs and enter diode emulation mode at light load condition. The buck conversion allows this device to directly step down high voltage batteries at the highest possible efficiency. The Audio Skipping Mode (ASM) setting maintains the switching frequency above 25kHz, which eliminates noise in audio applications. The RT8228A is intended for CPU core, chipset, DRAM, or other low voltage supplies as low as 0.5V. The RT8228A is available in a WQFN-12L 2x2 package.

Ordering Information

RT8228A□□

Package Type
QW : WQFN-12L 2x2 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)
Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

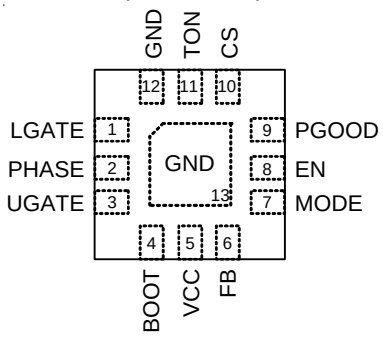
- **Built in 1% 0.5V Reference Voltage**
- **Adjustable 0.5V to 3.3V Output Range**
- **Quick Load Step Response within 100ns**
- **4700ppm/°C Programmable Current Limit by Low Side $R_{DS(ON)}$ Sensing**
- **4.5V to 26V Battery Input Range**
- **Resistor Programmable Frequency**
- **Internal Ramp Current Limit Soft-Start Control**
- **Drives Large Synchronous Rectifier FETs**
- **Integrated Boost Switch**
- **Over/Under Voltage Protection**
- **Thermal Shutdown**
- **Power Good Indicator**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook Computers
- CPU Core Supply
- Chipset/RAM Supply as Low as 0.5V
- Generic DC/DC Power Regulator

Pin Configurations

(TOP VIEW)

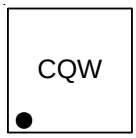


WQFN-12L 2x2

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Marking Information

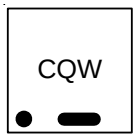
RT8228AGQW



CQ : Product Code

W : Date Code

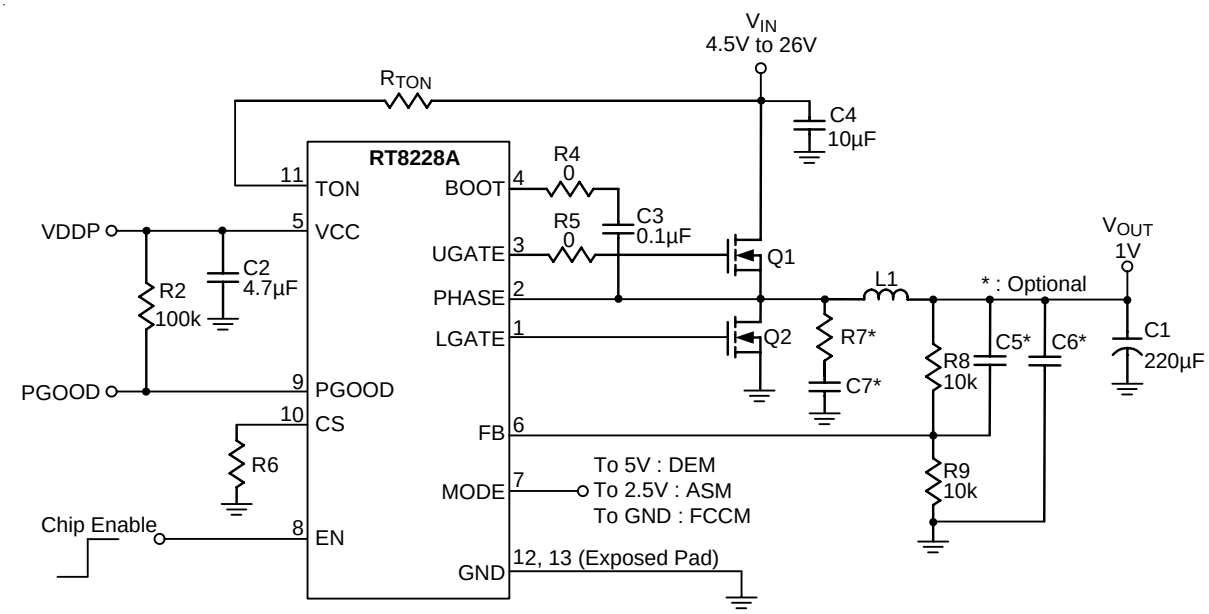
RT8228AZQW



CQ : Product Code

W : Date Code

Typical Application Circuit

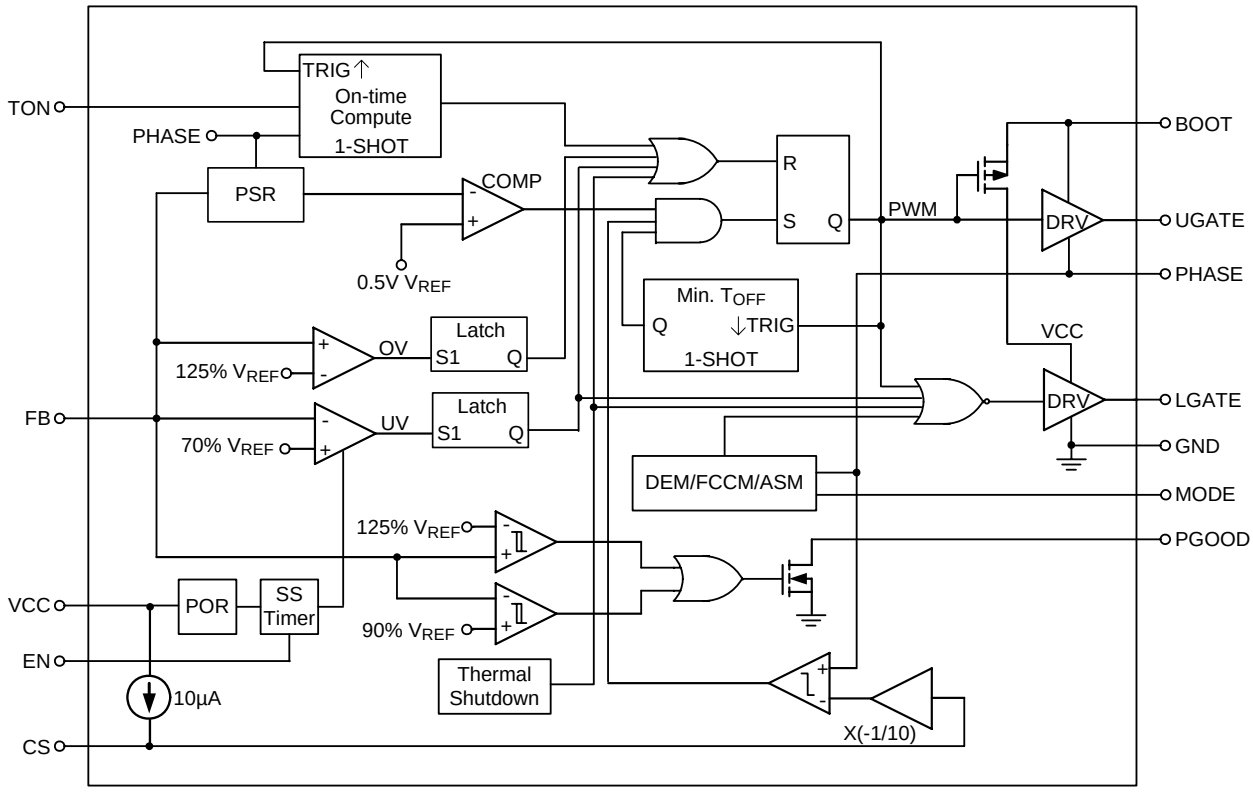


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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LGATE	Gate Drive Output for Low Side External MOSFET.
2	PHASE	External Inductor Connection Pin for PWM Converter. It behaves as the current sense comparator input for Low Side MOSFET $R_{DS(ON)}$ sensing and reference voltage for on time generation.
3	UGATE	Gate Drive Output for High Side External MOSFET.
4	BOOT	Supply Input for High Side Driver. Connect through a capacitor to the floating node (PHASE) pin.
5	VCC	Control Voltage Input. Provides the power for the buck controller, the low side driver and the bootstrap circuit for high side driver. Bypass to GND with a 4.7μF ceramic capacitor.
6	FB	V_{OUT} Feedback Input. Connect FB to a resistive voltage divider from V_{OUT} to GND to adjust the output from 0.5V to 3.3V
7	MODE	Pull Down to GND for Forced CCM Mode. Pull Up to 2.5V for Audio Skipping Mode (ASM). Pull Up to 5V for Diode Emulation Mode (DEM).
8	EN	PWM Chip Enable. Pull low to GND to disable the PWM.
9	PGOOD	Open Drain Power Good Indicator. High impedance indicates power is good.
10	CS	Current Limit Threshold Setting Input. Connect a setting resistor to GND and the current limit threshold is equal to 1/10 of the voltage at this pin.
11	TON	On-time Setting. Connect a resistor between this pin and V_{IN}.
12, 13 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6V
- FB, PGOOD, EN, CS, MODE to GND ---------- –0.3V to (VCC + 0.3V)
- TON to GND ---------- –0.3V to 32V
- BOOT to PHASE ---------- –0.3V to 6.5V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - < 20ns ---------- –8V to 38V
- UGATE to PHASE
  - DC ---------- –0.3V to (VCC + 0.3V)
  - < 20ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to (VCC + 0.3V)
  - < 20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-12L 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  - WQFN-12L 2x2, θ_{JA} ---------- 165°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 4.5V to 26V
- Control Voltage, V_{CC} ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

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Electrical Characteristics

(V_{CC} = 5V, V_{IN} = 15V, V_{EN} = 5V, V_{MODE} = 5V, R_{TON} = 500kΩ, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
V_{CC} Quiescent Supply Current	I_Q	FB forced above the regulation point, V_{EN} = 5V	--	0.5	1.25	mA
V_{CC} Shutdown Current	I_{SHDN}	V_{CC} Current, V_{EN} = 0V	--	--	1	μA
TON Operating Current		R_{TON} = 500k	--	30	--	μA
TON Shutdown Current		R_{TON} = 500k	--	--	1	μA
CS Shutdown Current		CS pull to GND	--	--	1	μA
FB Error Comparator Threshold Voltage		V_{CC} = 4.5V to 5.5V, DEM	495	500	505	mV
FB Input Bias Current		V_{FB} = 0.5V	–1	0.1	1	μA
Output Voltage Range			0.5	--	3.3	V
On-Time		V_{IN} =15V, V_{PHASE} = 1.25V, V_{MODE} = 0V	267	334	401	ns
Minimum Off-Time		V_{MODE} = 0V, FB = 0.45V	250	400	550	ns
Current Sensing Threshold						
CS Source Current		V_{CS} = 0.5V to 2V	9	10	11	μA
CS Source Current TC		On the basis of 25°C	--	4700	--	ppm/°C
Zero Crossing Threshold		V_{MODE} > 1.8V, PHASE – GND	–10	--	5	mV
ASM Min Frequency		V_{MODE} = 2.5V	--	25	--	kHz
Protection Function						
Current Limit Threshold		GND – PHASE, V_{CS} = 1V	85	100	115	mV
UV Threshold		UVP Detect, FB Falling Edge	60	70	80	%
OVP Threshold		OVP Detect, FB Rising Edge	120	125	130	%
OV Fault Delay		FB forced above OV threshold	--	5	--	μs
V_{CC} Power On Reset (POR) Threshold		Rising Edge	3.7	3.9	4.2	V
POR Threshold Hysteresis			--	100	--	mV
Current Limit Ramp at Soft-Start		Enable to current limit threshold = 50mV	--	900	--	μs
UV Blank Time		From EN signal going high	--	4.5	--	ms
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	10	--	°C
Driver On-Resistance						
UGATE Driver Source	$R_{UGATEsr}$	BOOT – PHASE forced to 5V, UGATE High State	--	2.5	5	Ω
UGATE Driver Sink	$R_{UGATEsk}$	BOOT – PHASE forced to 5V, UGATE Low State	--	1.5	3	Ω
LGATE Driver Source	$R_{LGATEsr}$	LGATE High State	--	2.5	5	Ω
LGATE Driver Sink	$R_{LGATEsk}$	LGATE Low State	--	0.8	1.5	Ω
Dead Time		LGATE Rising (Phase = 1.5V)	--	30	--	ns
		UGATE Rising	--	30	--	

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Boost Charging Switch on Resistance			V_{CC} to BOOT, 10mA	--	--	80	Ω
EN Threshold							
EN Threshold Voltage	Logic-High	V_{IH}		1.2	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
Mode Threshold							
DEM Threshold				V_{CC} – 0.5	--	--	V
ASM Threshold				1.8	--	2.9	V
FCCM Threshold				--	--	0.4	V
PGOOD (upper side threshold decided by OV threshold)							
Trip Threshold (Falling)			Measured at FB, with respect to reference	–13	–10	–7	%
Trip Threshold Hysteresis				--	3	--	%
Fault Propagation Delay			Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage			I_{SINK} = 1mA	--	--	0.4	V
Leakage Current			High state, forced to 5V	--	--	1	μA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings, Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

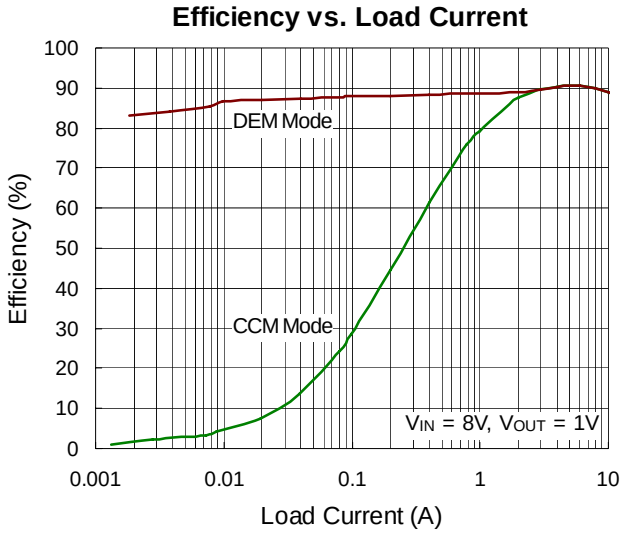
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

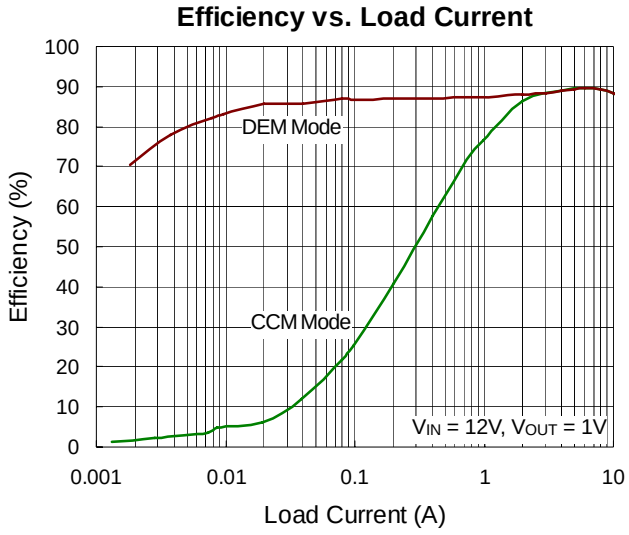
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

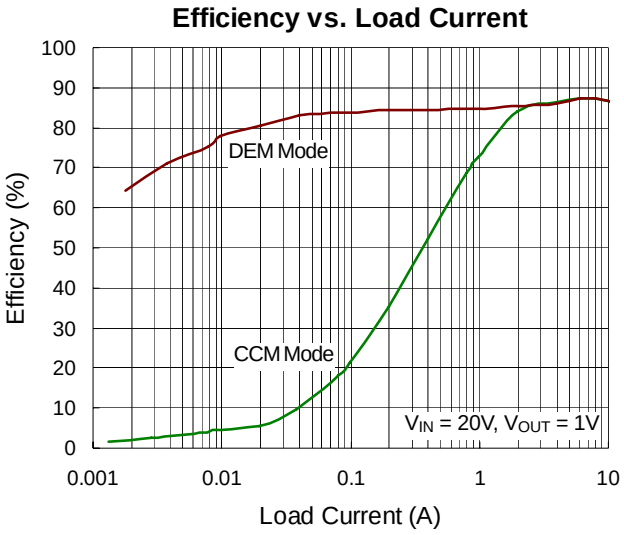
Note 4. The device is not guaranteed to function outside its operating conditions.

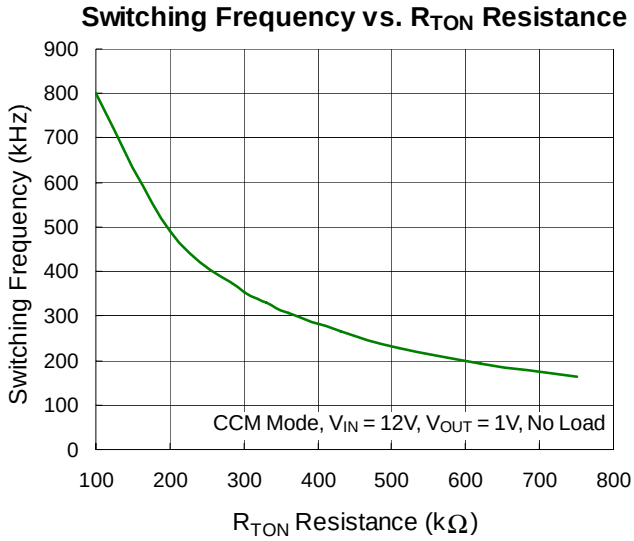
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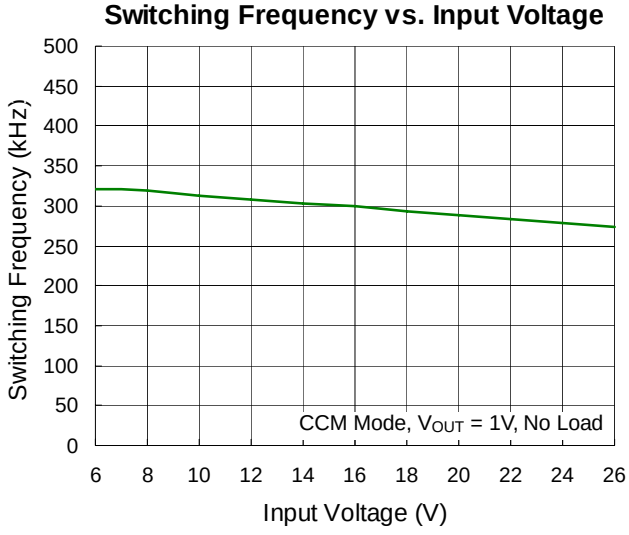
Typical Operating Characteristics

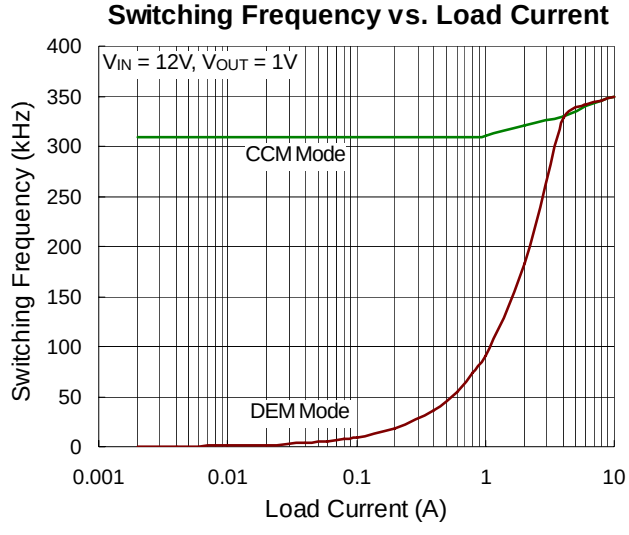






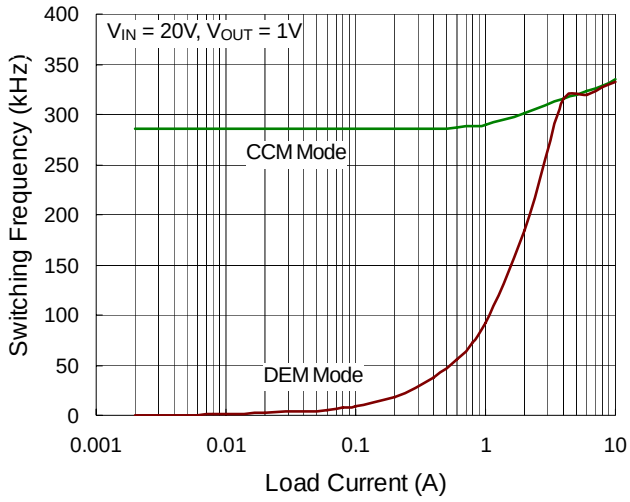




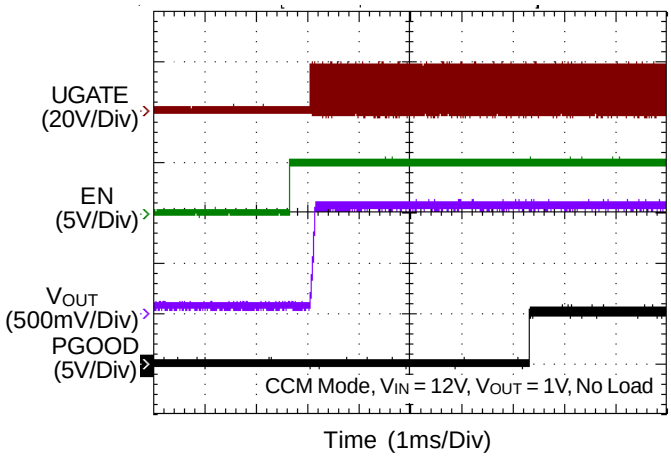


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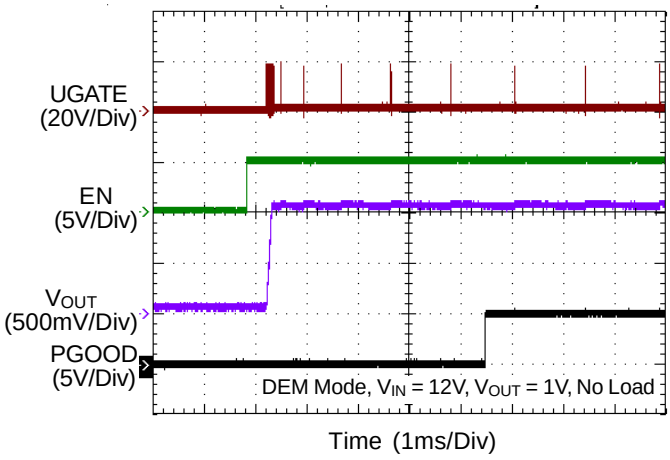
Switching Frequency vs. Load Current



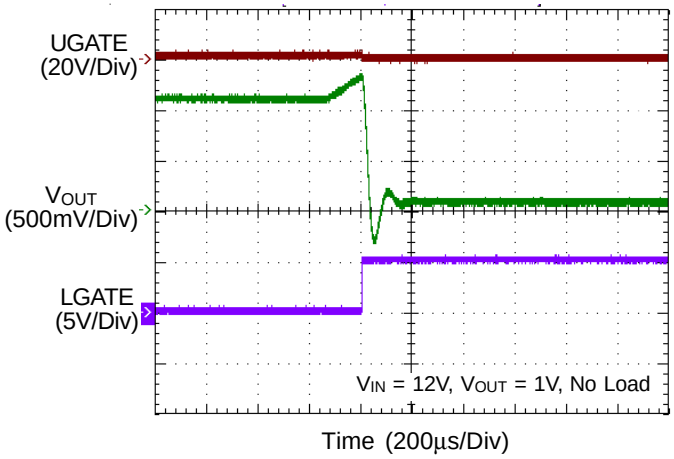
Power On from EN



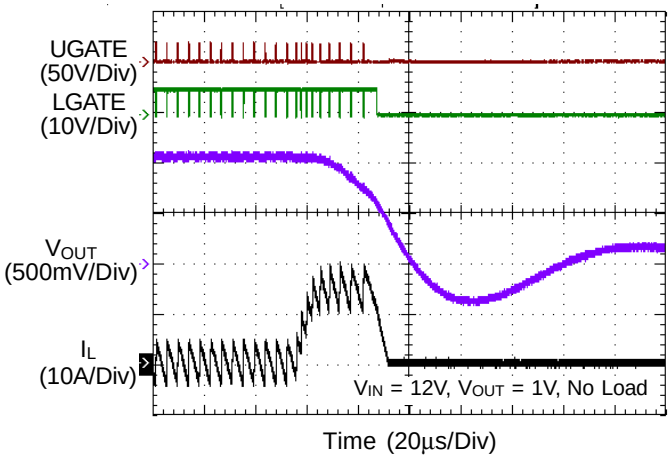
Power On from EN



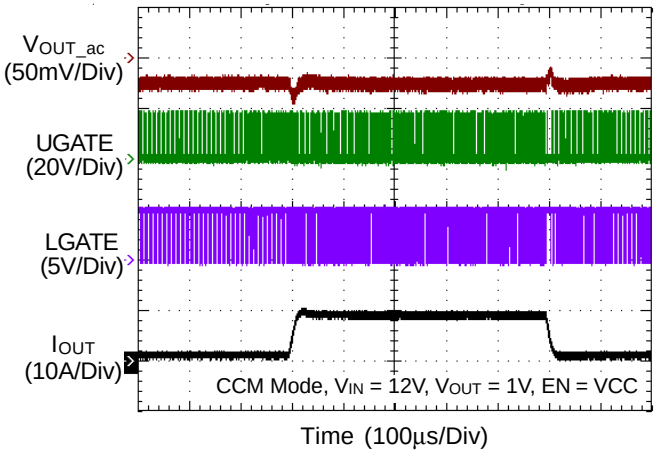
OVP



UVP

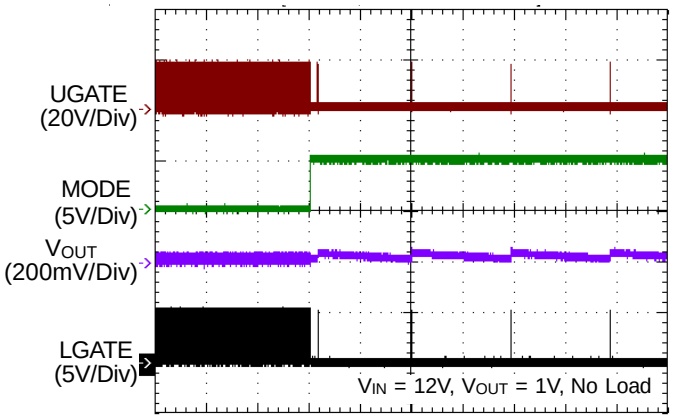


Load Transient Response

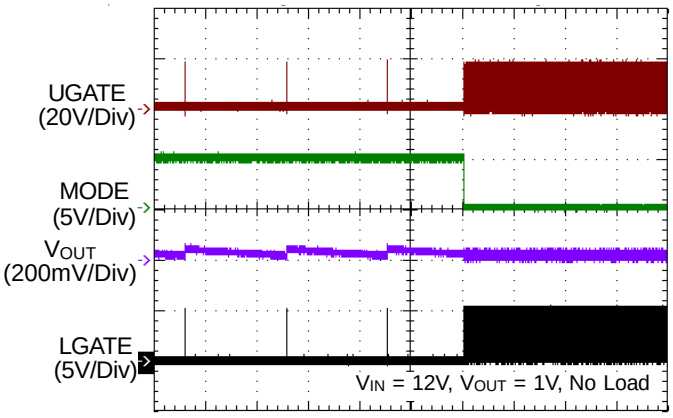


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Mode Transition CCM to DEM



Mode Transition DEM to CCM



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Application Information

The RT8228A PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers. Richtek Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load transient timing problems of fixed frequency current mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes. The PSR PWM modulator is specifically designed to have better noise immunity for such a single output application.

PWM Operation

The Mach Response™, PSR (Pulse Shaping Regulator) mode controller is suitable for low external component count configuration with appropriate amount of Equivalent Series Resistance (ESR) capacitor(s) at the output. The output ripple valley voltage is monitored at a feedback point voltage. Refer to the function diagrams of the RT8228A, the synchronous high side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET is turned off. The pulse width of this one shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

On-Time Control

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high side switch directly proportional to the output voltage and inversely proportional to the input voltage. The implementation results in a nearly constant switching frequency without the need of a clock generator.

$$t_{ON} = \frac{7.06p \times R_{TON} \times V_{OUT}}{(V_{IN} - 0.9)} + 33ns$$

where R_{TON} is the resistor connected from the input supply (V_{IN}) to the TON pin.

And then the switching frequency is :

$$\text{Frequency} = \frac{V_{OUT}}{V_{IN} \times t_{ON}}$$

Mode Selection Operation

DEM (Diode Emulation Mode) and ASM (Audio Skipping Mode) operation can be enabled by driving the tri-state MODE pin to a logic high level. The RT8228A can switch operation into DEM when the MODE pin is pulled up to 5V. If MODE is pulled to 2.5V, the controller will switch operation into ASM. Finally, if the pin is pulled to GND, the RT8228A will operate in CCM mode.

Diode Emulation Mode

In diode emulation mode, the RT8228A automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increasing VOUT ripple or load regulation. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial of negative current when the inductor freewheeling current reach negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level than requires the next "ON" cycle. The on-time is kept the same as that in the heavy load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light load operation can be calculated as follows (Figure 1) :

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is On-time.

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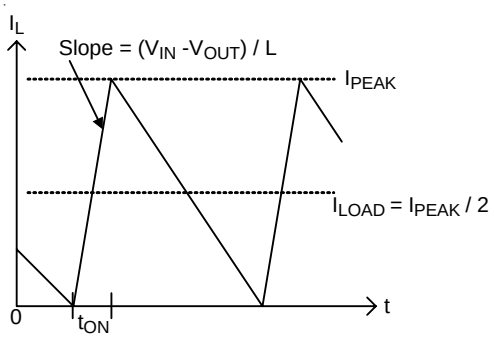


Figure 1. Boundary Condition of CCM/DEM

The switching waveforms may appear noisy and asynchronous when light loading causes diode emulation operation, but this is a normal operating condition that results in high light load efficiency. Trade offs in DEM noise vs. light load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degrade load transient response (especially at low input voltage levels).

Audio Skipping Mode

When the MODE pin is pulled to 2.5V, the controller operates in audio skipping mode with a minimum switching frequency of 25kHz. This mode eliminates audio frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In audio skipping mode, the low side switch gate driver signal is ORed with an internal oscillator (>25kHz). Once the internal oscillator is triggered, the audio skipping controller pulls LGATE logic high, turning on the low side MOSFET to induce a negative inductor current. After the output voltage rises above V_{REF}, the controller turns off the low side MOSFET (LGATE pulled logic low) and triggers a constant on-time operation (UGATE driven logic high). When the on-time operation expires, the controller re-enables the low side MOSFET until the inductor current drops below the zero crossing threshold.

Forced-CCM Mode

The low noise, forced-CCM mode (MODE = GND) disables the zero-crossing comparator, which controls the low side switch on-time. This causes the low side gate drive waveform to become the complement of the high side gate drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio V_{OUT}/V_{IN}. The benefit of forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost. The no load battery current can be up to 10mA to 40mA, depending on the external MOSFETs.

Current Limit Setting (OCP)

The RT8228A has cycle-by-cycle current limiting control. The current limit circuit employs a unique “valley” current sensing algorithm. If PHASE voltage plus the current limit threshold is below zero, the PWM is not allowed to initiate a new cycle (Figure 2). In order to provide both good accuracy and a cost effective solution, the RT8228A supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The CS pin should be connected to GND through the trip voltage setting resistor, R_{CS}. With the 10μA CS terminal source current, I_{CS}, and the setting resistor, R_{CS} the CS trip voltage, V_{CS}, can be calculated as shown in the following equation.

V_{CS} (mV) = R_{CS} (kΩ) x 10 (μA) x (1 / 10)

Inductor current is monitored by the voltage between the PGND pin and the PHASE pin, so the PHASE pin should be connected to the drain terminal of the low side MOSFET. I_{CS} has positive temperature coefficient to compensate the temperature dependency of the $R_{DS(ON)}$. PGND is used as the positive current sensing node so PGND should be connected to the source terminal of the bottom MOSFET.

As the comparison is done during the OFF state, V_{CS} sets the valley level of the inductor current. Thus, the load current at over current threshold, I_{LOAD_OC}, can be calculated as follows.

$$I_{LOAD_OC} = \frac{VCS}{RDS(ON)} + \frac{IRipple}{2}$$

$$= \frac{V_{CS}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

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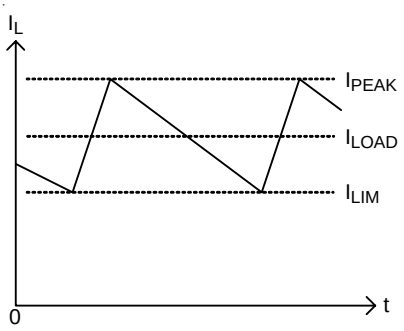


Figure 2. Valley Current Limit

MOSFET Gate Driver (UGATE, LGATE)

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET (s). When configured as a floating driver, 5V bias voltage is delivered from the VDDP supply. The average drive current is proportional to the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOT and PHASE pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on and low side MOSFET off to high side MOSFET on. The low side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET (s). The internal pull down transistor that drives LGATE low is robust, with a 0.8Ω typical on resistance. A 5V bias voltage is delivered from the VDDP supply. The instantaneous drive current is supplied by the flying capacitor between VDDP and GND.

For high current applications, some combinations of high and low side MOSFETs might be encountered that will cause excessive gate drain coupling, which can lead to efficiency killing, EMI-producing shoot through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high side MOSFET without degrading the turn-off time (Figure 3).

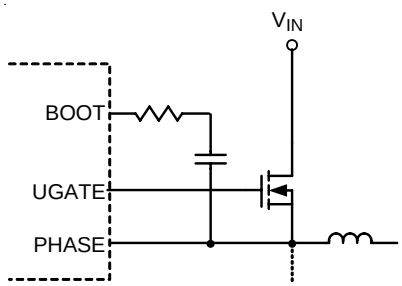


Figure 3. Reducing the UGATE Rise Time

Power Good Output (PGOOD)

The power good output is an open drain output and requires a pull-up resistor. When the output voltage is 25% above or 10% below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. In soft-start, PGOOD is actively held low and is allowed to transition high until soft-start is over and the output reaches 93% of its set voltage. There is a 2.5μs delay built into PGOOD circuitry to prevent false transitions.

POR, UVLO and Soft-Start

Power On Reset (POR) occurs when VCC rises above to approximately 3.9V, the RT8228A will reset the fault latch and preparing the PWM for operation. Below 3.7V, the VCC Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low. A built-in soft-start is used to prevent surge current from power supply input after EN is enabled. A current ramping up limit threshold can eliminate the V_{OUT} folded-back in the soft-start duration. The typical soft-start duration is 900μs.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage protection. When the output voltage exceeds 25% of the set voltage threshold, over voltage protection is triggered and the low side MOSFET is latched on. This activates the low side MOSFET to discharge the output capacitor. The RT8228A is latched once OVP is triggered and can only be released by VCC or EN power on reset. There is a 5μs delay built into the over voltage protection circuit to prevent false transitions.

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When the output voltage is less than 70% of the set voltage threshold, under voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. During soft-start, the UVP blanking time is 4.5ms.

Output Voltage Setting (FB)

The output voltage can be adjusted from 0.5V to 3.3V by setting the feedback resistor R1 and R2 (Figure 4). Choose

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R2 to be approximately 10kΩ, and solve for R1 using the equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is 0.5V.(typ.)

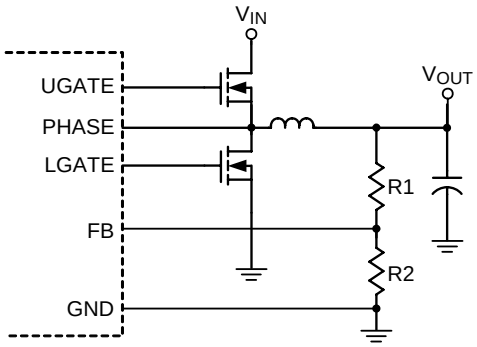


Figure 4. Setting VOUT with a Resistor Divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows :

$$L = \frac{T_{ON} \times (V_{IN} - V_{OUT})}{L_{IR} \times I_{LOAD(MAX)}}$$

where L_{IR} is the ratio of peak-of-peak ripple current to the maximum average inductor current. Find a low pass inductor having the lowest possible DC resistance that fits in the allowed dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough and not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left[\left(\frac{L_{IR}}{2}\right) \times I_{LOAD(MAX)}\right]$$

Output Capacitor Selection

The output filter capacitor must have low enough Equivalent Series Resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must also be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault latch.

Although Mach Response™ DRV™ dual ramp valley mode provides many advantages such as ease-of-use, minimum external component configuration, and extremely short response time, due to not employing an error amplifier in the loop, a sufficient feedback signal needs to be provided by an external circuit to reduce the jitter level. The required signal level is approximately 15 mV at the comparing point. This generates $V_{RIPPLE} = (V_{OUT} / 0.5) \times 15mV$ at the output node. The output capacitor ESR should meet this requirement.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8228A, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-12L 2x2 package, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)} = (125°C - 25°C) / (165°CW) = 0.606W$ for

WQFN-12L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8228A package, the derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

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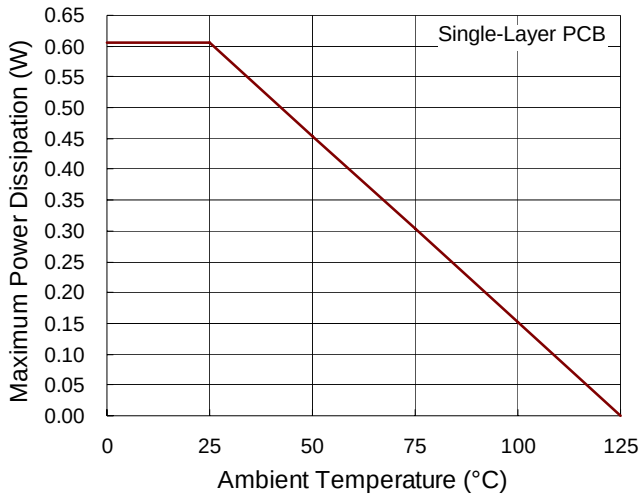


Figure 5. Derating Curves for RT8228A Packages

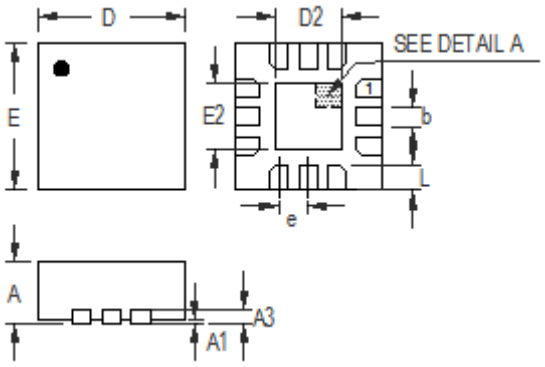
Layout Considerations

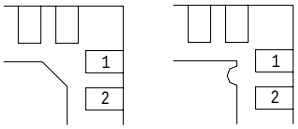
Layout is very important in high frequency switching converter design. If the layout is designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. The following points must be followed for a proper layout of RT8228A.

- Connect a filter capacitor to VCC, 1μF to 4.7μF range is recommended. Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as MODE, FB, GND, EN, PGOOD, CS, VCC, and TON should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer (s) as ground plane (s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane (s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

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Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
e	0.400		0.016	
D2	0.850	0.950	0.033	0.037
E2	0.850	0.950	0.033	0.037
L	0.250	0.350	0.010	0.014

W-Type 12L QFN 2x2 Package

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