NX3L4684

Low-ohmic dual single-pole double-throw analog switch

Rev. 8 — 3 April 2014 Product data sheet

1. General description

The NX3L4684 is a dual low-ohmic single-pole double-throw analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input (nS), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ).

Schmitt trigger action at the digital inputs makes the circuit tolerant to slower input rise and fall times. Low threshold digital inputs allows this device to be driven by 1.8 V logic levels in 3.3 V applications without significant increase in supply current I_{CC}. This makes it possible for the NX3L4684 to switch 4.3 V signals with a 1.8 V digital controller, eliminating the need for logic level translation. The NX3L4684 allows signals with amplitude up to V_{CC} to be transmitted from nZ to nY0 or nY1; or from nY0 or nY1 to nZ. Its low ON resistance (0.3 Ω for Y0 port, 0.5 Ω for Y1 port) and flatness (0.1 Ω) ensures minimal attenuation and distortion of transmitted signals.

2. Features and benefits

- Wide supply voltage range from 1.4 V to 4.3 V
- Very low ON resistance (peak) for Y0 port:
  - 0.8 Ω (typical) at V_{CC} = 1.4 V
  - 0.5 Ω (typical) at V_{CC} = 1.65 V
  - 0.3 Ω (typical) at V_{CC} = 2.3 V
  - 0.25 Ω (typical) at V_{CC} = 2.7 V
  - 0.25 Ω (typical) at V_{CC} = 4.3 V
- Break-before-make switching
- High noise immunity
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
  - IEC61000-4-2 contact discharge exceeds 6000 V for switch ports
- CMOS low-power consumption
- Latch-up performance exceeds 100 mA per JESD 78B Class II Level A
- 1.8 V control logic at V_{CC} = 3.6 V
- Control input accepts voltages above supply voltage
- Very low supply current, even when input is below V_{CC}
- High current handling capability (350 mA continuous current under 3.3 V supply)
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Cell phone
- PDA
- Portable media player

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX3L4684GM	–40 °C to +125 °C	XQFN10	plastic extremely thin quad flatpackage; no leads; 10 terminals; body 2 × 1.55 × 0.5 mm	SOT1049-3
NX3L4684TK	–40 °C to +125 °C	HVSON10	plastic thermal enhanced very thin small outline package; no leads; 10 terminals; 3 × 3 × 0.85 mm	SOT650-2

5. Marking

Table 2. Marking

Type number	Marking code
NX3L4684GM	D84
NX3L4684TK	D84

6. Functional diagram

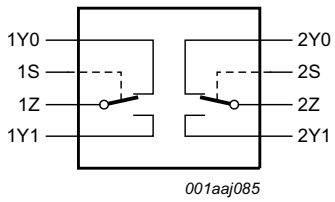


Fig 1. Logic symbol

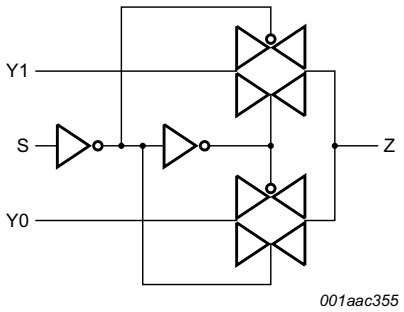


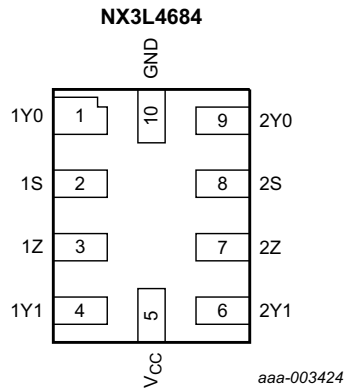
Fig 2. Logic diagram (one switch)

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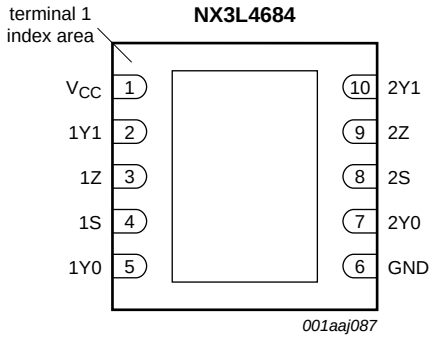
7. Pinning information

7.1 Pinning



Transparent top view

Fig 3. Pin configuration SOT1049-3 (XQFN10)



Transparent top view

Fig 4. Pin configuration SOT650-2 (HVSON10)

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT1049-3	SOT650-2	
1Y0	1	5	independent input or output
1S	2	4	select input
1Z	3	3	common output or input
1Y1	4	2	independent input or output
V_{CC}	5	1	supply voltage
2Y1	6	10	independent input or output
2Z	7	9	common output or input
2S	8	8	select input
2Y0	9	7	independent input or output
GND	10	6	ground (0 V)

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8. Functional description

Table 4. Function table[1]

Input nS	Channel on
L	nY0
H	nY1

[1] H = HIGH voltage level;
L = LOW voltage level.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
V_I	input voltage	select input nS [1]	–0.5	+4.6	V
V_{SW}	switch voltage	switch input nY0 or nY1 [2]	–0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < –0.5 V	–50	-	mA
I_{SK}	switch clamping current	V_I < –0.5 V or V_I > V_{CC} + 0.5 V	-	±50	mA
I_{SW}	switch current	V_{SW} > –0.5 V or V_{SW} < V_{CC} + 0.5 V; source or sink current	-	±350	mA
		V_{SW} > –0.5 V or V_{SW} < V_{CC} + 0.5 V; pulsed at 1 ms duration, < 10 % duty cycle; peak current	-	±500	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C [3]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed but may not exceed 4.6 V.

[3] For XQFN10 packages: above 132 °C the value of P_{tot} derates linearly with 14.1 mW/K.
For HVSON10 packages: above 135 °C the value of P_{tot} derates linearly with 17.2 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.4	4.3	V
V_I	input voltage	select input nS	0	4.3	V
V_{SW}	switch voltage	switch input nY0 or nY1 [1]	0	V_{CC}	V
T_{amb}	ambient temperature		–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.4 V to 4.3 V [2]	-	200	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nYn. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to select input nS signal levels.

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11. Static characteristics

Table 7. Static characteristics

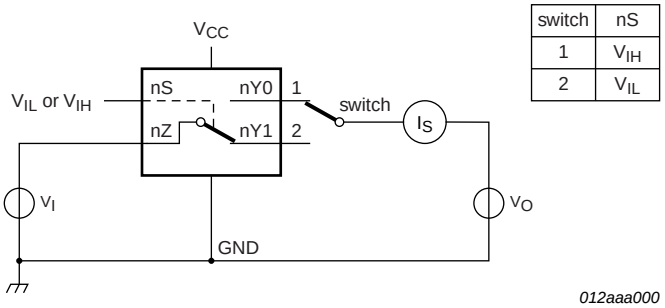
At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.4 V to 1.6 V	0.9	-	-	0.9	-	-	V
		V_{CC} = 1.65 V to 1.95 V	0.9	-	-	0.9	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.1	-	-	1.1	-	-	V
		V_{CC} = 2.7 V to 3.6 V	1.3	-	-	1.3	-	-	V
		V_{CC} = 3.6 V to 4.3 V	1.4	-	-	1.4	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.4 V to 1.6 V	-	-	0.3	-	0.3	0.3	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.4	-	0.4	0.3	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.5	-	0.5	0.4	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.5	-	0.5	0.5	V
		V_{CC} = 3.6 V to 4.3 V	-	-	0.6	-	0.6	0.6	V
I_I	input leakage current	select input nS; V_I = GND to 4.3 V; V_{CC} = 1.4 V to 4.3 V	-	-	-	-	±0.5	±1	µA
$I_{S(OFF)}$	OFF-state leakage current	nYn port; see Figure 5							
		V_{CC} = 1.4 V to 3.6 V	-	-	±5	-	±10	±100	nA
		V_{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±200	nA
$I_{S(ON)}$	ON-state leakage current	nZ port; see Figure 6							
		V_{CC} = 1.4 V to 3.6 V	-	-	±5	-	±20	±200	nA
		V_{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±400	nA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{SW} = GND or V_{CC}							
		V_{CC} = 3.6 V	-	-	100	-	300	3000	nA
		V_{CC} = 4.3 V	-	-	150	-	500	5000	nA
ΔI_{CC}	additional supply current	V_{SW} = GND or V_{CC}							
		V_I = 2.6 V; V_{CC} = 4.3 V	-	2.0	4.0	-	7	7	µA
		V_I = 2.6 V; V_{CC} = 3.6 V	-	0.35	0.7	-	1	1	µA
		V_I = 1.8 V; V_{CC} = 4.3 V	-	7.0	10.0	-	15	15	µA
		V_I = 1.8 V; V_{CC} = 3.6 V	-	2.5	4.0	-	5	5	µA
		V_I = 1.8 V; V_{CC} = 2.5 V	-	50	200	-	300	500	nA
C_I	input capacitance		-	1.0	-	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	port nY0	-	65	-	-	-	-	pF
		port nY1	-	35	-	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	port nY0	-	260	-	-	-	-	pF
		port nY1	-	160	-	-	-	-	pF

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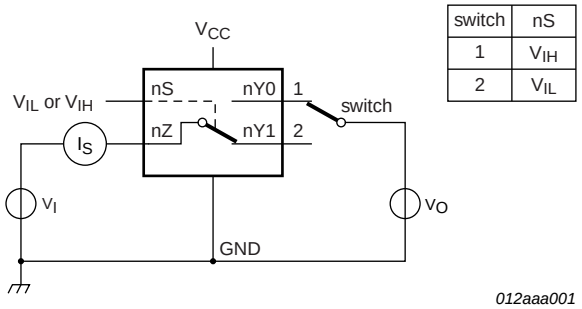
11.1 Test circuits



switch	nS
1	V_{IH}
2	V_{IL}

V_I = 0.3 V or V_{CC} − 0.3 V; V_O = V_{CC} − 0.3 V or 0.3 V.

Fig 5. Test circuit for measuring OFF-state leakage current



switch	nS
1	V_{IH}
2	V_{IL}

V_I = 0.3 V or V_{CC} − 0.3 V; V_O = V_{CC} − 0.3 V or 0.3 V.

Fig 6. Test circuit for measuring ON-state leakage current

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11.2 ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Figure 9 to Figure 21.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	port nY0; see Figure 7; V_I = GND to V_{CC}; I_{SW} = 100 mA						
		V_{CC} = 1.4 V	-	0.85	2.0	-	2.2	Ω
		V_{CC} = 1.65 V	-	0.55	0.8	-	0.9	Ω
		V_{CC} = 2.3 V	-	0.35	0.5	-	0.6	Ω
		V_{CC} = 2.7 V	-	0.30	0.45	-	0.5	Ω
		V_{CC} = 4.3 V	-	0.30	0.45	-	0.5	Ω
		port nY1; see Figure 7; V_I = GND to V_{CC}; I_{SW} = 100 mA						
		V_{CC} = 1.4 V	-	1.65	3.7	-	4.1	Ω
		V_{CC} = 1.65 V	-	0.95	1.6	-	1.7	Ω
		V_{CC} = 2.3 V	-	0.55	0.8	-	0.9	Ω
		V_{CC} = 2.7 V	-	0.50	0.75	-	0.9	Ω
		V_{CC} = 4.3 V	-	0.50	0.75	-	0.9	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = GND to V_{CC}; I_{SW} = 100 mA [2]						
		V_{CC} = 1.4 V	-	0.15	0.3	-	0.3	Ω
		V_{CC} = 1.65 V	-	0.15	0.2	-	0.3	Ω
		V_{CC} = 2.3 V	-	0.04	0.08	-	0.1	Ω
		V_{CC} = 2.7 V	-	0.04	0.075	-	0.1	Ω
		V_{CC} = 4.3 V	-	0.04	0.075	-	0.1	Ω
$R_{ON(flat)}$	ON resistance (flatness)	port nY0; V_I = GND to V_{CC}; I_{SW} = 100 mA [3]						
		V_{CC} = 1.4 V	-	0.5	1.7	-	1.8	Ω
		V_{CC} = 1.65 V	-	0.25	0.6	-	0.7	Ω
		V_{CC} = 2.3 V	-	0.1	0.2	-	0.2	Ω
		V_{CC} = 2.7 V	-	0.1	0.15	-	0.2	Ω
		V_{CC} = 4.3 V	-	0.1	0.20	-	0.25	Ω
		port nY1; V_I = GND to V_{CC}; I_{SW} = 100 mA [3]						
		V_{CC} = 1.4 V	-	1.0	3.3	-	3.6	Ω
		V_{CC} = 1.65 V	-	0.5	1.2	-	1.3	Ω
		V_{CC} = 2.3 V	-	0.15	0.3	-	0.35	Ω
		V_{CC} = 2.7 V	-	0.13	0.3	-	0.35	Ω
		V_{CC} = 4.3 V	-	0.2	0.4	-	0.45	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

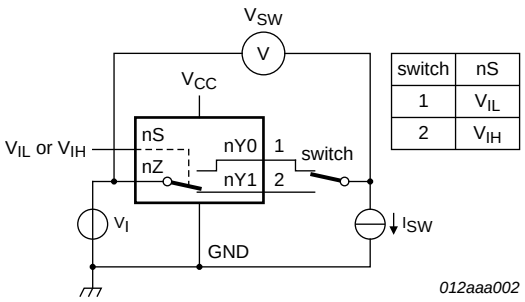
[2] Measured at identical V_{CC}, temperature and input voltage.

[3] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

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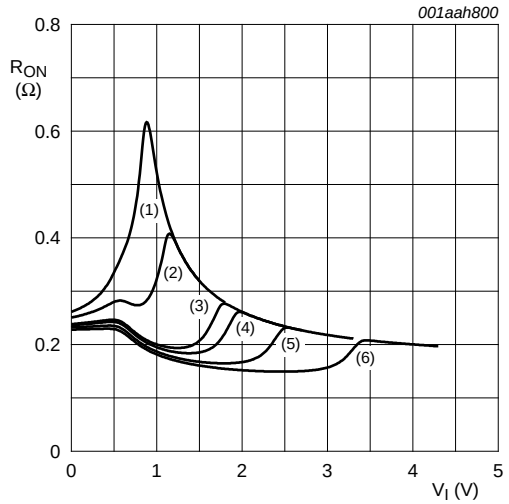
11.3 ON resistance test circuit and graphs



switch	nS
1	V_{IL}
2	V_{IH}

$R_{ON} = V_{SW} / I_{SW}$.

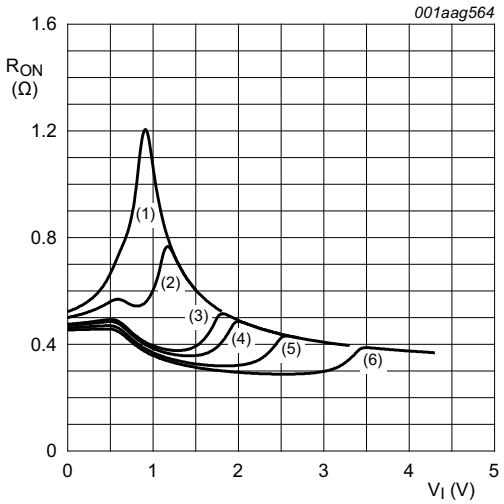
Fig 7. Test circuit for measuring ON resistance



(1) V_{CC} = 1.5 V.
(2) V_{CC} = 1.8 V.
(3) V_{CC} = 2.5 V.
(4) V_{CC} = 2.7 V.
(5) V_{CC} = 3.3 V.
(6) V_{CC} = 4.3 V.

Measured at T_{amb} = 25 °C.

Fig 8. Typical ON resistance as a function of input voltage (nY0 port)



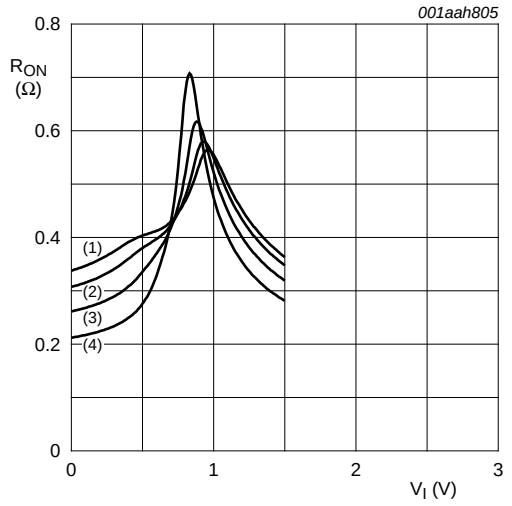
(1) V_{CC} = 1.5 V.
(2) V_{CC} = 1.8 V.
(3) V_{CC} = 2.5 V.
(4) V_{CC} = 2.7 V.
(5) V_{CC} = 3.3 V.
(6) V_{CC} = 4.3 V.

Measured at T_{amb} = 25 °C.

Fig 9. Typical ON resistance as a function of input voltage (nY1 port)

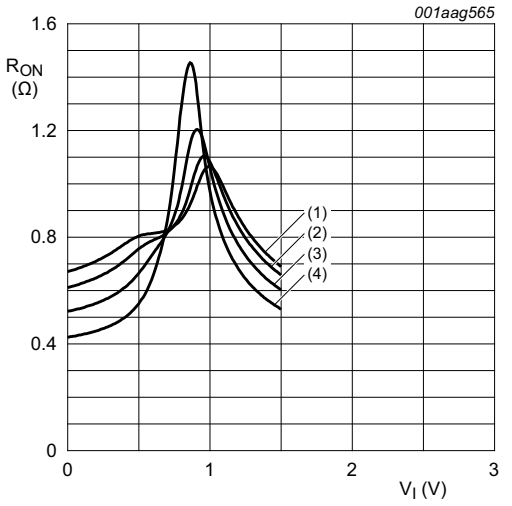
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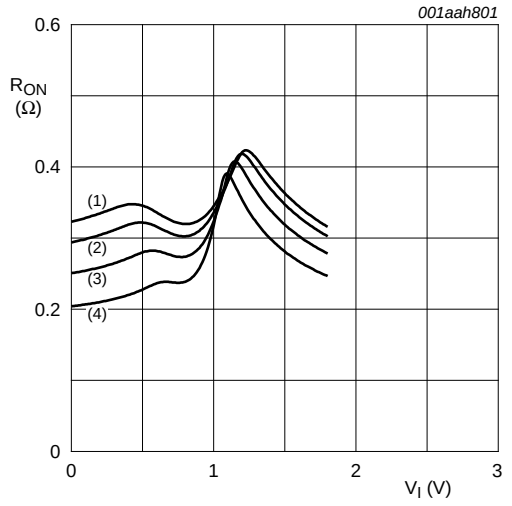
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 10. ON resistance as a function of input voltage; V_{CC} = 1.5 V (nY0 port)



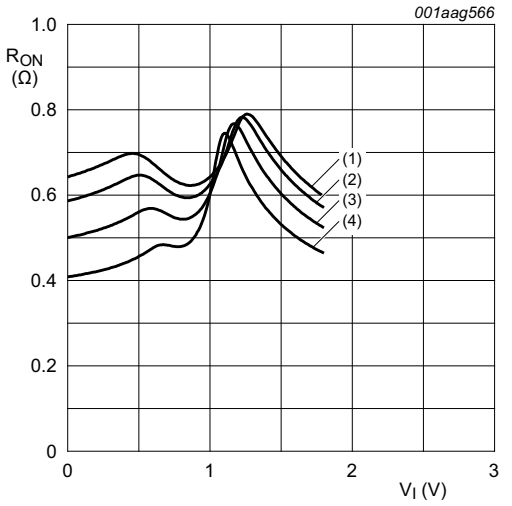
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 11. ON resistance as a function of input voltage; V_{CC} = 1.5 V (nY1 port)



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 12. ON resistance as a function of input voltage; V_{CC} = 1.8 V (nY0 port)

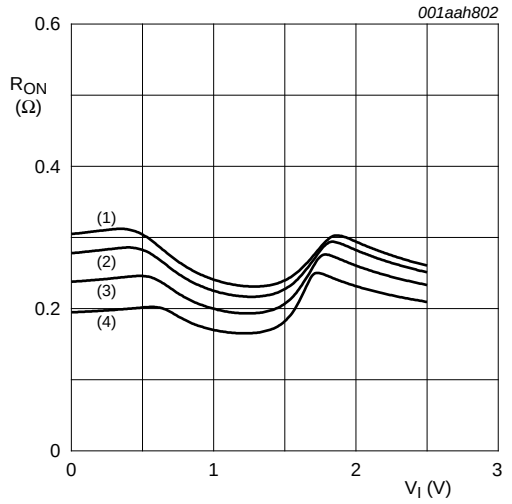


(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 13. ON resistance as a function of input voltage; V_{CC} = 1.8 V (nY1 port)

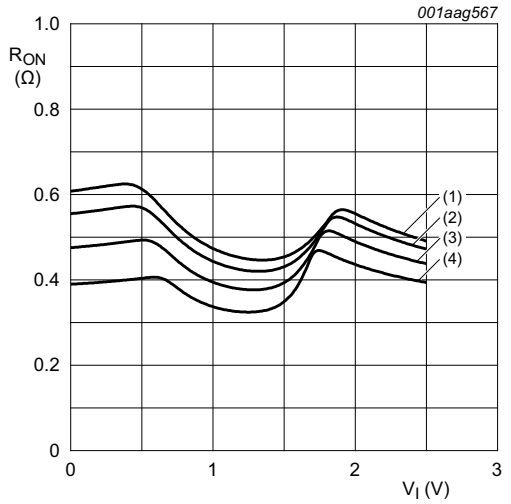
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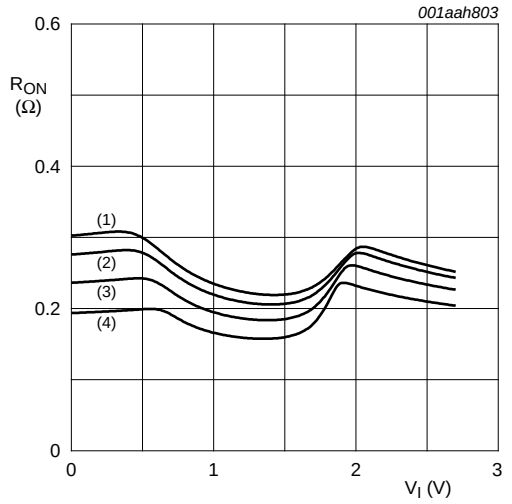
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 14. ON resistance as a function of input voltage; V_{CC} = 2.5 V (nY0 port)



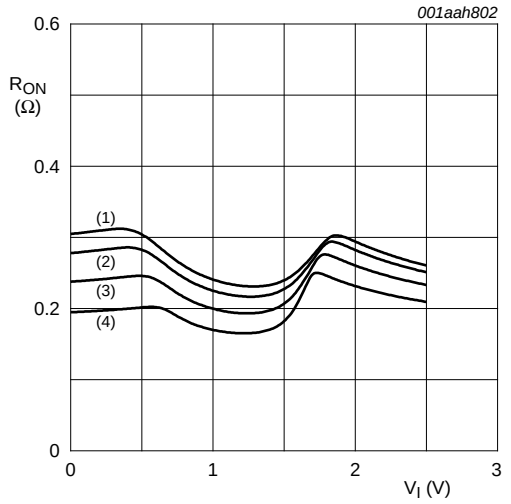
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 15. ON resistance as a function of input voltage; V_{CC} = 2.5 V (nY1 port)



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 16. ON resistance as a function of input voltage; V_{CC} = 2.7 V (nY0 port)

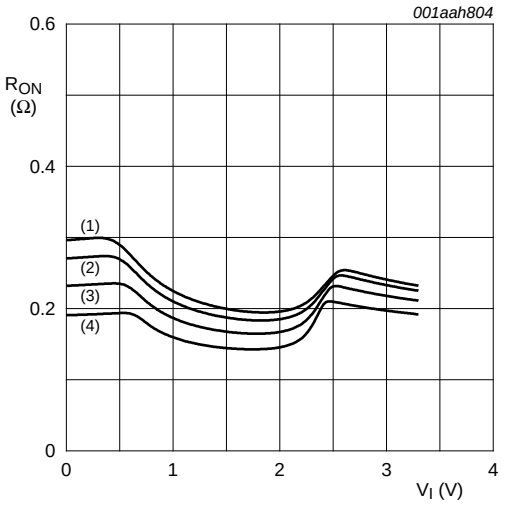


(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 17. ON resistance as a function of input voltage; V_{CC} = 2.7 V (nY1 port)

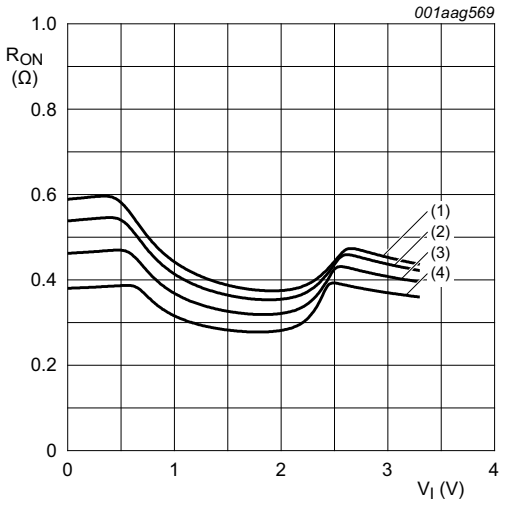
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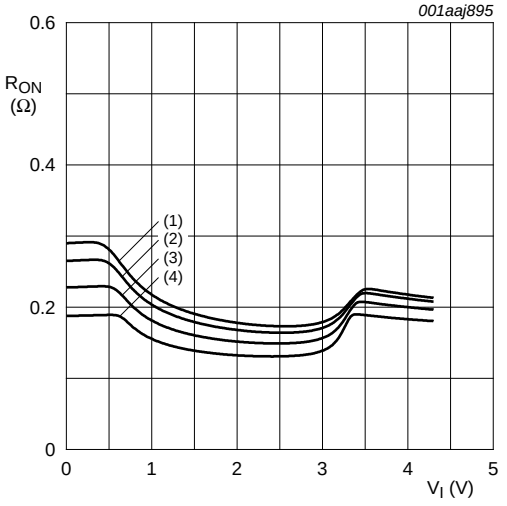
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 18. ON resistance as a function of input voltage; V_{CC} = 3.3 V (nY0 port)



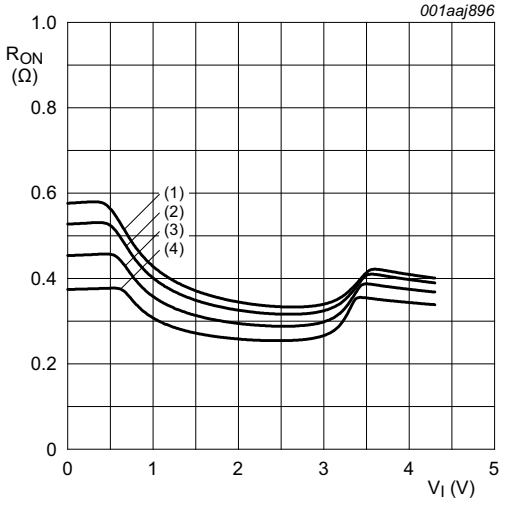
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 19. ON resistance as a function of input voltage; V_{CC} = 3.3 V (nY1 port)



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 20. ON resistance as a function of input voltage; V_{CC} = 4.3 V (nY0 port)



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 21. ON resistance as a function of input voltage; V_{CC} = 4.3 V (nY1 port)

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12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 24.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t_{en}	enable time	nS to nZ or nYn; see Figure 22							
		V_{CC} = 1.4 V to 1.6 V	-	50	100	-	130	130	ns
		V_{CC} = 1.65 V to 1.95 V	-	35	80	-	85	95	ns
		V_{CC} = 2.3 V to 2.7 V	-	24	50	-	55	60	ns
		V_{CC} = 2.7 V to 3.6 V	-	20	45	-	50	55	ns
		V_{CC} = 3.6 V to 4.3 V	-	20	45	-	50	55	ns
t_{dis}	disable time	nS to nZ or nYn; see Figure 22							
		V_{CC} = 1.4 V to 1.6 V	-	30	70	-	80	90	ns
		V_{CC} = 1.65 V to 1.95 V	-	18	55	-	60	65	ns
		V_{CC} = 2.3 V to 2.7 V	-	11	25	-	30	35	ns
		V_{CC} = 2.7 V to 3.6 V	-	9	20	-	25	30	ns
		V_{CC} = 3.6 V to 4.3 V	-	9	20	-	25	30	ns
t_{b-m}	break-before-make time	see Figure 23 [2]							
		V_{CC} = 1.4 V to 1.6 V	-	20	-	9	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	19	-	7	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	13	-	4	-	-	ns
		V_{CC} = 2.7 V to 3.6 V	-	10	-	2	-	-	ns
		V_{CC} = 3.6 V to 4.3 V	-	10	-	1	-	-	ns

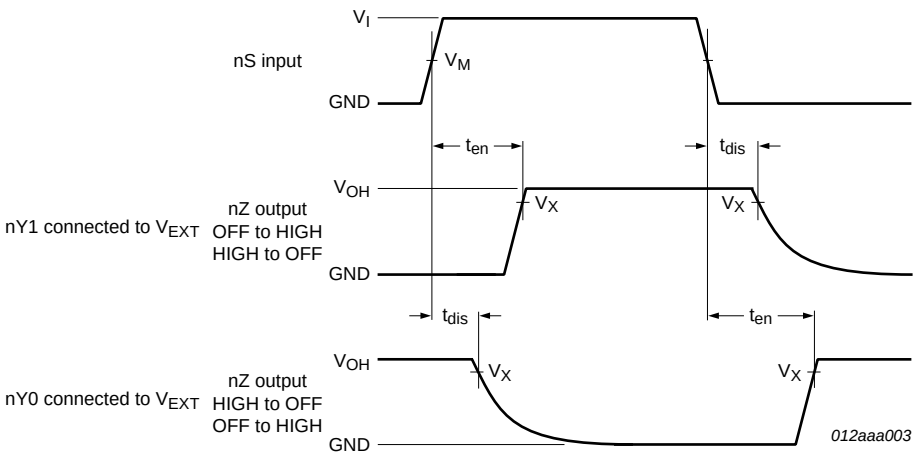
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V, 3.3 V and 4.3 V respectively.

[2] Break-before-make guaranteed by design.

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12.1 Waveform and test circuits



Measurement points are given in Table 10.

Logic level: V_{OH} is typical output voltage level that occurs with the output load.

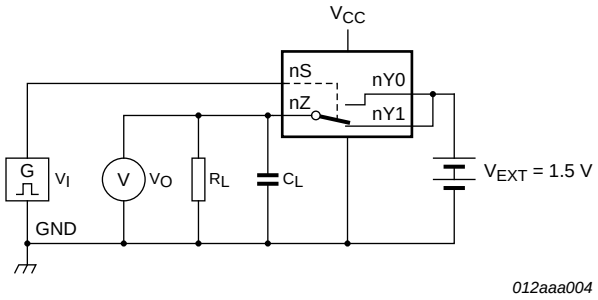
Fig 22. Enable and disable times

Table 10. Measurement points

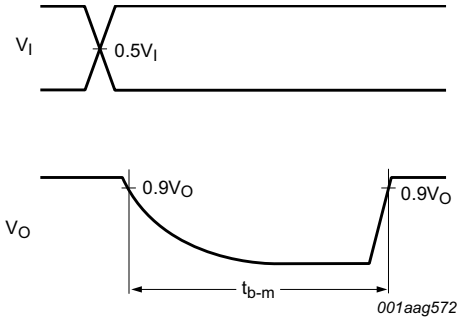
Supply voltage	Input	Output
V_{CC}	V_M	V_X
1.4 V to 4.3 V	$0.5V_{CC}$	$0.9V_{OH}$

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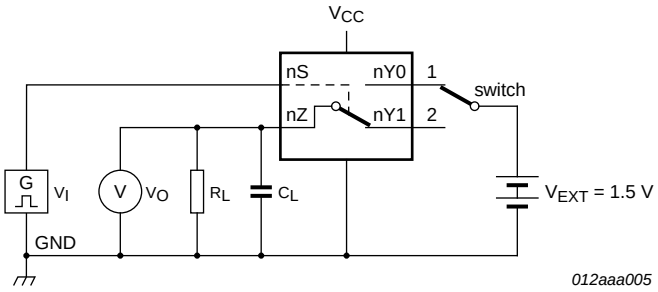


a. Test circuit.



b. Input and output measurement points

Fig 23. Test circuit for measuring break-before-make timing



Test data is given in Table 11.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 24. Load circuit for switching times

Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.4 V to 4.3 V	V_{CC}	≤ 2.5 ns	35 pF	50 Ω

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12.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.

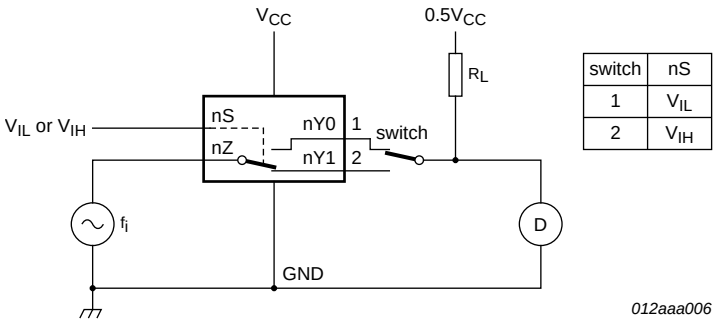
Symbol	Parameter	Conditions	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
THD	total harmonic distortion	f_i = 20 Hz to 20 kHz; R_L = 32 Ω; see Figure 25 [1]				
		V_{CC} = 1.4 V; V_I = 1 V (p-p)	-	0.06	-	%
		V_{CC} = 1.65 V; V_I = 1.2 V (p-p)	-	0.02	-	%
		V_{CC} = 2.3 V; V_I = 1.5 V (p-p)	-	0.02	-	%
		V_{CC} = 2.7 V; V_I = 2 V (p-p)	-	0.02	-	%
		V_{CC} = 4.3 V; V_I = 2 V (p-p)	-	0.02	-	%
		V_{CC} = 3.0 V; V_I = 1 V (p-p); R_L = 600 Ω	-	0.01	-	%
$f_{(-3dB)}$	−3 dB frequency response	R_L = 50 Ω; see Figure 26 [1]				
		port nY0; V_{CC} = 1.4 V to 4.3 V	-	15	-	MHz
		port nY1; V_{CC} = 1.4 V to 4.3 V	-	20	-	MHz
α_{iso}	isolation (OFF-state)	f_i = 100 kHz; R_L = 50 Ω; see Figure 27 [1]				
		V_{CC} = 1.4 V to 4.3 V	-	−90	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; f_i = 1 MHz; C_L = 50 pF; R_L = 50 Ω; see Figure 28				
		V_{CC} = 1.4 V to 3.6 V	-	0.5	-	V
		V_{CC} = 3.6 V to 4.3 V	-	0.7	-	V
Xtalk	crosstalk	between switches; [1] f_i = 100 kHz; R_L = 50 Ω; see Figure 29				
		V_{CC} = 1.4 V to 4.3 V	-	−90	-	dB
Q_{inj}	charge injection	f_i = 1 MHz; C_L = 0.1 nF; R_L = 1 MΩ; V_{gen} = 0 V; R_{gen} = 0 Ω; see Figure 30				
		V_{CC} = 1.5 V	-	10	-	pC
		V_{CC} = 1.8 V	-	14	-	pC
		V_{CC} = 2.5 V	-	21	-	pC
		V_{CC} = 3.3 V	-	30	-	pC
		V_{CC} = 4.3 V	-	50	-	pC

[1] f_i is biased at $0.5V_{CC}$.

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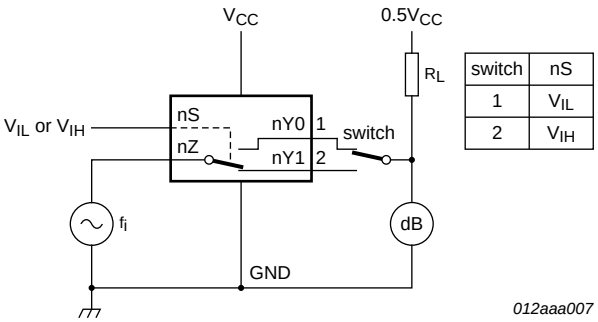
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12.3 Test circuits



switch	nS
1	V_{IL}
2	V_{IH}

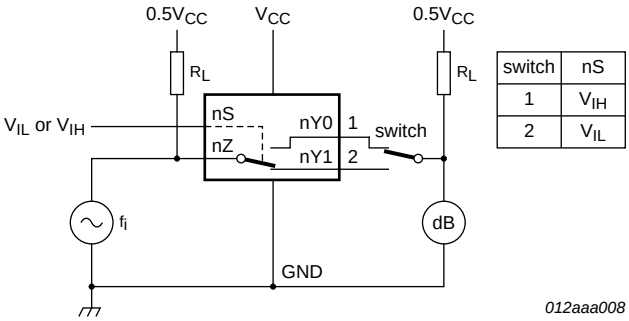
Fig 25. Test circuit for measuring total harmonic distortion



switch	nS
1	V_{IL}
2	V_{IH}

Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads −3 dB.

Fig 26. Test circuit for measuring the frequency response when channel is in ON-state



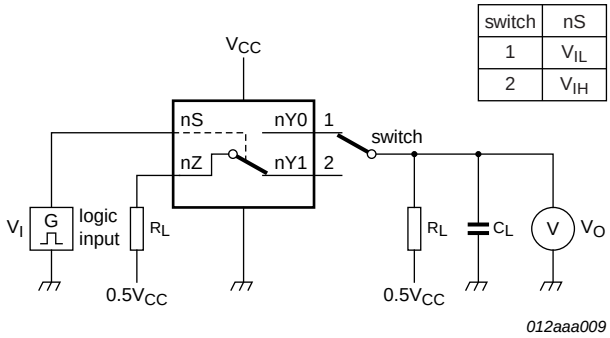
switch	nS
1	V_{IH}
2	V_{IL}

Adjust f_i voltage to obtain 0 dBm level at input.

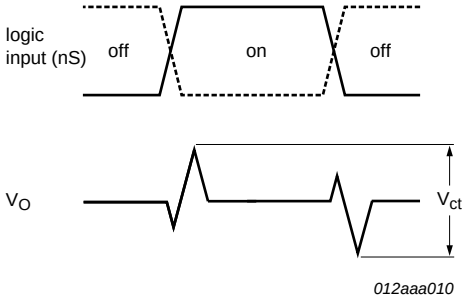
Fig 27. Test circuit for measuring isolation (OFF-state)

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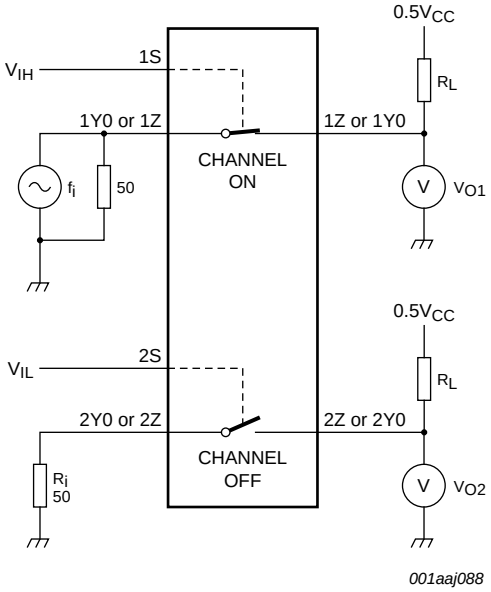


a. Test circuit



b. Input and output pulse definitions

Fig 28. Test circuit for measuring crosstalk voltage between digital inputs and switch

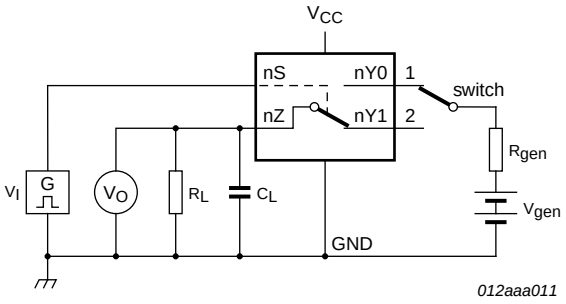


$20 \log_{10} (V_{O2} / V_{O1})$ or $20 \log_{10} (V_{O1} / V_{O2})$.

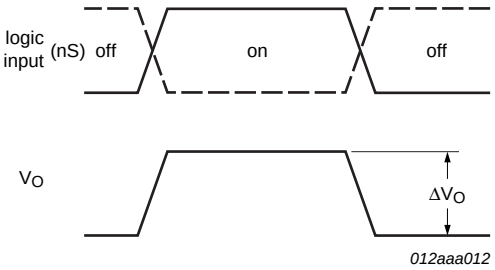
Fig 29. Test circuit for measuring crosstalk between switches

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a. Test circuit.



b. Input and output pulse definitions

Definition: $Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

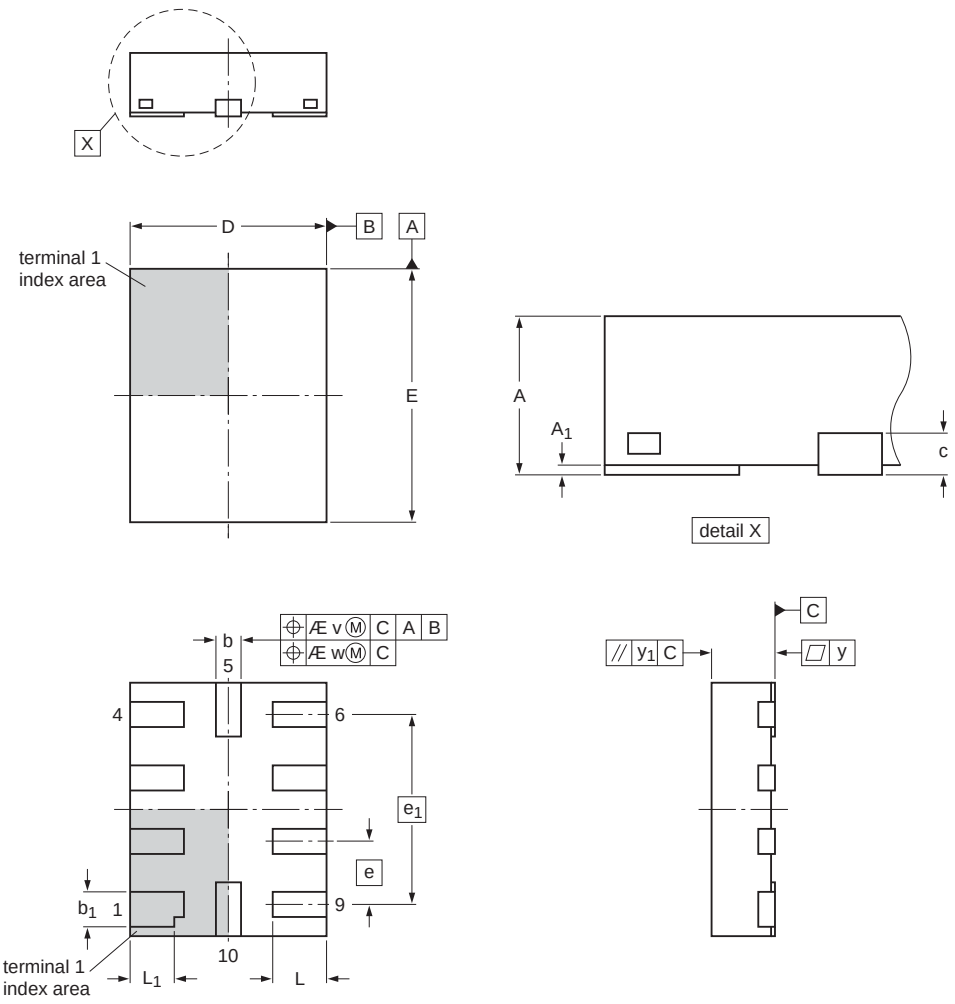
Fig 30. Test circuit for measuring charge injection

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13. Package outline

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.55 x 2.00 x 0.50 mm **SOT1049-3**



Dimensions

Unit(1)		A	A1	b	b1	c	D	E	e	e1	L	L1	v	w	y	y1
mm	max	0.5	0.05	0.25	0.33		1.65	2.1			0.48	0.40				
	nom			0.20	0.28	0.127	1.55	2.0	0.5	1.5	0.43	0.35	0.1	0.05	0.05	0.05
	min		0.00	0.15	0.23		1.45	1.9			0.38	0.30				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1049-3_po

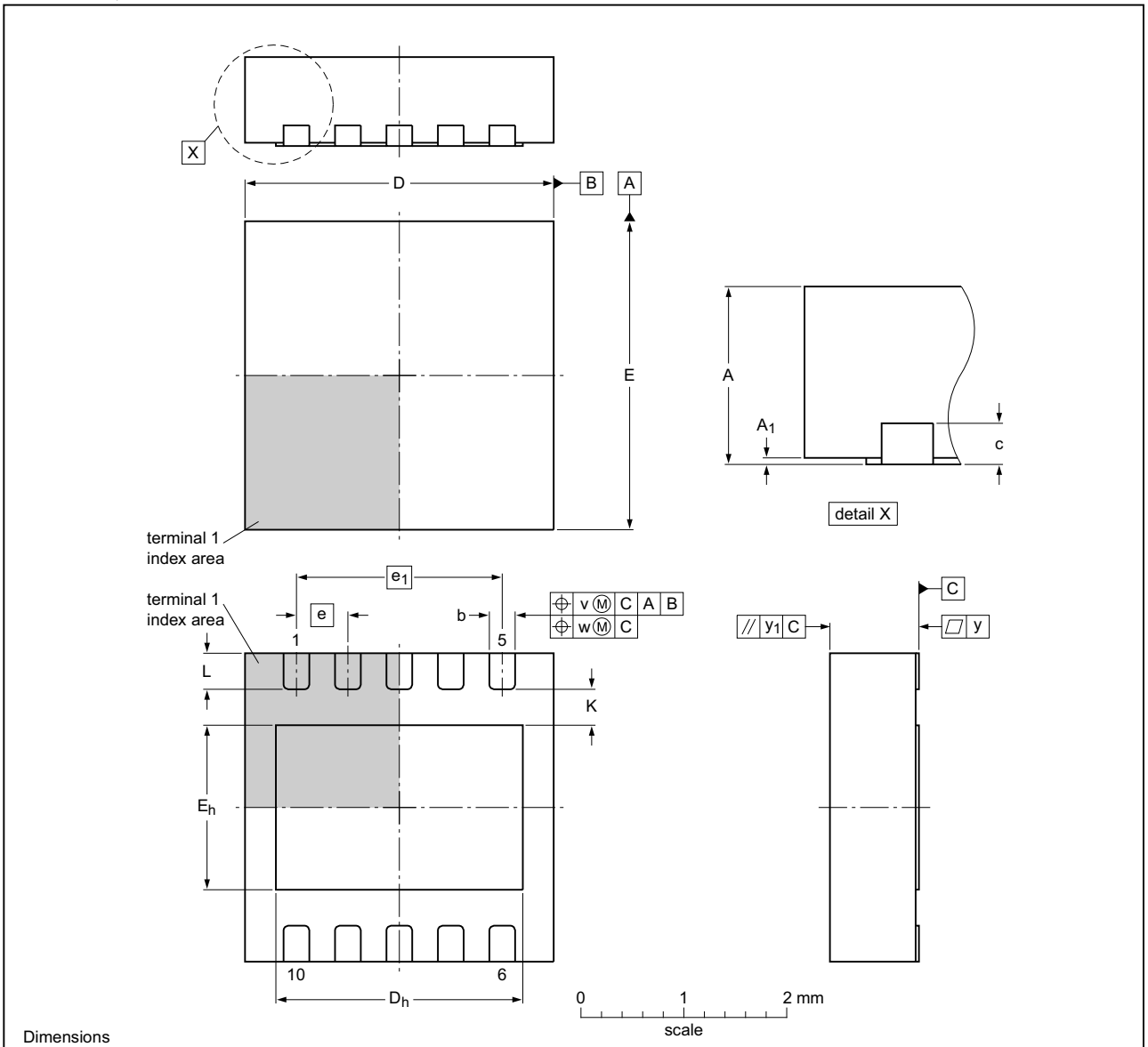
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1049-3	- - -	MO255	- - -			~~10-12-06~~ 11-03-30

Fig 31. Package outline SOT1049-3 (XQFN10)

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HVSON10: plastic thermal enhanced very thin small outline package; no leads; 10 terminals; 3 x 3 x 0.85 mm **SOT650-2**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	K	L	v	w	y	y_1
	max	1.00	0.05	0.30		3.1	2.5	3.1	1.7			0.41	0.45				
mm	nom	0.85	0.03	0.25	0.2	3.0	2.4	3.0	1.6	0.5	2	0.35	0.35	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.18		2.9	2.3	2.9	1.5			0.28	0.30				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot650-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT650-2	- - -	MO-229	- - -			~~09-03-16~~ 09-03-18

Fig 32. Package outline SOT650-2 (HVSON10)

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14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PDA	Personal Digital Assistant

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3L4684 v.8	20140403	Product data sheet	-	NX3L4684 v.7
Modifications:	• Package outline drawing SOT650-1 changed to SOT650-2 (Figure 32).			
NX3L4684 v.7	20120618	Product data sheet	-	NX3L4684 v.6
NX3L4684 v.6	20111104	Product data sheet	-	NX3L4684 v.5
NX3L4684 v.5	20110107	Product data sheet	-	NX3L4684 v.4
NX3L4684 v.4	20100324	Product data sheet	-	NX3L4684 v.3
NX3L4684 v.3	20100209	Product data sheet	-	NX3L4684 v.2
NX3L4684 v.2	20090401	Product data sheet	-	NX3L4684 v.1
NX3L4684 v.1	20081127	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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18. Contents

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