High Efficiency, Main Power Supply Controller for Notebook Computers

General Description

The RT8223A/B dual step-down, switch-mode power-supply controller generates logic-supply voltages in battery-powered systems. The RT8223A/B includes two pulse-width modulation (PWM) controllers fixed at 5V/ 3.3V or adjustable from 2V to 5.5V. This device also features 2 linear regulators providing fixed 5V and 3.3V outputs. The linear regulator each provides up to 70mA output current with automatic linear-regulator bootstrapping to the PWM outputs. The RT8223A/B includes on-board power-up sequencing, the power good output, internal soft-start, and internal soft-discharge output that prevents negative voltages on shutdown.

A constant on-time PWM control scheme operates without sense resistor and provides 100ns response to load transients while maintaining a relatively constant switching frequency. The unique ultrasonic mode maintains the switching frequency above 25kHz, which eliminates noise in audio applications. Other features include diode-emulation mode (DEM), which maximizes efficiency in light-load applications, and fixed-frequency PWM mode, which reduces RF interference in sensitive application

Ordering Information

RT8223□□□

- Package Type
  QW : WQFN-24L 4x4 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)
- Pin Function
  A : Default
  B : With ENC

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Wide Input Voltage Range 6V to 25V**
- **Dual Fixed 5V/3.3V Outputs or Adjustable from 2V to 5.5V, 1.5% Accuracy**
- **Fixed 3.3V and 5V LDO Output : 70mA**
- **2V Reference Voltage ±1% : 50μA**
- **Constant ON-Time Control with 100ns Load Step Response**
- **Frequency Selectable via TONSEL Setting**
- **$R_{DS(ON)}$ Current Sensing and Programmable Current Limit combined with Enable Control**
- **Selectable PWM, DEM, or Ultrasonic Mode**
- **Internal Soft-Start and Soft-Discharge**
- **High Efficiency up to 97%**
- **5mW Quiescent Power Dissipation**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

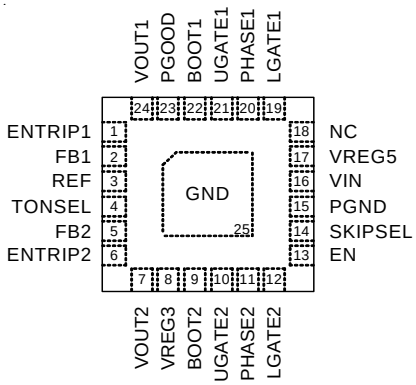
- Notebook and Sub-Notebook Computers
- 3-Cell and 4-Cell Li+ Battery-Powered Devices

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

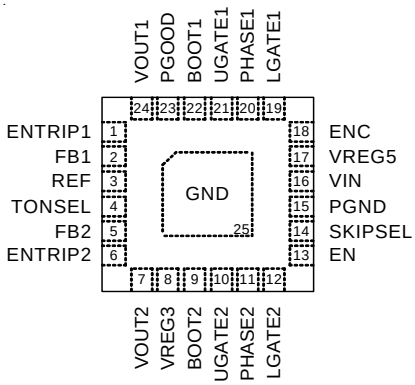
Pin Configurations

(TOP VIEW)



RT8223A

WQFN-24L 4x4

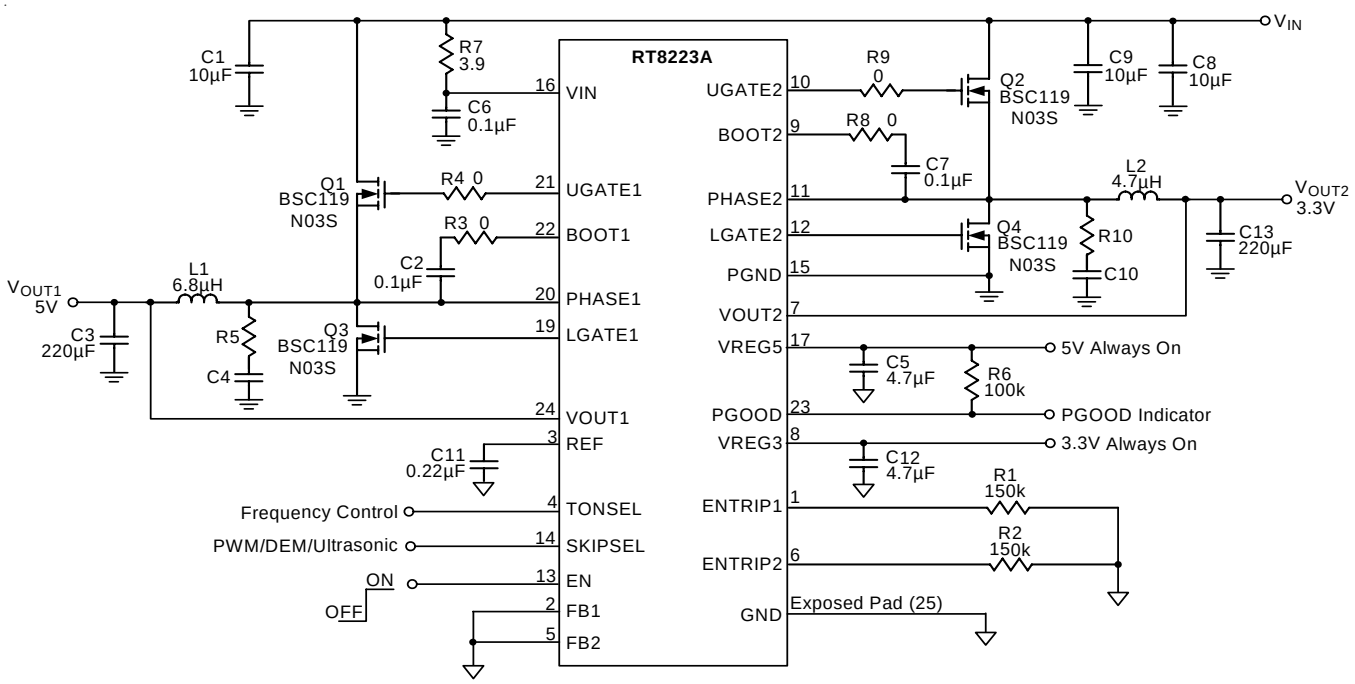


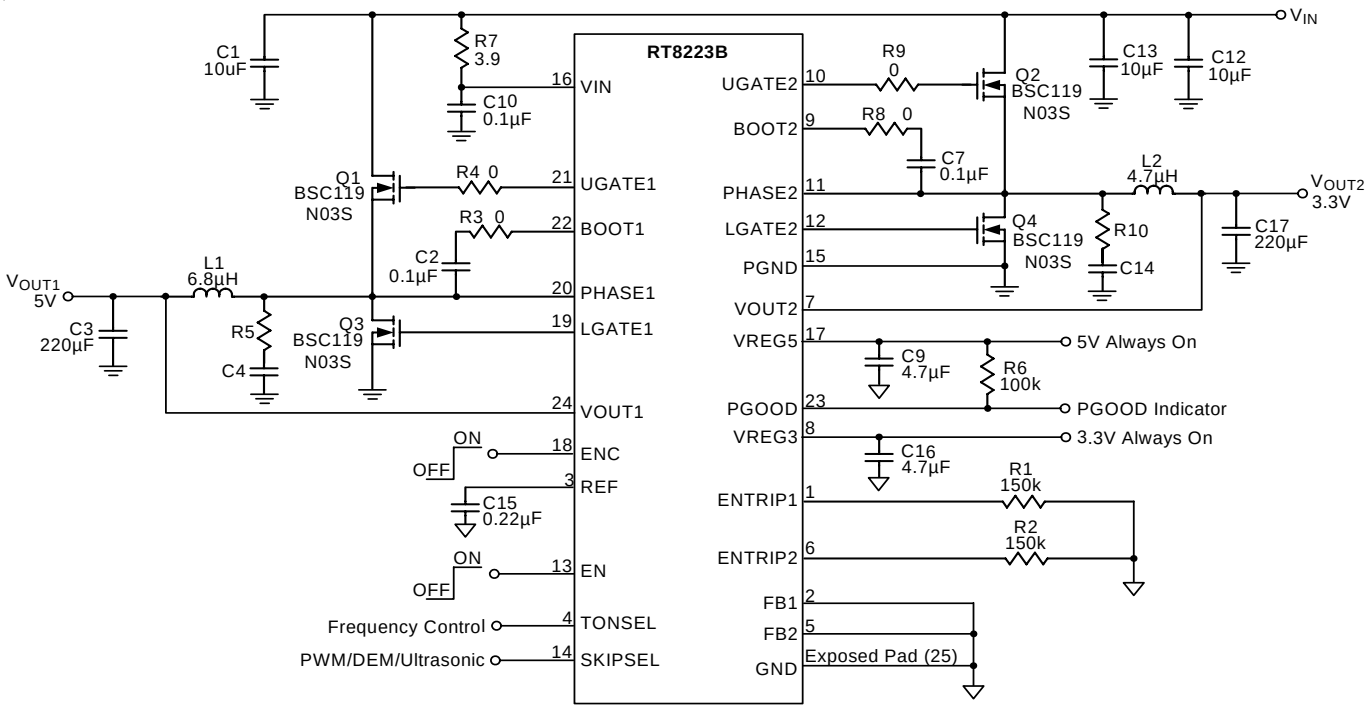
RT8223B

WQFN-24L 4x4

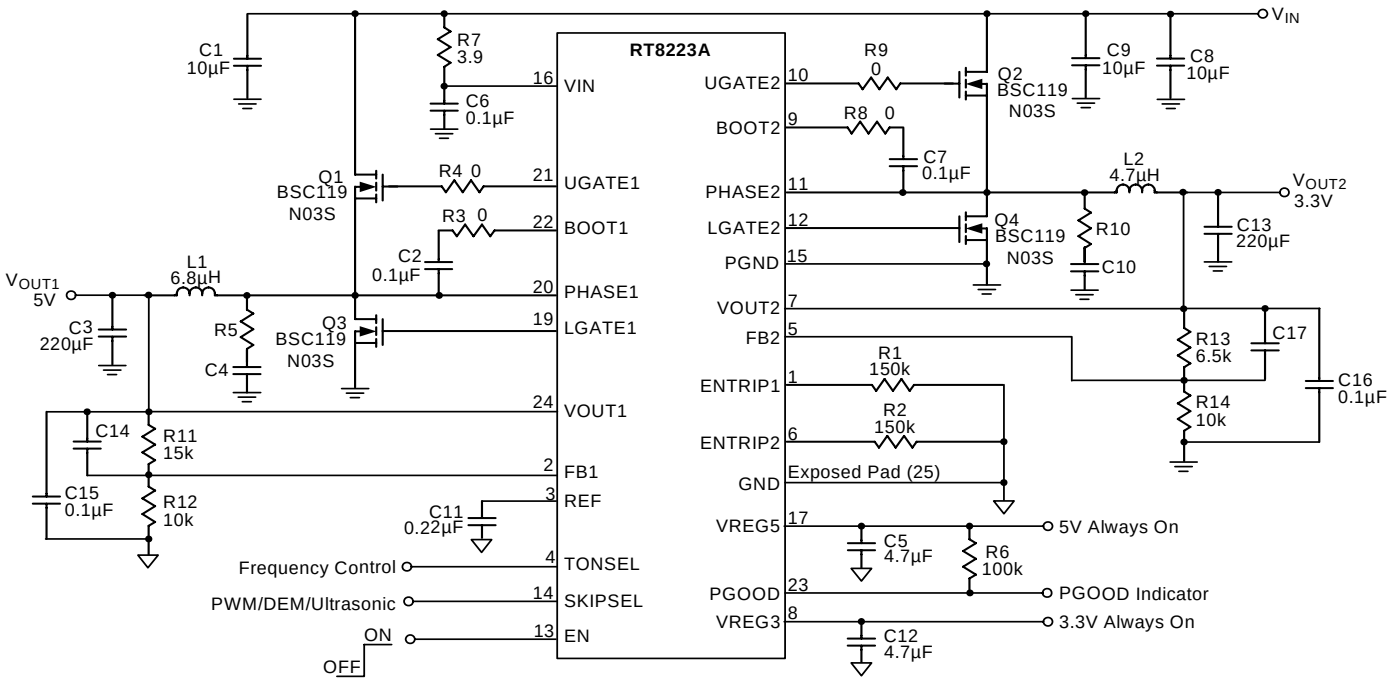
Typical Application Circuit

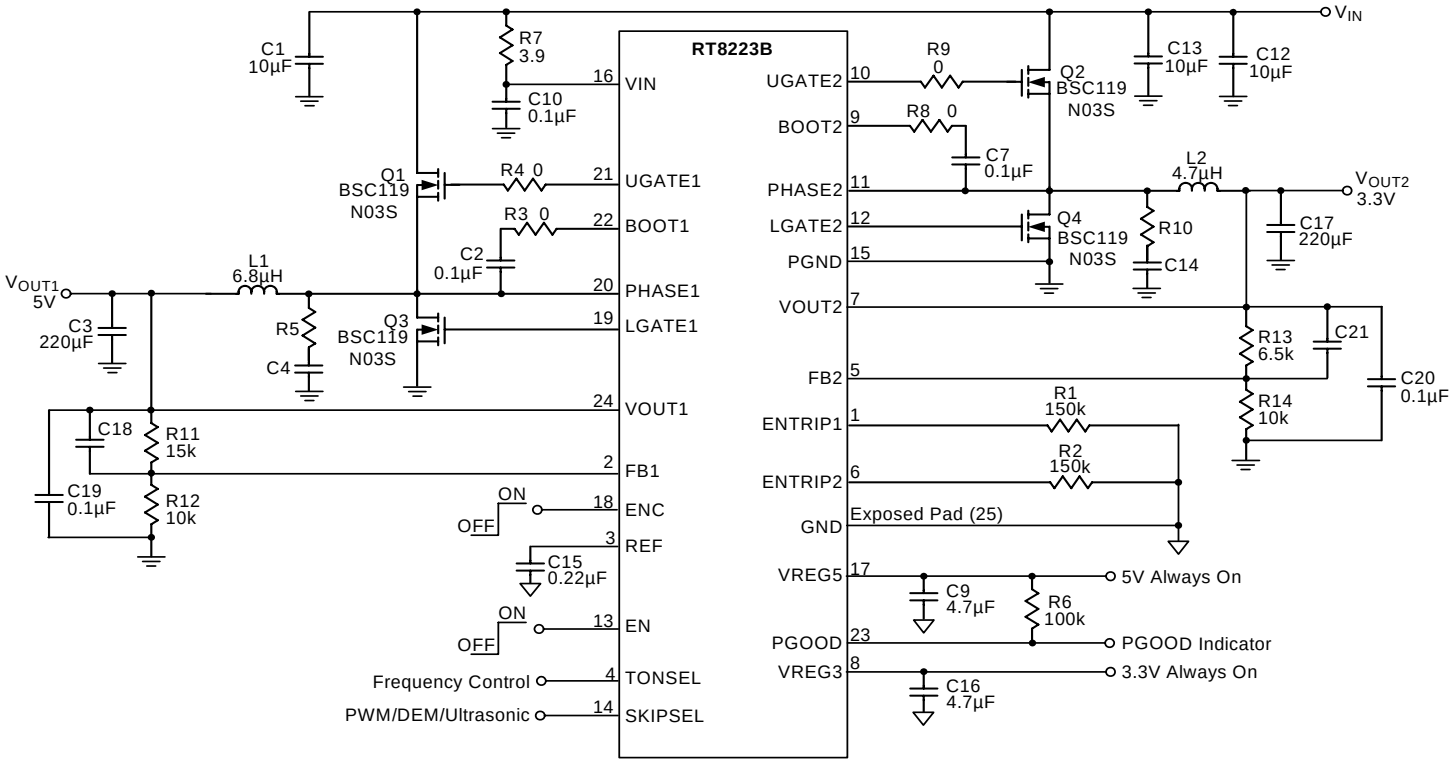
For Fixed Voltage Regulator



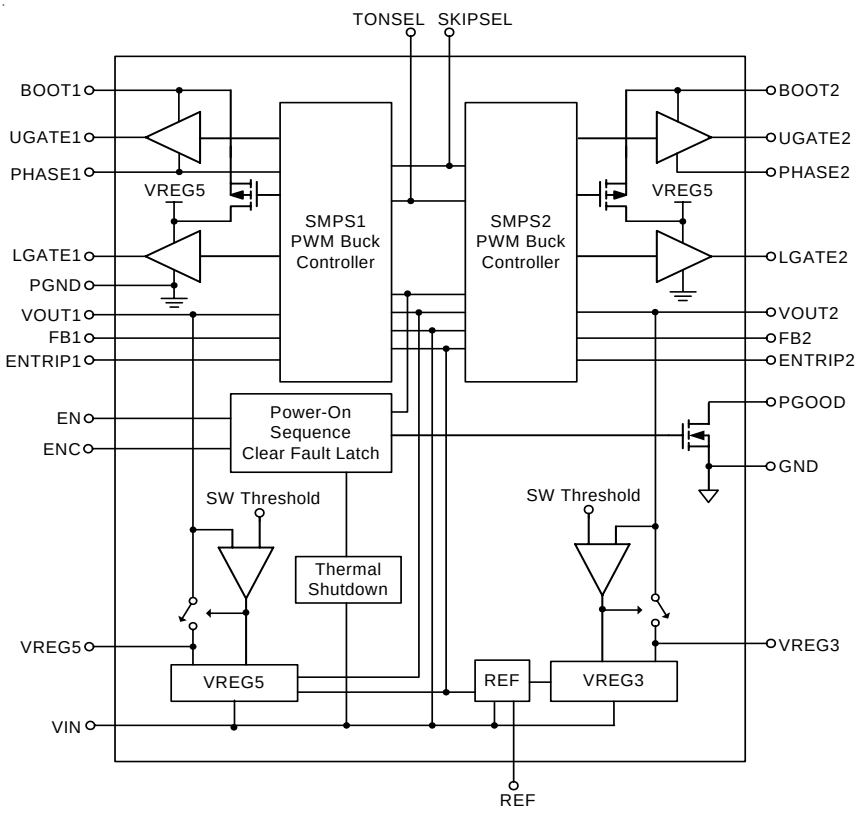

RT8223B
VIN
UGATE1
BOOT1
PHASE1
LGATE1
VOUT1
ENC
REF
EN
TONSEL
SKIPSEL
UGATE2
BOOT2
PHASE2
LGATE2
PGND
VOUT2
VREG5
PGOOD
VREG3
ENTRIP1
ENTRIP2
FB1
FB2
GND
Exposed Pad (25)
C1 10uF
R7 3.9
C10 0.1µF
Q1 BSC119 N03S
R4 0
R3 0
C2 0.1µF
L1 6.8µH
C3 220µF
R5
C4
Q3 BSC119 N03S
ON
OFF
C15 0.22µF
Frequency Control
PWM/DEM/Ultrasonic
R9 0
R8 0
C7 0.1µF
Q2 BSC119 N03S
Q4 BSC119 N03S
C13 10µF
C12 10µF
L2 4.7µH
R10
C14
C17 220µF
C9 4.7µF
R6 100k
C16 4.7µF
R1 150k
R2 150k
5V Always On
PGOOD Indicator
3.3V Always On
VIN
VOUT1 5V
VOUT2 3.3V

For Adjustable Voltage Regulator

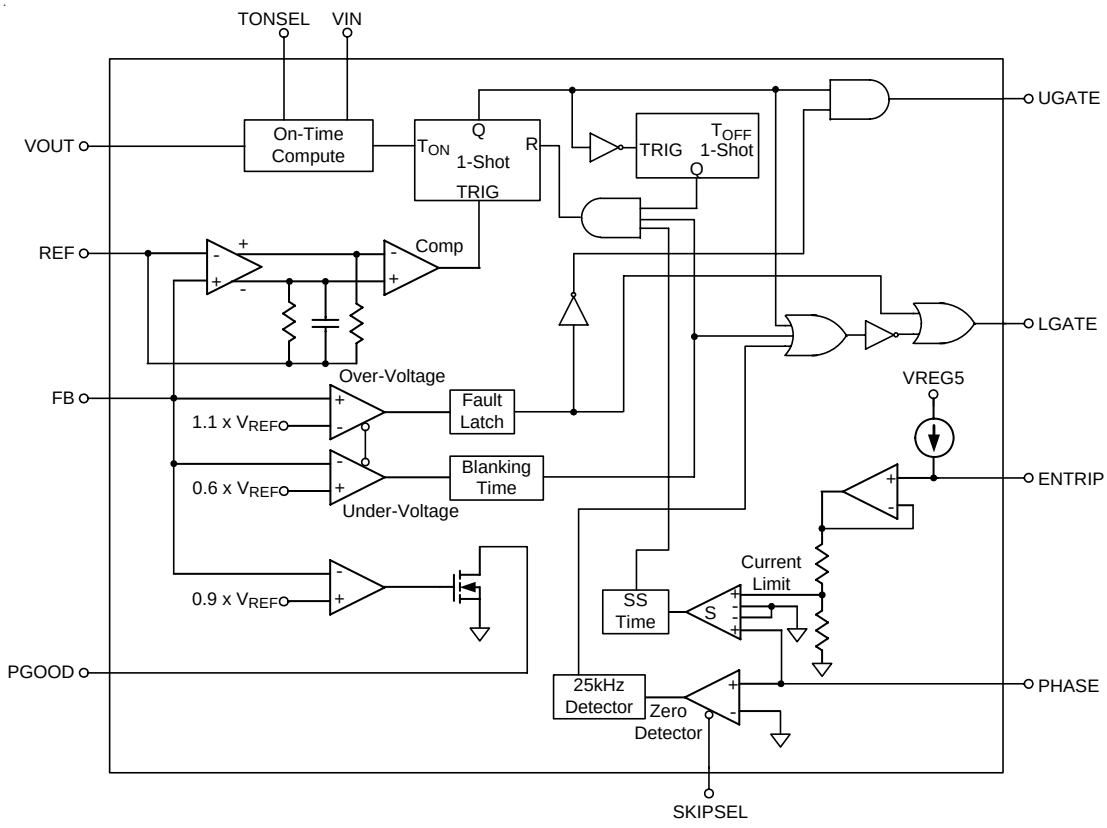




Function Block Diagram



Function Block Diagram



PWM Controller (One Side)

Functional Pin Description

ENTRIP1 (Pin 1)

Channel 1 enable and Current Limit setting Input. Connect a resistor to GND to set the threshold for channel 1 synchronous $R_{DS(ON)}$ sense. The GND – PHASE1 current-limit threshold is 1/10th the voltage seen at ENTRIP1 over a 0.5V to 2V range. There is an internal 10μA current source from VREG5 to ENTRIP1.

FB1 (Pin 2)

SMPS1 Feedback Input. Connect FB1 to VREG5 or GND for fixed 5V operation. Or connect FB1 to a resistive voltage-divider from VOUT1 to GND to adjust output from 2V to 5.5V.

REF (Pin 3)

2V Reference Output. Bypass to GND with a 0.22μF capacitor. REF can source up to 50μA for external loads. Loading REF degrades FBx and output accuracy according to the REF load regulation error.

TONSEL (Pin 4)

Frequency Selectable Input for VOUT1/VOUT2 respectively.

400kHz/500kHz : Connect to VREG5 or VREG3

300kHz/375kHz : Connect to REF

200kHz/250kHz : Connect to GND

FB2 (Pin 5)

SMPS2 Feedback Input. Connect FB2 to VREG5 or GND for fixed 3.3V operation. Or connect FB2 to a resistive voltage-divider from VOUT2 to GND to adjust output from 2V to 5.5V.

ENTRIP2 (Pin 6)

Channel 2 enable and Current Limit setting Input. Connect a resistor to GND to set the threshold for channel 2 synchronous $R_{DS(ON)}$ sense. The GND – PHASE2 current limit threshold is 1/10th the voltage seen at ENTRIP2 over a 0.5V to 2V range. There is an internal 10μA current source from VREG5 to ENTRIP2.

VOUT2 (Pin 7)

SMPS2 Output Voltage Sense Input. Connect to the SMPS2 output. VOUT2 is an input to the on-time one shot circuit. It also serves as the SMPS2 feedback input in fixed voltage mode.

VREG3 (Pin 8)

3.3V Linear Regulator Output.

BOOT2 (Pin 9)

Boost Flying Capacitor Connection for SMPS2. Connect to an external capacitor according to the typical application circuits.

UGATE2 (Pin 10)

High-Side MOSFET Floating Gate Driver Output for SMPS2. UGATE2 swings between PHASE2 and BOOT2.

PHASE2 (Pin 11)

Inductor Connection for SMPS2. PHASE2 is the internal lower supply rail for the UGATE2 high side gate driver. PHASE2 is also the current-sense input for the SMPS2.

LGATE2 (Pin 12)

SMPS2 Synchronous-Rectifier Gate-Drive Output. LGATE2 swings between PGND and VREG5.

EN (Pin 13)

Master Enable Input. The REF/VREG5/VREG3 are enabled if it is within logic high level and disabled if it is less than the logic low level.

SKIPSEL (Pin 14)

Operation Mode Selectable Input.

Ultrasonic Mode : Connect to VREG5 or VREG3

Diode Emulation Mode : Connect to GND

PWM Mode : Connect to REF

GND [Exposed Pad (25)]

Analog Ground for SMPS controller. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

PGND (Pin 15)

Power Ground for SMPS controller. Connect PGND externally to the underside of the exposed pad.

VIN (Pin 16)

High Voltage Power Supply Input for 5V/3.3V LDO and Feed-forward ON-Time circuitry.

VREG5 (Pin 17)

5V Linear Regulator Output.VREG5 is also the supply voltage for the low-side MOSFET driver and analog supply voltage for the device.

NC (Pin 18) (RT8223A)

No Internal Connection.

ENC (Pin 18) (RT8223B)

SMPSx Enable Input. Pull up to VREG3 or VREG5 to turn on both switcher channels. Short to GND to shutdown them.

LGATE1 (Pin 19)

SMPS1 Synchronous Rectifier Gate Drive Output. LGATE1 swings between PGND and VREG5.

PHASE1 (Pin 20)

Inductor Connection for SMPS1. PHASE1 is the internal lower supply rail for the UGATE1 high side gate driver. PHASE1 is also the current sense input for the SMPS1.

UGATE1 (Pin 21)

High-Side MOSFET Floating Gate Driver Output for SMPS1. UGATE1 swings between PHASE1 and BOOT1.

BOOT1 (Pin 22)

Boost Flying Capacitor Connection for SMPS1. Connect to an external capacitor according to the typical application circuits.

PGOOD (Pin 23)

Power Good Output for channel 1 and channel 2. (Logical AND)

VOUT1 (Pin 24)

SMPS1 Output Voltage-Sense Input. Connect to the SMPS1 output. VOUT1 is an input to the on-time one shot circuit. It also serves as the SMPS1 feedback input in fixed-voltage mode.

Absolute Maximum Ratings (Note 1)

- VIN, EN to GND ---------- –0.3V to 30V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - < 20ns ---------- –8V to 38V
- BOOTx to PHASEx ---------- –0.3V to 6V
- ENTRIPx, SKIPSEL, TONSEL, PGOOD, to GND ---------- –0.3V to 6V
- VREG5, VREG3, FBx, VOUTx, ENC, REF to GND ---------- –0.3V to 6V
- UGATEx to PHASEx
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-24L 4x4 ---------- 1.923W
- Package Thermal Resistance (Note 2)
  - WQFN-24L 4x4, θ_{JA} ---------- 52°C/W
  - WQFN-24L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 6V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 100°C

Electrical Characteristics

(V_{IN} = 12V, EN = ENC = 5V, ENTRIP1 = ENTRIP2 = 2V, No Load on VREG5, VREG3, VOUT1, VOUT2 and REF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Supply							
VIN Standby Supply Current	I_{VIN_SBY}	V_{IN} = 6V to 25V, Both SMPS Off, EN = 5V, ENC = GND		--	200	--	μA
VIN Shutdown Supply Current	I_{VIN_SHDH}	V_{IN} = 6V to 25V, ENTRIPx = EN = GND		--	20	40	μA
Quiescent Power Consumption		Both SMPSs On, FBx = SKIPSEL = REF V_{OUT1} = 5.3V, V_{OUT2} = 3.5V (Note 5)		--	5	7	mW
SMPS Output and FB Voltage							
VOUT1 Output Voltage in Fixed Mode	V_{OUT1}	V_{IN} = 6V to 25V, FB1= REF or 5V, SKIPSEL = REF		4.975	5.05	5.125	V
VOUT2 Output Voltage in Fixed Mode	V_{OUT2}	V_{IN} = 6V to 25V, FB2 = REF or 5V, SKIPSEL = REF		3.285	3.33	3.375	V
FBx in Output Adjustable Mode	FBx	V_{IN} = 6V to 25V		1.975	2	2.025	V
Output Voltage Adjustment Range	V_{OUTx}	SMPS1, SMPS2		2	--	5.5	V
FBx Adjustable-mode Threshold Voltage		Fixed or Adj-Mode comparator threshold		0.2	0.4	0.55	V
DC Load Regulation	V_{LOAD}	Either SMPS, SKIPSEL = REF, 0 to 5A		--	–0.1	--	%
		Either SMPS, SKIPSEL = VREG5, 0 to 5A		--	–1.7	--	
		Either SMPS, SKIPSEL = GND, 0 to 5A		--	–1.5	--	
Line Regulation	V_{LINE}	Either SMPS, V_{IN} = 6V to 25V		--	0.005	--	%/V
On Time							
On-Time Pulse Width	t_{UGATEx}	TONSEL = GND	V_{OUT1} = 5.05V	1895	2105	2315	ns
			V_{OUT2} = 3.33V	999	1110	1221	
		TONSEL = REF	V_{OUT1} = 5.05V	1227	1403	1579	
			V_{OUT2} = 3.33V	647	740	833	
		TONSEL = VREG5	V_{OUT1} = 5.05V	895	1052	1209	
			V_{OUT2} = 3.33V	475	555	635	
Minimum Off-Time	t_{LGATEx}			200	300	400	ns
Ultrasonic Mode Frequency		SKIPSEL = VREG5 or VREG3		20	28	--	kHz
Soft Start							
Soft-Start Time	t_{SSx}	Zero to Full Limit from ENTRIPx Enable		--	2	--	ms
Current Sense							
Current Limit Threshold (Default)		$V_{ENTRIPx}$ = VREG5, GND–PHASEx		180	200	220	mV
ENTRIPx Source Current	$I_{ENTRIPx}$	$V_{ENTRIPx}$ = 0.9V		9.4	10	10.6	μA
ENTRIPx Current Temperature Coefficient	$TC_{IENTRIPx}$			--	1600	--	PPM/°C
ENTRIPx Adjustment Range		$V_{ENTRIPx} = I_{ENTRIPx} \times R_{ENTRIPx}$		0.5	--	2	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit Threshold		GND–PHASEx, $V_{ENTRIPx}$ =2V	180	200	220	mV
Zero-Current Threshold		SKIPSEL = VREG5 or GND, GND–PHASEx	--	3	--	mV
Internal Regulator and Reference						
VREG5 Output Voltage	V_{VREG5}	V_{OUT1} = GND, 6V < V_{IN} < 25V, 0 < I_{VREG5} < 70mA	4.8	5	5.2	V
VREG3 Output Voltage	V_{VREG3}	V_{OUT2} = GND, 6V < V_{IN} < 25V, 0 < I_{VREG3} < 70mA	3.2	3.33	3.46	V
VREG5 Short Current	I_{VREG5}	VREG5 = GND, V_{OUT1} = GND	--	175	275	mA
VREG3 Short Current	I_{VREG3}	VREG3 = GND, V_{OUT2} = GND	--	175	275	mA
VREG5 Switchover Threshold to V_{OUT1}		Rising Edge at V_{OUT1} Regulation Point	4.53	4.66	4.79	V
VREG3 Switchover Threshold	V_{SW3}	Rising Edge at V_{OUT2} Regulation Point, Hysteresis = 6%	2.98	3.08	3.18	V
VREGx Switchover Equivalent Resistance	R_{SW}	VREGx to V_{OUTx}, 10mA	--	1.5	3	Ω
REF Output Voltage	V_{REF}	No External Load	1.98	2	2.02	V
REF Load Regulation		0 < I_{LOAD} < 50uA	--	10	--	mV
REF Sink Current		REF in Regulation	5	--	--	μA
UVLO						
VREG3 UVLO Threshold		SMPSx off	--	2.5	--	V
VREG5 UVLO Threshold		Rising Edge	--	4.35	4.5	V
		Falling Edge	3.9	4.05	4.25	V
Power Good						
PGOOD Threshold	V_{PGOODx}	PGOOD Detect (FBx Rising Edge)	–11	–7.5	–4	%
		Hysteresis	--	8	--	
PGOOD Propagation Delay		Falling Edge, 50mV Overdrive	--	10	--	μs
PGOOD Leakage Current		High State, Forced to 5.5V	--	--	1	μA
PGOOD Output Low Voltage		I_{SINK} = 4mA	--	--	0.3	V
Fault Detection						
OVP Trip Threshold	V_{FB_OVP}	FBx with Respect to Internal Reference	108	111	115	%
OVP Propagation Delay			--	10	--	μs
UVP Trip Threshold	V_{UV}	UVP Detect (FBx Falling Edge)	46	52	58	%
		Hysteresis	--	8	--	
UVP Shutdown Blanking Time	t_{SHDN_UVP}	From ENTRIPx Enable	--	3	--	ms
Thermal Shutdown						
Thermal Shutdown	T_{SHDN}		--	150	--	°C
Thermal Shutdown Hysteresis			--	10	--	°C
Discharge						
VOUTx Discharge Current	I_{DISx}	ENTRIPx = ENC = 0V, V_{OUTx} = 0.5V	10	60	--	mA
VREGx Discharge Current		EN = 0V, VREGx = 0.5V	2.5	--	--	mA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Input						
FB1/FB2 Input Voltage		Low Level (Internal Fixed VOUTx)	--	--	0.2	V
		High Level (Internal Fixed VOUTx)	4.5	--	--	
SKIPSEL Input Voltage		Low Level (DEM Mode)	--	--	0.8	V
		REF Level (PWM Mode)	1.8	--	2.3	
		High Level (Ultrasonic Mode)	2.7	--	--	
ENTRIPx Input Voltage	$V_{ENTRIPx}$	Low Level (SMPSs Off)	--	--	0.35	V
		On Level (SMPSs On)	0.5	--	2	
		High Level (SMPSs Off)	4.5	--	--	
EN Voltage	V_{EN}	Shutdown	--	--	0.4	V
		Enable	2.4	--	--	
		Open	2.4	3.3	4.2	
EN Current	I_{EN}	V_{EN} = 0.2V (Source)	1	3	5	μA
		V_{EN} = 3.3V (Sink)	--	3	8	
ENC Threshold Voltage (RT8223B)	V_{ENC}	Shutdown	--	--	0.6	V
		Enable	2	--	--	
TONSEL Setting Voltage		V_{OUT1}/V_{OUT2} = 200kHz/250kHz	--	--	0.8	V
		V_{OUT1}/V_{OUT2} = 300kHz/375kHz	1.8	--	2.3	
		V_{OUT1}/V_{OUT2} = 400kHz/500kHz	2.7	--	--	
Input Leakage Current		TONSEL, SKIPSEL = 0V or 5V	−1	--	1	μA
		ENC = 0V or 5V (RT8223B)	−1	--	1	
Internal BOOT Switch						
Internal Boost Charging Switch On-Resistance		VREG5 to BOOTx	--	20	--	Ω
Power MOSFET Drivers						
UGATEx On-Resistance		UGATEx, High state	--	3	6	Ω
		UGATEx, Low state	--	1.5	4	
LGATEx On-Resistance		LGATEx, High State	--	2.2	5	
		LGATEx, Low State	--	0.6	1.5	
Dead Time		LGATEx Rising	--	30	--	ns
		UGATEx Rising	--	40	--	

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case positions of θ_{JC} are on the lead of the SOP package and the expose pad for the SOP(Exposed Pad) package.

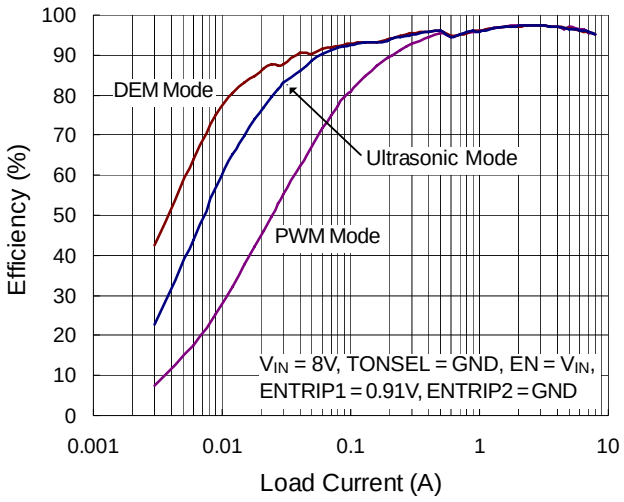
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

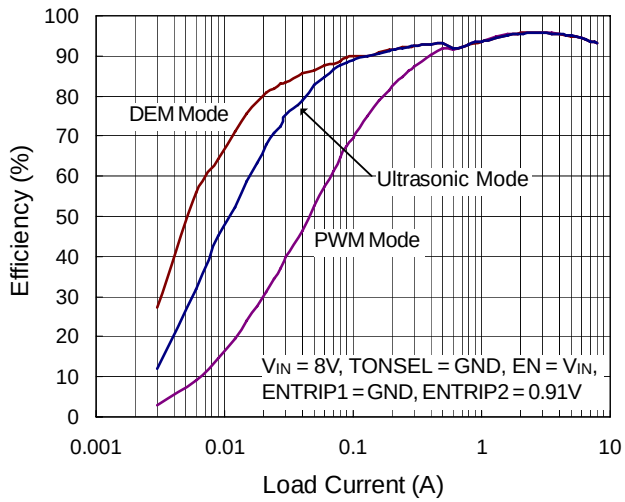
Note 5. $P_{VIN} + P_{VREG5}$

Typical Operating Characteristics

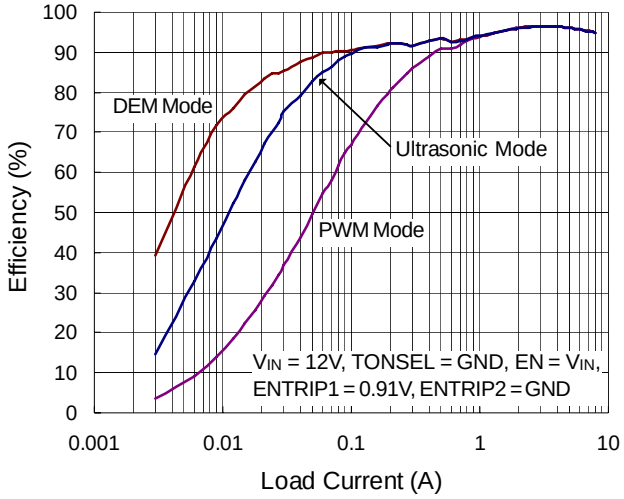
V_{OUT1} Output Efficiency vs. Load Current



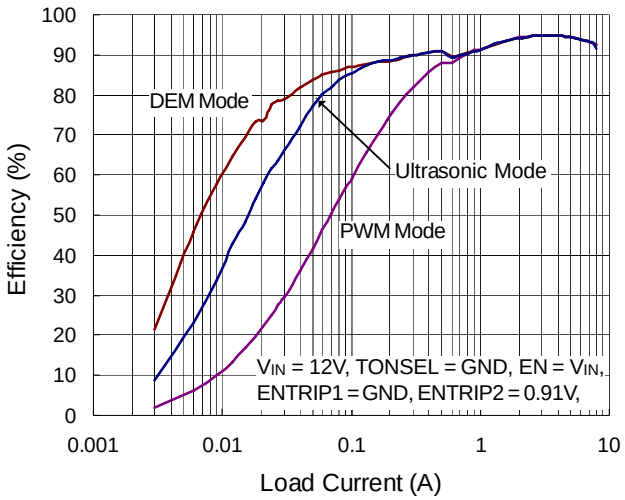
V_{OUT2} Output Efficiency vs. Load Current



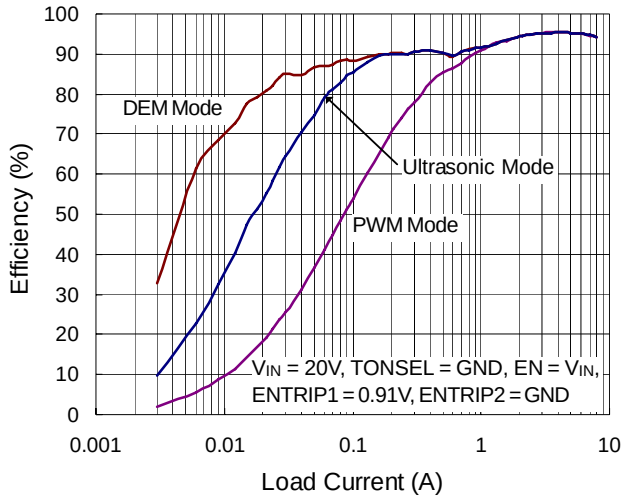
V_{OUT1} Output Efficiency vs. Load Current



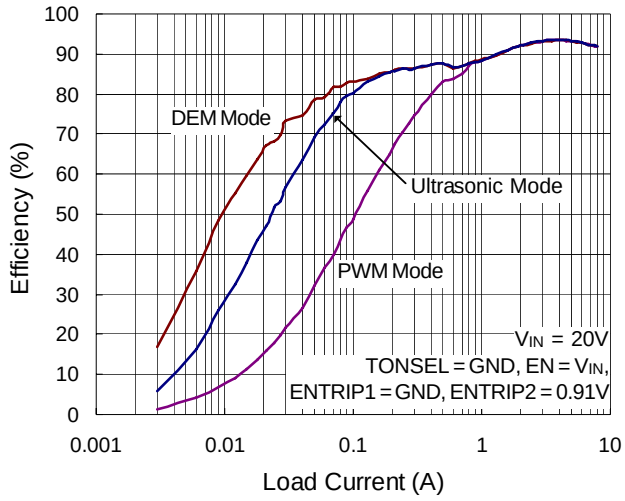
V_{OUT2} Output Efficiency vs. Load Current



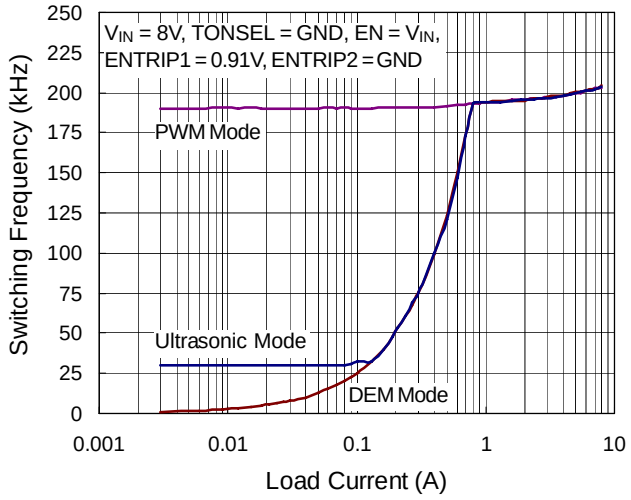
V_{OUT1} Output Efficiency vs. Load Current



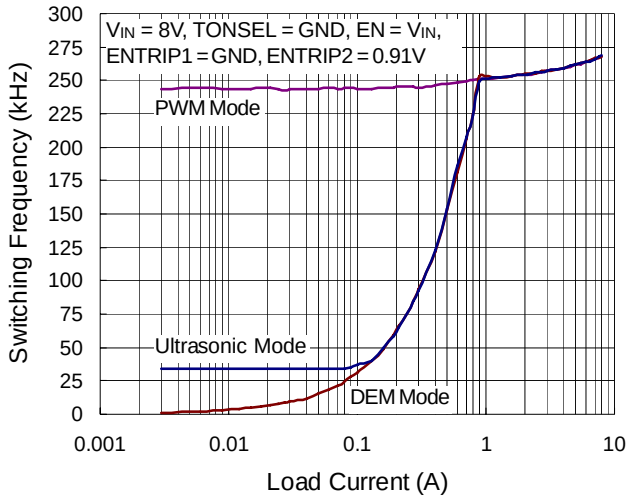
V_{OUT2} Output Efficiency vs. Load Current



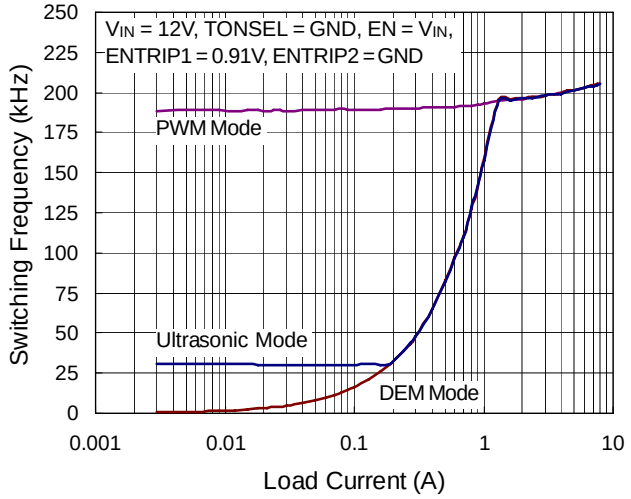
V_{OUT1} Output Switching Frequency vs. Load Current



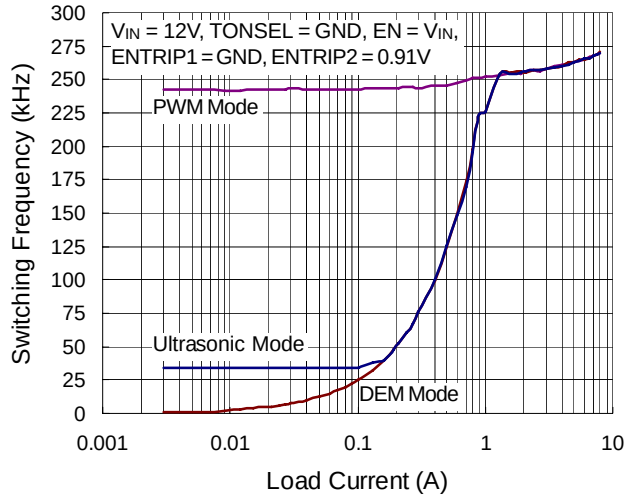
V_{OUT2} Output Switching Frequency vs. Load Current



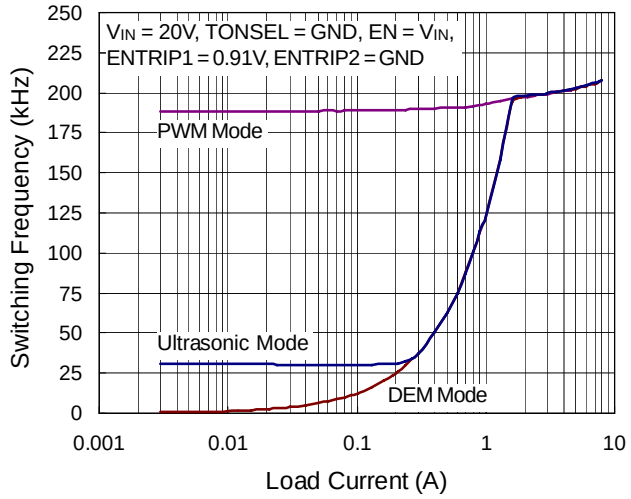
V_{OUT1} Output Switching Frequency vs. Load Current



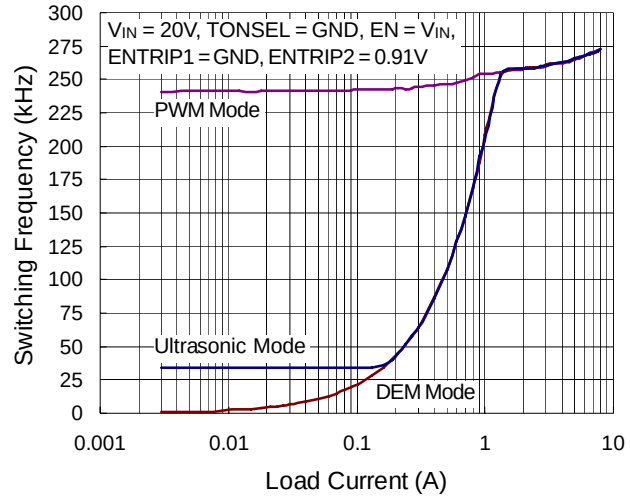
V_{OUT2} Output Switching Frequency vs. Load Current



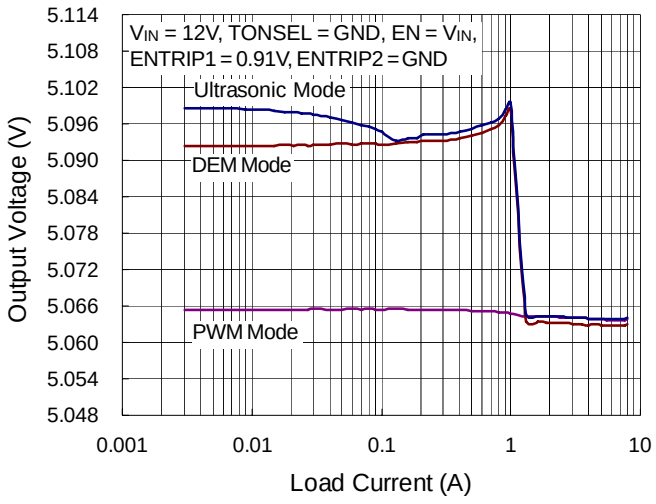
V_{OUT1} Output Switching Frequency vs. Load Current



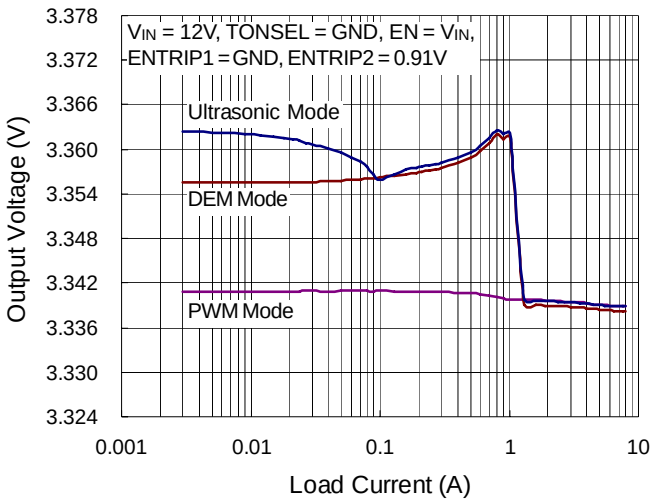
V_{OUT2} Output Switching Frequency vs. Load Current



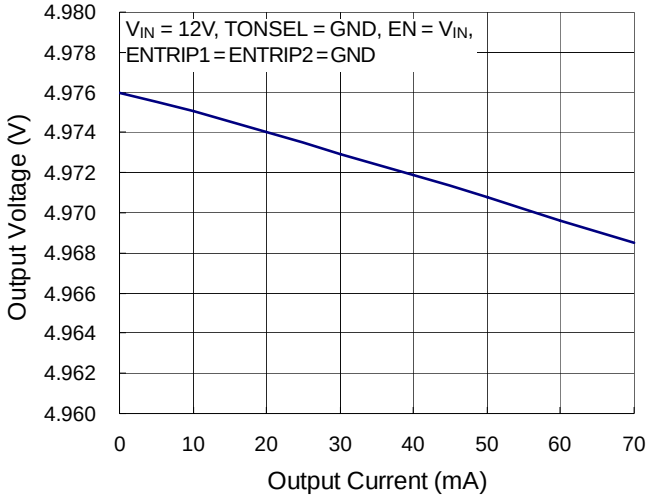
V_{OUT1} Output Voltage vs. Load Current



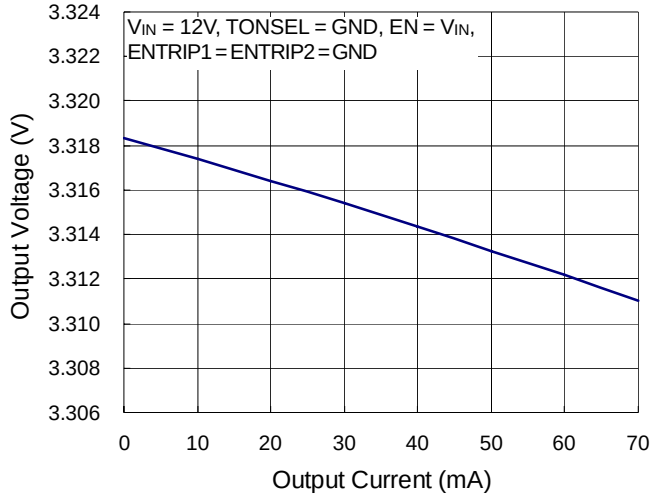
V_{OUT2} Output Voltage vs. Load Current



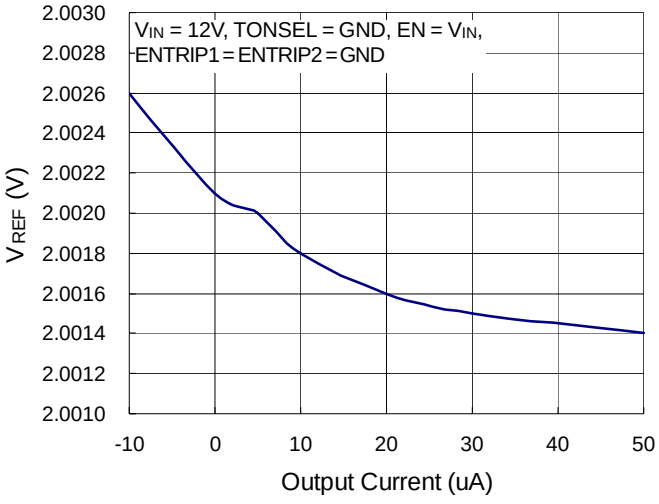
VREG5 Output Voltage vs. Output Current



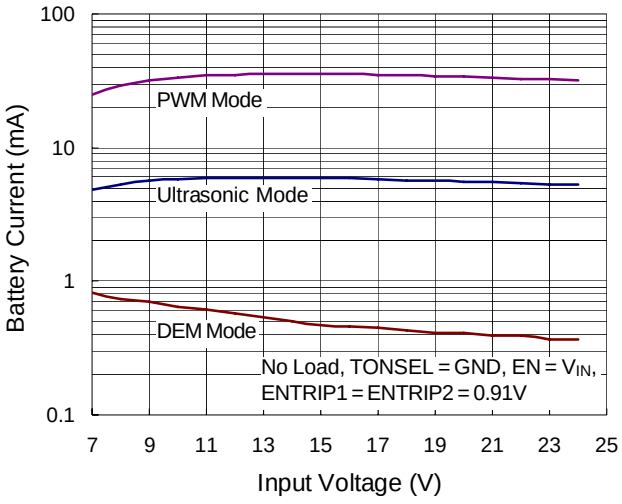
VREG3 Output Voltage vs. Output Current



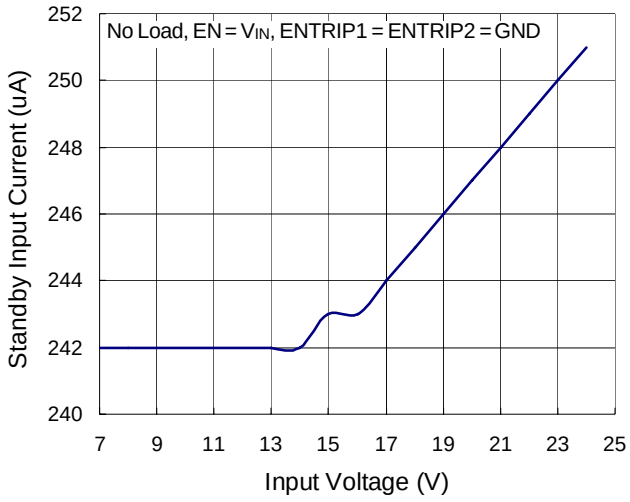
V_{REF} vs. Output Current



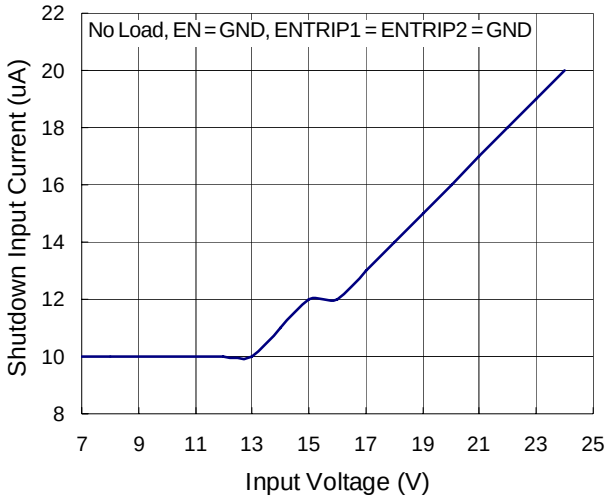
Battery Current vs. Input Voltage



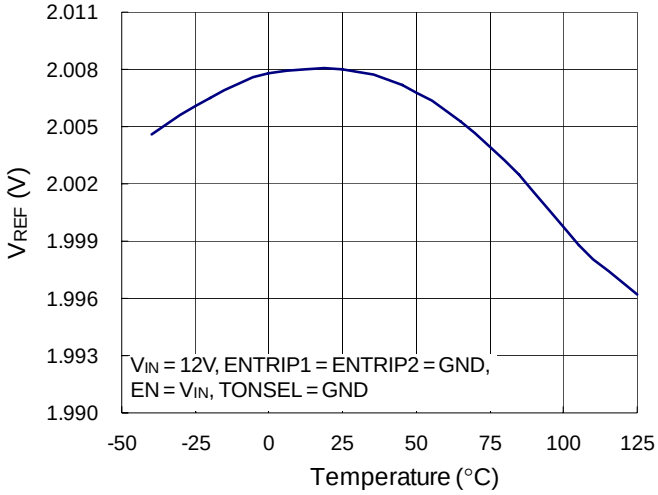
Standby Input Current vs. Input Voltage



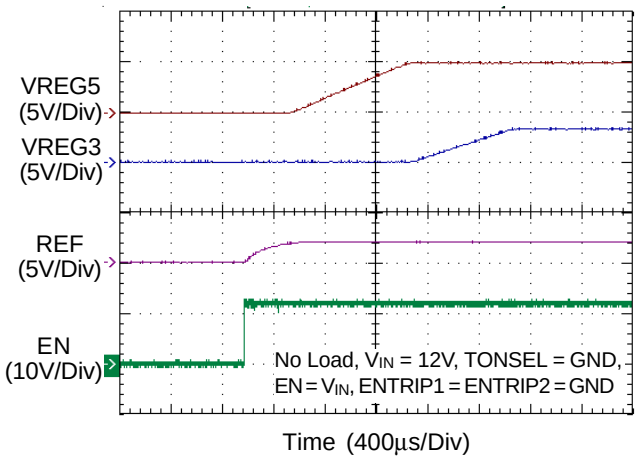
Shutdown Input Current vs. Input Voltage



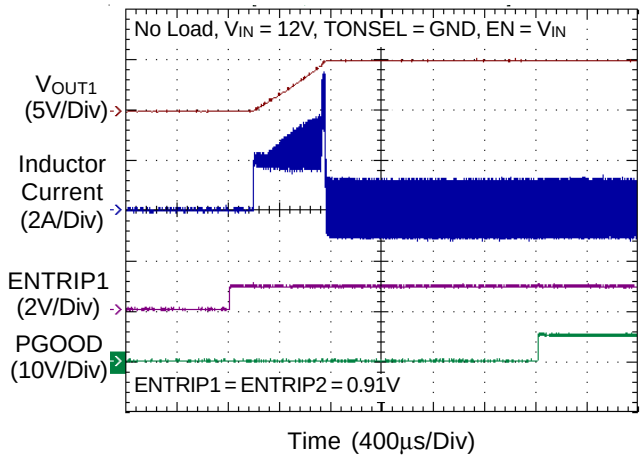
V_{REF} vs. Temperature



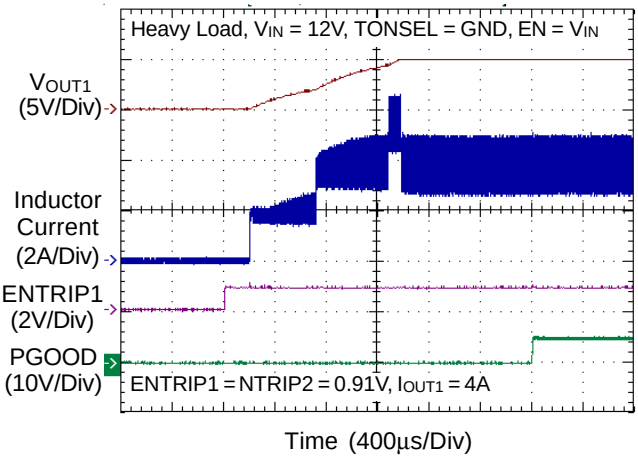
Start Up



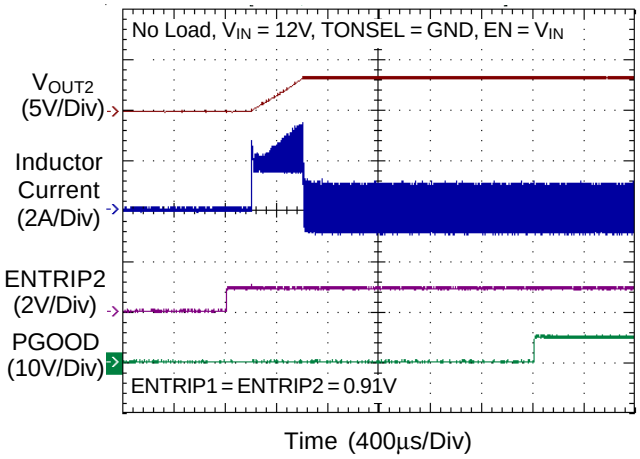
V_{OUT1} Start Up



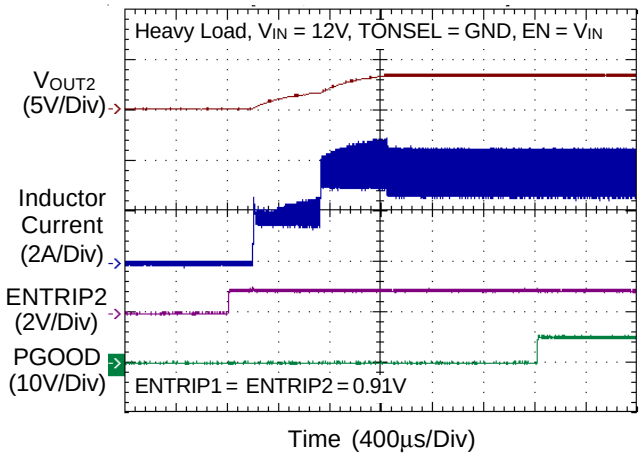
V_{OUT1} Start Up



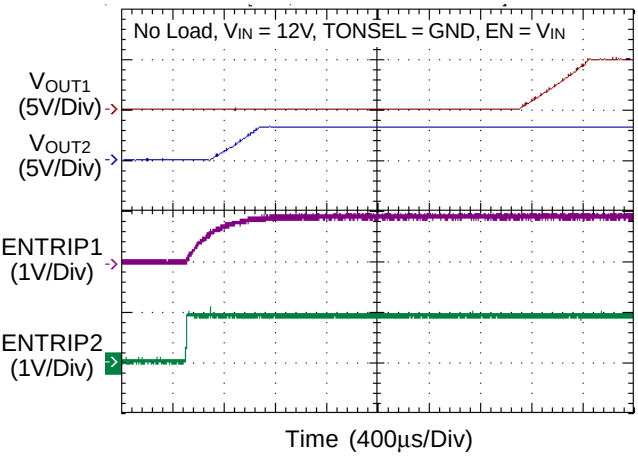
V_{OUT2} Start Up



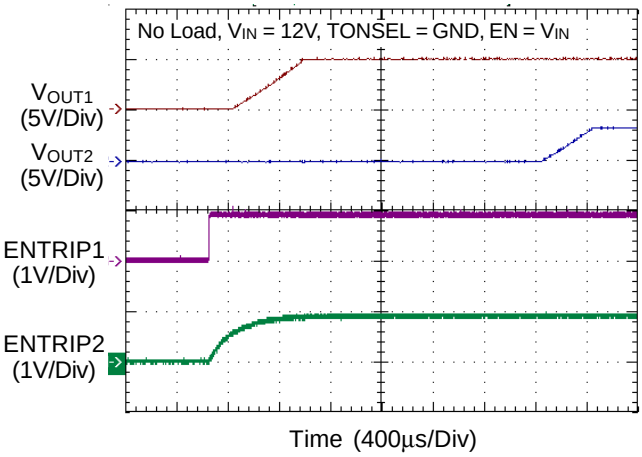
V_{OUT2} Start Up



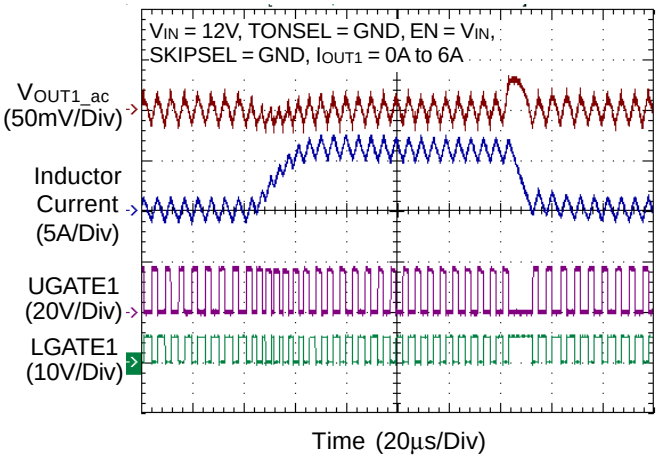
V_{OUT1} Delay Start



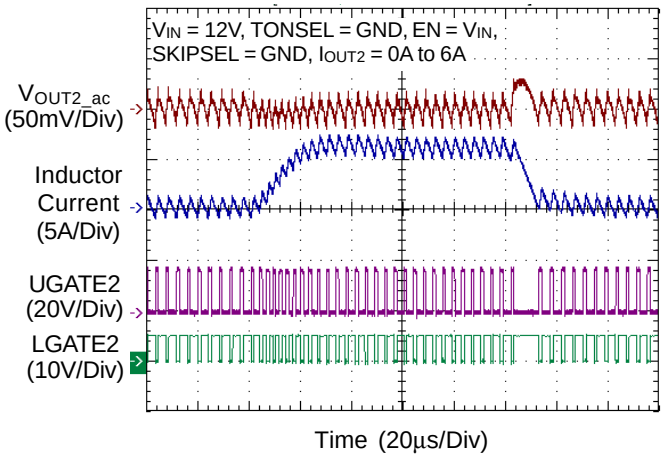
V_{OUT2} Delay Start



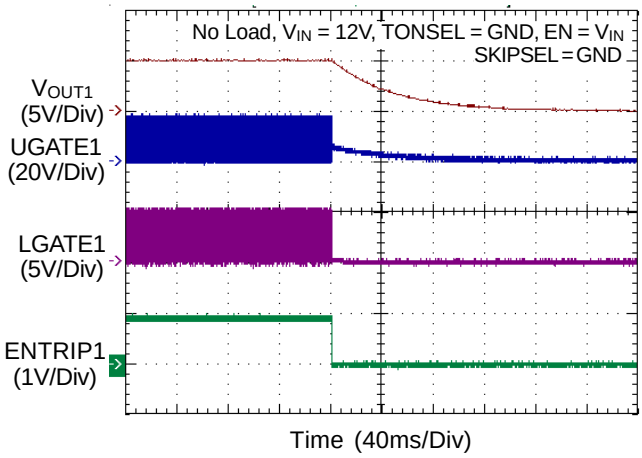
V_{OUT1} PWM Mode Load Transient Response



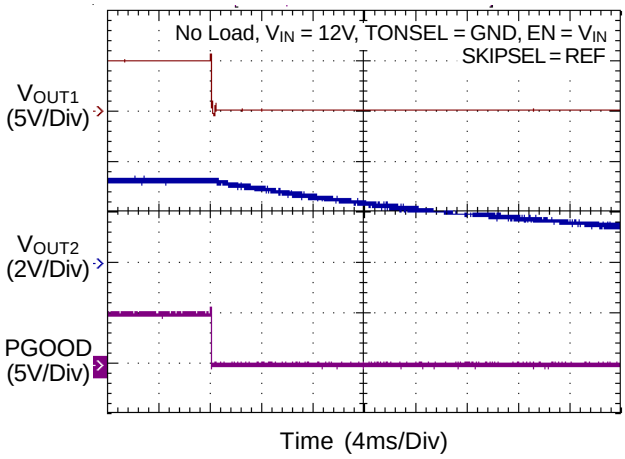
V_{OUT2} PWM Mode Load Transient Response



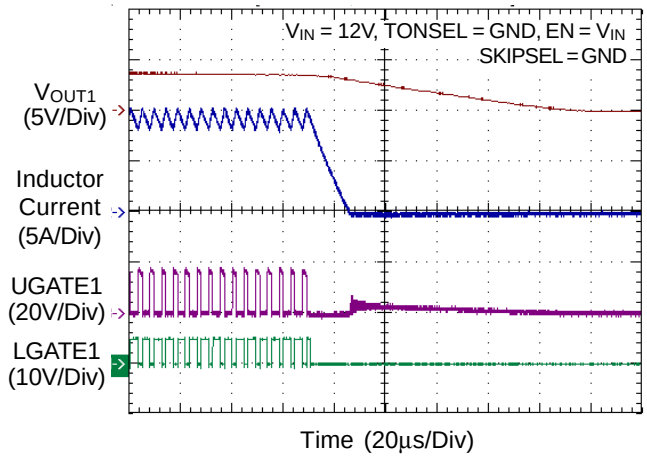
Power Off from ENTRIP1



OVP



UVP



Application Information

The RT8223A/B is a dual, Mach Response™ DRV™ dual ramp valley mode synchronous buck controller. The controller is designed for low voltage power supplies for notebook computers. Richtek's Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load-transient timing problems of fixed-frequency current mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a dual output application. The RT8223A/B includes 5V (VREG5) and 3.3V (VREG3) linear regulators. VREG5 linear regulator can step down the battery voltage to supply both internal circuitry and gate drivers. The synchronous-switch gate drivers are directly powered from VREG5. When VOUT1 voltage is above 4.66V, an automatic circuit will switch the power of the device from VREG5 linear regulator from VOUT1.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's effective series resistance (ESR) to act as a current sense resistor, so the output ripple voltage provides the PWM ramp signal. Refer to the RT8223A/B's function block diagram, the synchronous high-side MOSFET will be turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this one shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage range. Another one shot sets a minimum off-time (300ns typ.). The on-time one shot will be triggered if the error comparator is high, the low side switch current is below the current limit threshold, and the minimum off-time one shot has timed out.

PWM Frequency and On-Time Control

The Mach Response™ control architecture runs with pseudo-constant frequency by feed forwarding the input and output voltage into the on-time one shot timer. The high-side switch on-time is inversely proportional to the input voltage as measured by the V_{IN}, and proportional to the output voltage. There are two benefits of a constant switching frequency. The first is the frequency can be selected to avoid noise sensitive regions such as the 455kHz IF band. The second is the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The frequency for 3V SMPS is set at 1.25 times higher than the frequency for 5V SMPS. This is done to prevent audio-frequency "beating" between the two sides, which switch asynchronously for each side. The frequencies are set by TONSEL pin connection as Table1. The on-time is given by :

$$\text{On-Time} = K \times (V_{OUT} / V_{IN})$$

where "K" is set by the TONSEL pin connection (Table 1). The on-time guaranteed in the Electrical Characteristics tables are influenced by switching delays in the external high-side power MOSFET. Two external factors that influence switching-frequency accuracy are resistive drops in the two conduction loops (including inductor and PC board resistance) and the dead-time effect. These effects are the largest contributors to the change of frequency with changing load current. The dead time effect increases the effective on-time, reducing the switching frequency as one or both dead times. It occurs only in PWM mode (SKIPSEL= REF) when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes PHASEx to go high earlier than normal, extending the on-time by a period equal to the low-to-high dead time. For loads above the critical conduction point, the actual switching frequency is :

$$f = (V_{OUT} + V_{DROP1}) / (t_{ON} \times (V_{IN} + V_{DROP1} - V_{DROP2}))$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path; and t_{ON} is the on-time calculated by the RT8223A/B.

Table 1. TONSEL Connection and Switching Frequency

TON	SMPS 1 K-Factor (us)	SMPS 1 Frequency (kHz)	SMPS 2 K-Factor (us)
GND	5	200	4
REF	3.33	300	2.67
VREG5 or VREG3	2.5	400	2

TON	SMPS 2 Frequency (kHz)	Approximate K-Factor Error (%)
GND	250	±10
REF	375	±10
VREG5 or VREG3	500	±10

Operation Mode Selection (SKIPSEL)

The RT8223A/B supports three operation modes : Diode Emulation Mode, Ultrasonic Mode, and Forced CCM Mode.

Diode-Emulation Mode (SKIPSEL = GND)

In Diode Emulation mode, The RT8223A/B automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increase of V_{OUT} ripple or load regulation. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low-side MOSFET allows only partial of negative current when the inductor free-wheeling current reach negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level that requires the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation can be calculated as follows (Figure 1) :

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times T_{ON}$$

where Ton is the On-time.

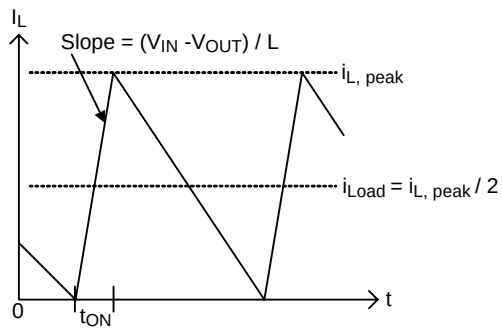


Figure 1. Boundary condition of CCM/DCM

The switching waveforms may appear noisy and asynchronous when light loading causes Diode-Emulation operation, but this is a normal operating condition that results in high light load efficiency. Trade offs in PFM noise vs. light load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input-voltage levels).

Ultrasonic Mode (SKIPSEL = VREG5 or VREG3)

Connecting SKIPSEL to VREG5 or VREG3 activates a unique Diode-Emulation mode with a minimum switching frequency of 25kHz. This ultrasonic mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the low-side switch gate driver signal is OR with an internal oscillator (>25kHz). Once the internal oscillator is triggered, the ultrasonic controller pulls LGATEx high, turning on the low side MOSFET to induce a negative inductor current. After the output voltage across the REF, the controller turns off the low-side MOSFET (LGATEx pulled low) and triggers a constant on-time (UGATEx driven high). When the on-time has expired, the controller re-enables the low-side MOSFET until the controller detects that the inductor current dropped below the zero-crossing threshold.

Forced CCM Mode (SKIPSEL = REF)

The low-noise, forced CCM mode (SKIPSEL = REF) disables the zero-crossing comparator, which controls the low side switch on-time. This causes the low side gate driver waveform to become the complement of the high

side gate-driver waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio of V_{OUT}/V_{IN}. The benefit of forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost : The no load battery current can be 10mA to 40mA, depending on the external MOSFETs.

Reference and linear Regulators (REF, VREGx)

The 2V reference (REF) is accurate within ±1% over temperature, making REF useful as a precision system reference. Bypass REF to GND with a 0.22µF (min) capacitor. REF can supply up to 50uA for external loads. Loading REF reduces the VOUTx output voltage slightly because of the reference load regulation error.

VREG5 regulator supplies total of 70mA for internal and external loads, including MOSFET gate driver and PWM controller. VREG3 regulator supplies up to 70mA for external loads. Bypass VREG5 and VREG3 with a 4.7µF (min) capacitor; use an additional 1µF per 5mA of internal and external load.

When the 5V main output voltage is above the VREG5 switchover threshold, an internal 1.5Ω N-MOSFET switch connects VOUT1 to VREG5 while simultaneously shutting down the VREG5 linear regulator. Similarly, when the 3.3V main output voltage is above the VREG3 switchover threshold, an internal 1.5Ω N-MOSFET switch connects VOUT2 to VREG3 while simultaneously shutting down the VREG3 linear regulator. It can decrease the power dissipation from the same battery, because the converted efficiency of SMPS is better than the converted efficiency of linear regulator.

Current Limit Setting (ENTRIPx)

The RT8223A/B has cycle-by-cycle current limiting control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASEx is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 2). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, battery and output voltage.

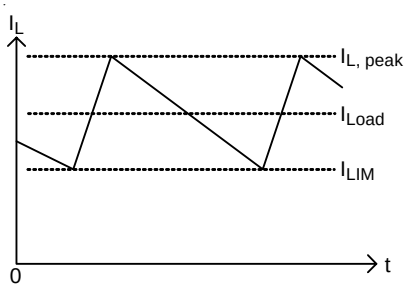


Figure 2. "valley" Current-Limit

The RT8223A/B uses the on resistance of the synchronous rectifier as the current sense element. Use the worse case maximum value for $R_{DS(ON)}$ from the MOSFET datasheet, and add a margin of 0.5%/°C for the rise in $R_{DS(ON)}$ with temperature.

The R_{ILIM} resistor between the ENTRIPx pin and GND sets the over current threshold. The resistor R_{ILIM} is connected to a 10µA current source from ENTRIPx. When the voltage drop across the sense resistor or low side MOSFET equals 1/10 the voltage across the R_{ILIM} resistor, positive current limit will be activated. The high side MOSFET will not be turned on until the voltage drop across the MOSFET falls below 1/10 the voltage across the R_{ILIM} resistor.

Choose a current limit resistor by following equation :

$V_{ILIM} = (R_{ILIM} \times 10\mu A) / 10 = I_{ILIM} \times R_{DS(ON)}$

$R_{ILIM} = (I_{ILIM} \times R_{DS(ON)}) \times 10 / 10\mu A$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current sense signal at PHASEx and GND. Mount or place the IC close to the low side MOSFET.

MOSFET Gate Driver (UGATEx, LGATEx)

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5-V bias voltage is delivered from VREG5 supply. The average drive current is also calculated by the gate charge at V_{GS} = 5 V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOTx and PHASEx pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on.

The low side driver is designed to drive high current low $R_{DS(ON)}$ N-MOSFET(s). The internal pull down transistor

that drives LGATEx low is robust, with a 0.6Ω typical on-resistance. A 5V bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by an input capacitor connected between VREG5 and GND.

For high current applications, some combinations of high and low side MOSFETs might be encountered that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BOOTx, which increases the turn-on time of the high side MOSFET without degrading the turn-off time (Figure 3).

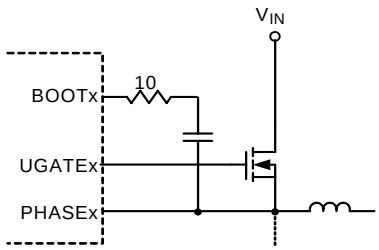


Figure 3. Reducing the UGATEx Rise Time

Soft-Start

A build-in soft-start is used to prevent surge current from power supply input after ENTRIPx is enabled. The typical soft-start duration is 2ms period. Furthermore, the maximum allowed current limit is segmented in 5 steps: 20%, 40%, 60%, 80% and 100% during the 2ms period.

UVLO Protection

The RT8223A/B has VREG5 under voltage lock out protection (UVLO). When the VREG5 voltage is lower than 4.2V (typ.) and the VREG3 voltage is lower than 2.5V (typ.), both switch power supplies will be shut off. This is a non-latch protection.

Power Good Output (PGOOD)

The PGOOD is an open-drain type output and requires a pull-up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. It will be released when both output voltage are above 92.5% of nominal regulation point. The PGOOD goes low if either output turns off or is 10% below its nominal regulator point.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage. When over voltage protection is enabled, if the output voltage exceeds 11% of its set voltage threshold, the over voltage protection will be triggered and the LGATEx low-side gate drivers will be forced high. This activates the low side MOSFET switch, which rapidly discharges the output capacitor and pulls the input voltage downward.

RT8223A/B will be latched once OVP is triggered and can only be released by EN power-on reset. There is a 10μs delay built into the over voltage protection circuit to prevent false transition.

Note that LGATEx latching high causes the output voltage to dip slightly negative when energy has been previously stored in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the over voltage condition is caused by a short in high-side switch, turning the low side MOSFET on 100% creates an electrical short between the battery and GND, blowing the fuse and disconnecting the battery from the output.

Output Under voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When under voltage protection is enabled, if the output is less than 70% of its set voltage threshold, under voltage protection will be triggered, then both UGATEx and LGATEx gate drivers are forced low while entering soft-discharge mode. During soft-start, the UVP will be blanked around 3ms.

Thermal Protection

The RT8223A/B provides thermal shutdown to prevent the overheat damage. Thermal shutdown occurs when the die temperature exceeds +150°C. All internal circuitry shuts down during thermal shutdown. The RT8223A/B triggers thermal shutdown if VREGx is not supplied from VOUTx, while input voltage on VIN and drawing current from VREGx are too high. Even if VREGx is supplied from VOUTx, overloading the VREGx causes large power dissipation on automatic switches, which may result in thermal shutdown.

Discharge Mode (Soft Discharge)

When ENTRIPx is low and a transition to standby, shutdown mode occurs, or the output under voltage fault latch is set, the outputs discharge mode will be triggered. During discharge mode, there is one path to discharge the outputs capacitor residual charge. That is output capacitor discharge to GND through an internal MOS switch.

Shutdown Mode

The RT8223A/B SMPS1, SMPS2, VREG3 and VREG5 have independent enabling control. Drive EN, ENTRIP1, ENTRIP2 and ENC below the precise input falling edge trip level to place the RT8223A/B in its low power shutdown state. The RT8223A/B consumes only 20μA of input current while in shutdown.

Power-Up Sequencing and On/Off Controls (ENTRIPx, ENC)

ENTRIP1 and ENTRIP2 control SMPS power-up sequencing. When the RT8223A/B applies in the single channel mode, ENTRIP1 or ENTRIP2 enables the respective outputs when ENTRIPx voltage rises above 0.4V. Furthermore, the RT8223A/B applies in the dual channel mode. ENC enables the outputs when ENC voltage rises above 2V.

If both of ENTRIP1 and ENTRIP2 become higher than the enable threshold voltage at a different time (without 60μs), one can force the latter one output starts after the former one regulates.

Output Voltage Setting (FBx)

Connect FBx directly to GND or VREG5 to enable the fixed, SMPS output voltages (3.3V and 5V). Connect a resistor voltage divider at the FBx between the VOUTx and GND to adjust the respective output voltage between 2V and 5.5V (Figure 4). Choose R2 to be approximately 10kΩ, and solve for R1 using the equation :

$$V_{OUTx} = V_{FBx} \times \left[1+\left(\frac{R1}{R2}\right)\right]$$

where V_{FBx} is 2V (typ.).

VREG5 connects to VOUT1 through an internal switch only when VOUT1 is above the VREG5 automatic switch threshold (4.66V). VREG3 connects to VOUT2 through an internal switch only when VOUT2 is above the VREG3 automatic switch threshold (3V). This is the most effective way when the fixed output voltages are used. Once VREGx is supplied from VOUTx, the internal linear regulator turns off. This reduces internal power dissipation and improves efficiency when the VREGx is powered with a high input voltage.

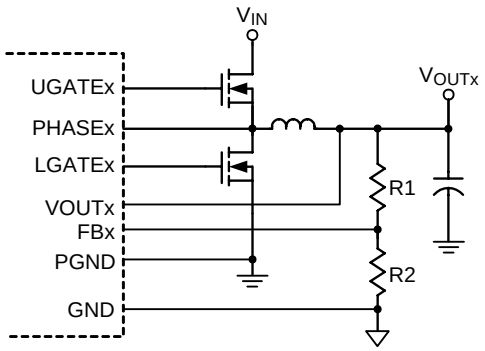


Figure 4. Setting VOUTx with a Resistor-Divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or L_{IR}) determine the inductor value as shown as follows :

$$L = \frac{T_{ON} \times (V_{IN} - V_{OUTx})}{L_{IR} \times I_{LOAD(MAX)}}$$

where L_{IR} is the ratio of the peak to peak ripple current to the average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + [(L_{IR} / 2) \times I_{LOAD(MAX)}]$$

This inductor ripple current also impacts transient-response performance, especially at low VIN – VOUTx differences. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The peak amplitude of the output transient V_{SAG} is also a function of the output transient. The V_{SAG} also features a function of the

maximum duty factor, which can be calculated from the on-time and minimum off-time :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times \left(K \frac{V_{OUTx}}{V_{IN}} + T_{OFF(MIN)}\right)}{2 \times C_{OUT} \times V_{OUTx} \times \left[K\left(\frac{V_{IN} - V_{OUTx}}{V_{IN}}\right) - T_{OFF(MIN)}\right]}$$

Where minimum off-time ($T_{OFF(MIN)}$) = 300ns (typ.) and K is from Table 1.

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full load to no load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{L_{IR} \times I_{LOAD(MAX)}}$$

where V_{P-P} is the peak to peak output voltage ripple.

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

For low input to output voltage differentials (VIN / VOUTx < 2), additional output capacitance is required to maintain stability and good efficiency in ultrasonic mode.

The amount of overshoot due to stored inductor energy can be calculated as :

$$V_{SOAR} \leq \frac{(I_{PEAK})^2 \times L}{2 \times C_{OUT} \times V_{OUTx}}$$

where I_{PEAK} is the peak inductor current.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high-value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high- ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting VOUTx or the FBx divider close to the inductor.

Unstable operation manifests itself in two related and distinctly different ways: double pulsing and feedback loop instability.

Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the 300ns minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero to max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step response under or overshoot.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow

and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8223A/B, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-24L 4x4 package, the thermal resistance θ_{JA} is 52°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (52°C/W) = 1.923W for WQFN-24L 4x4 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8223A/B package, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

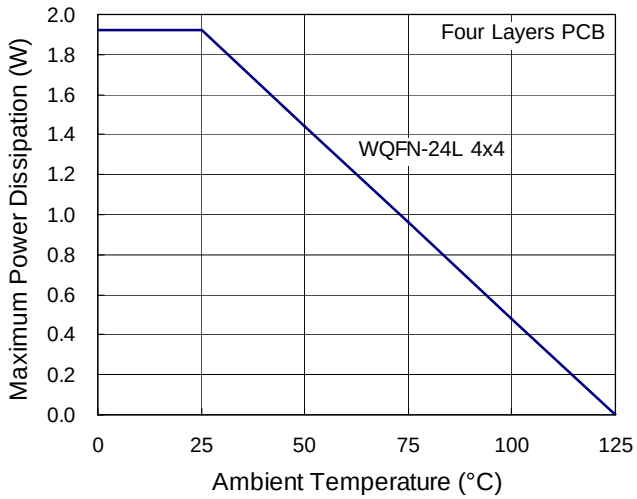


Figure 5. Derating Curve for RT8223A/B Package

Layout Considerations

Layout is very important in high frequency switching converter design. If the IC is designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout using the RT8223A/B.

- Place the filter capacitor close to the IC, within 12 mm (0.5 inch) if possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance. Use 0.65-mm (25 mils) or wider trace.
- All sensitive analog traces and components such as VOUTx, FBx, GND, ENTRIPx, PGOOD, and TONSEL should be placed away from high voltage switching nodes such as PHASEx, LGATEx, UGATEx, or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Gather ground terminal of VIN capacitor(s), VOUTx capacitor(s), and source of low side MOSFETs as close as possible. PCB trace defined as PHASEx node, which connects to source of high side MOSFET, drain of low side MOSFET and high voltage side of the inductor, should be as short and wide as possible.

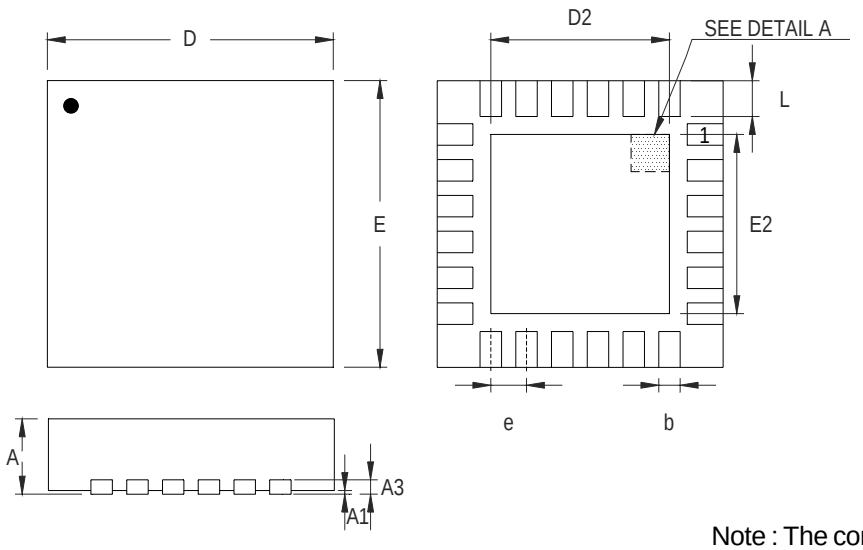
Table 2. Operation Mode Truth Table

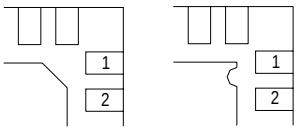
Mode	Test Condition	Comment
Power-UP	VREGx < UVLO threshold	Transitions to discharge mode after a VIN POR and after REF becomes valid. VREG5, VREG3, and REF remain active.
RUN	EN = high, VOUT1 or VOUT2 enabled	Normal Operation.
Over Voltage Protection	Either output > 111% of the nominal level.	LGATEx is forced high. VREG3, VREG5 active. Exited by VIN POR or by toggling EN, ENTRIPx
Under Voltage Protection	Either output < 70% of the nominal level after 3ms time-out expires and output is enabled	Both UGATEx and LGATEx are forced low and enter discharge mode. VREG3, VREG5 active. Exited by VIN POR or by toggling EN, ENTRIPx, ENC
Discharge	Either SMPS output is still high in either standby mode or shutdown mode	During discharge mode, there is one path to discharge the outputs capacitor residual charge. That is output capacitor discharge to GND through an internal switch.
Standby	ENC < startup threshold, EN = high.	VREG3, VREG5 active.
Shutdown	EN = low	All circuitry off.
Thermal Shutdown	TJ > +150°C	All circuitry off. Exit by VIN POR or by toggling EN, ENTRIPx, ENC

Table 3. Power Up Sequencing

EN (V)	ENC (V)	ENTRIP1 (V)	ENTRIP2 (V)	VREG5	VREG3	SMPS1	SMPS2
Low	Low	X	X	Off	Off	Off	Off
“>1V” => High	Low	X	X	On (after REF powers up)	On (after REF powers up)	Off	Off
“>1V” => High	“>2V” => High	Low	Low	On (after REF powers up)	On (after REF powers up)	Off	Off
“>1V” => High	“>2V” => High	Low	High	On (after REF powers up)	On (after REF powers up)	Off	On
“>1V” => High	“>2V” => High	High (after ENTRIP2 is high without 60μs)	High	On (after REF powers up)	On (after REF powers up)	On (after SMPS2 on)	On
“>1V” => High	“>2V” => High	High	Low	On (after REF powers up)	On (after REF powers up)	On	Off
“>1V” => High	“>2V” => High	High	High (after ENTRIP1 is high without 60μs)	On (after REF powers up)	On (after REF powers up)	ON	On (after SMPS1 on)
“>1V” => High	“>2V” => High	High	High	On (after REF powers up)	On (after REF powers up)	On	On

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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