PEMD12; PUMD12

NPN/PNP resistor-equipped transistors; R1 = 47 kΩ, R2 = 47 kΩ

Rev. 4 — 21 November 2011 Product data sheet

1. Product profile

1.1 General description

NPN/PNP double Resistor-Equipped Transistors (RET) in Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package		PNP/PNP complement	NPN/NPN complement	Package configuration
	NXP	JEITA			
PEMD12	SOT666	-	PEMB2	PEMH2	ultra small and flat lead
PUMD12	SOT363	SC-88	PUMB2	PUMH2	very small

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

1.4 Quick reference data

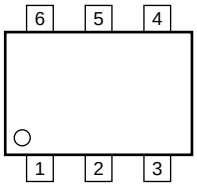
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
R1	bias resistor 1 (input)		33	47	61	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	

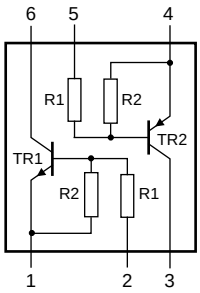
2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		



001aab555



006aaa143

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PEMD12	-	plastic surface-mounted package; 6 leads	SOT666
PUMD12	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 5. Marking codes

Type number	Marking code[1]
PEMD12	D2
PUMD12	D*1

[1] * = placeholder for manufacturing site code

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5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

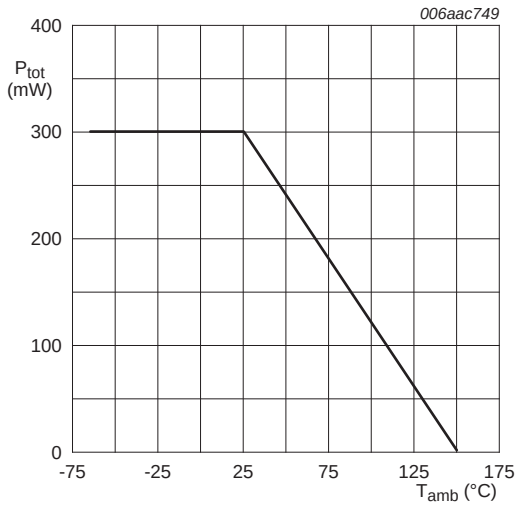
Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage TR1					
	positive			-	+40	V
	negative			-	−10	V
	input voltage TR2					
	positive			-	+10	V
	negative			-	−40	V
I_O	output current			-	100	mA
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD12 (SOT666)		[1][2]	-	200	mW
	PUMD12 (SOT363)		[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD12 (SOT666)		[1][2]	-	300	mW
	PUMD12 (SOT363)		[1]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			−65	+150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

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FR4 PCB, standard footprint

Fig 1. Per device: Power derating curve for SOT363 (SC-88) and SOT666

6. Thermal characteristics

Table 7. Thermal characteristics

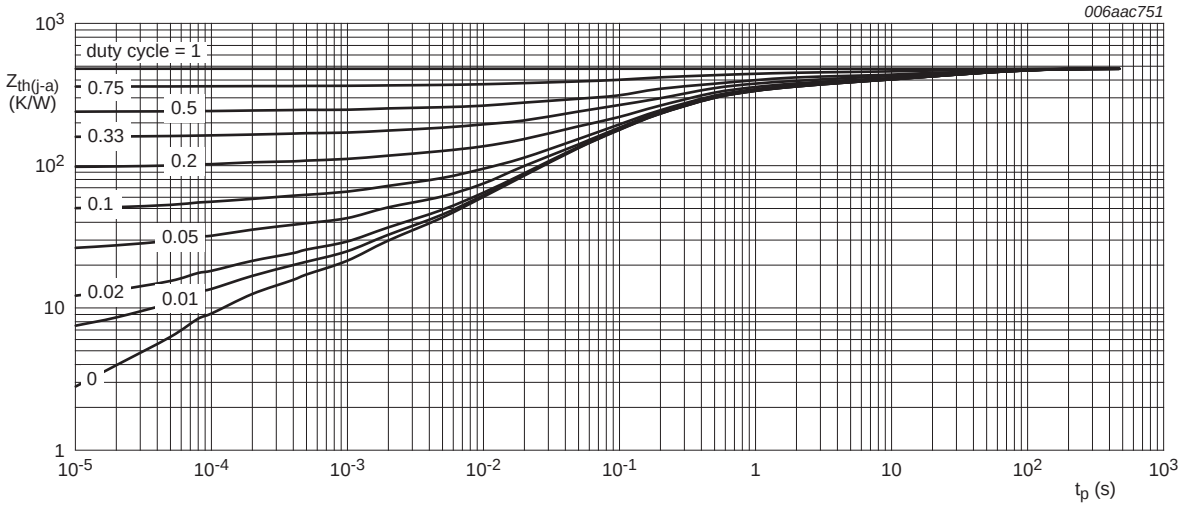
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	PEMD12 (SOT666)		[1][2]	-	-	625	K/W
	PUMD12 (SOT363)		[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	PEMD12 (SOT666)		[1][2]	-	-	417	K/W
	PUMD12 (SOT363)		[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

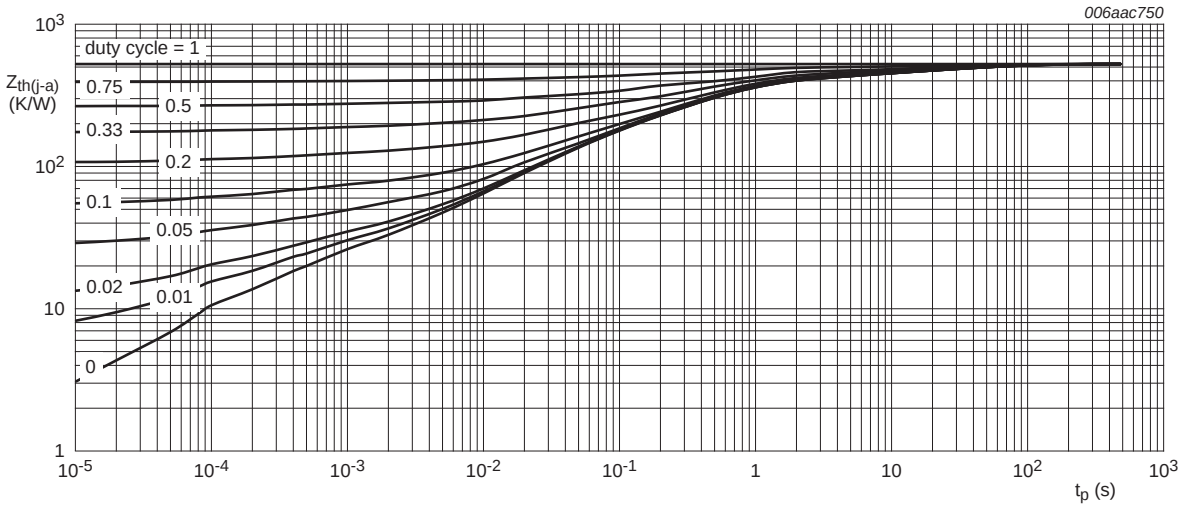
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FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PEMD12 (SOT666); typical values



FR4 PCB, standard footprint

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PUMD12 (SOT363); typical values

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7. Characteristics

Table 8. Characteristics

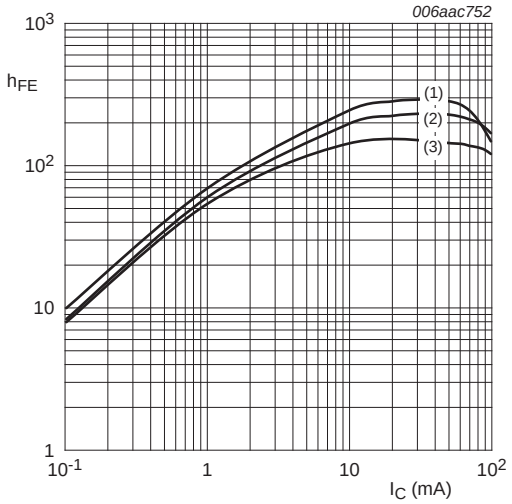
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity						
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A	-	-	1	μA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C	-	-	5	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A	-	-	90	μA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA	80	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	-	-	150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 μA	-	1.2	0.8	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 2 mA	3	1.6	-	V
R1	bias resistor 1 (input)		33	47	61	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	V_{CB} = 10 V; $I_E = i_e$ = 0 A; f = 1 MHz				
	TR1 (NPN)		-	-	2.5	pF
	TR2 (PNP)		-	-	3	pF
f_T	transition frequency	V_{CE} = 5 V; I_C = 10 mA; f = 100 MHz [1]				
	TR1 (NPN)		-	230	-	MHz
	TR2 (PNP)		-	180	-	MHz

[1] Characteristics of built-in transistor

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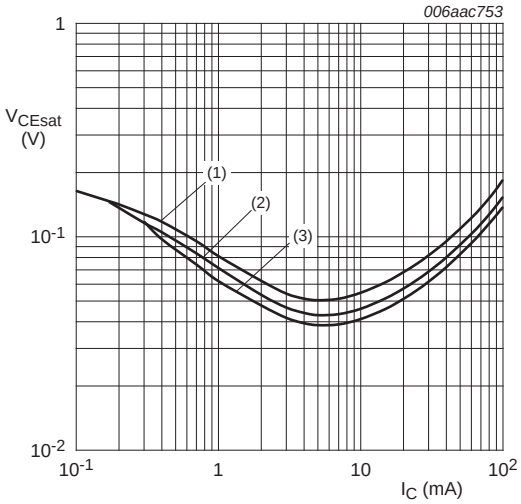
V_{CE} = 5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 4. TR1 (NPN): DC current gain as a function of collector current; typical values



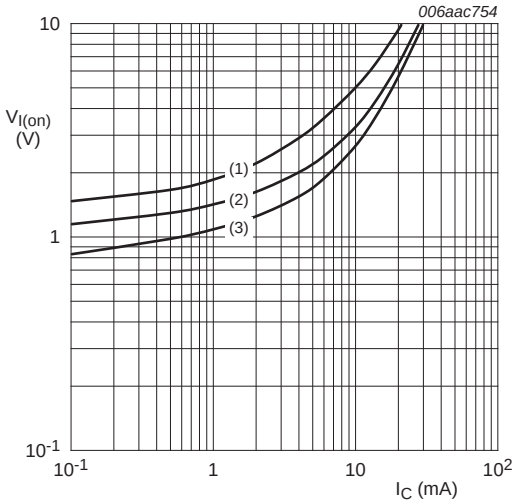
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



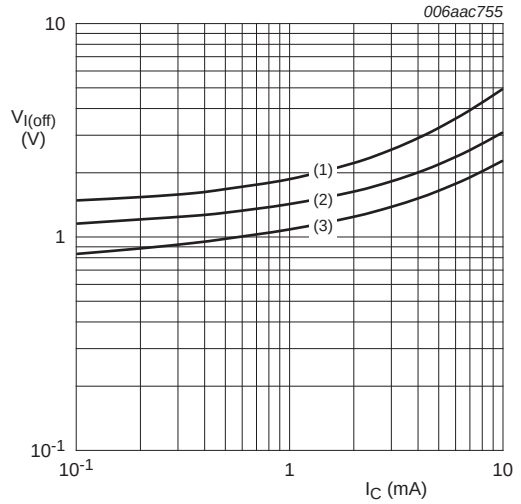
V_{CE} = 0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V

(1) T_{amb} = −40 °C

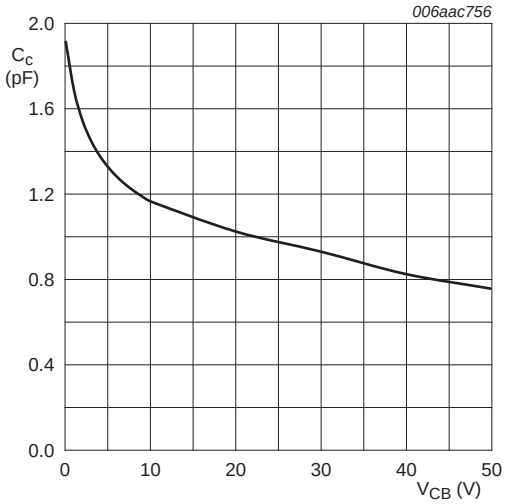
(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values

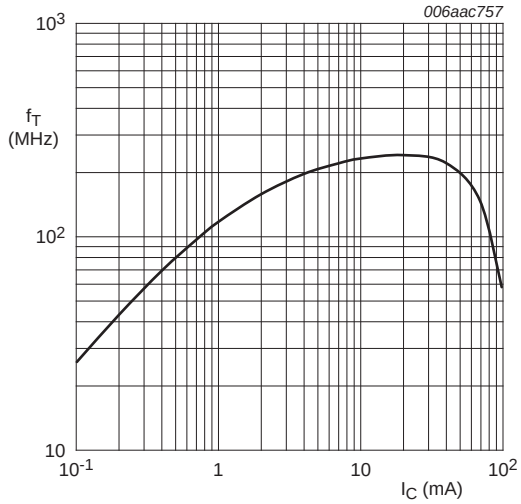
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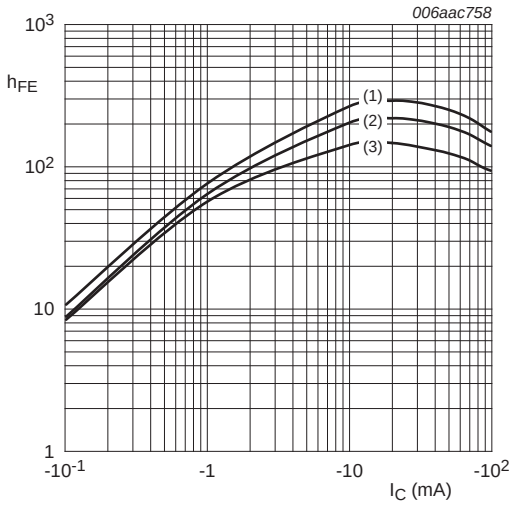
f = 1 MHz; T_{amb} = 25 °C

Fig 8. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values



V_{CE} = 5 V; T_{amb} = 25 °C

Fig 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



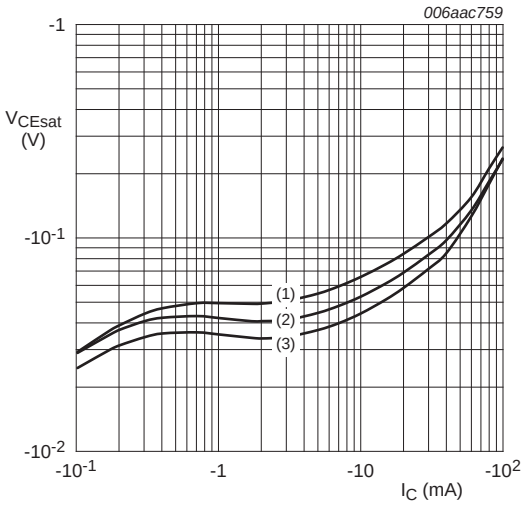
V_{CE} = −5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 10. TR2 (PNP): DC current gain as a function of collector current; typical values



I_C/I_B = 20

(1) T_{amb} = 100 °C

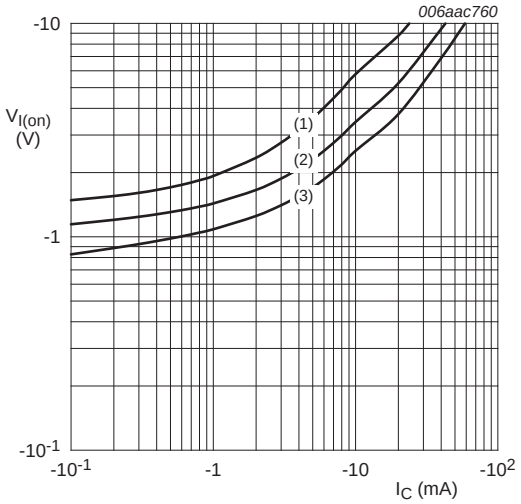
(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 11. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

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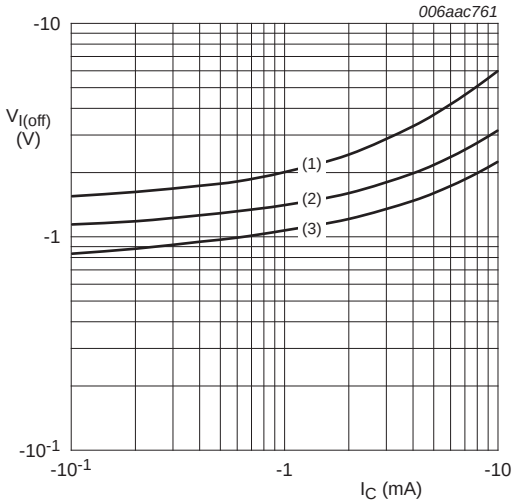
V_{CE} = −0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 12. TR2 (PNP): On-state input voltage as a function of collector current; typical values



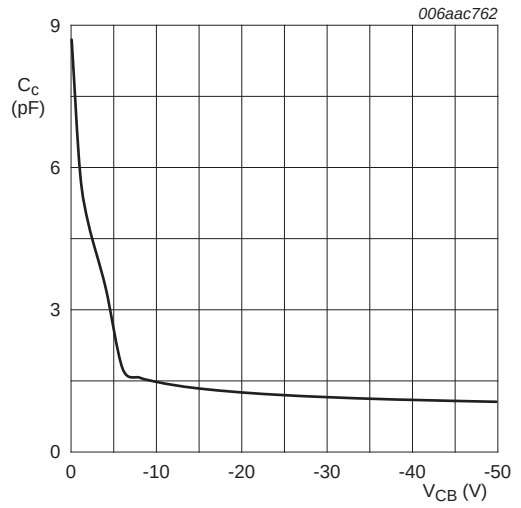
V_{CE} = −5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

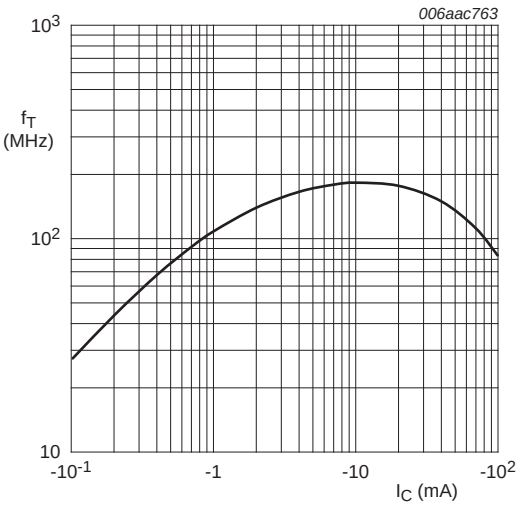
(3) T_{amb} = 100 °C

Fig 13. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig 14. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values of built-in transistor



V_{CE} = −5 V; T_{amb} = 25 °C

Fig 15. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

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8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

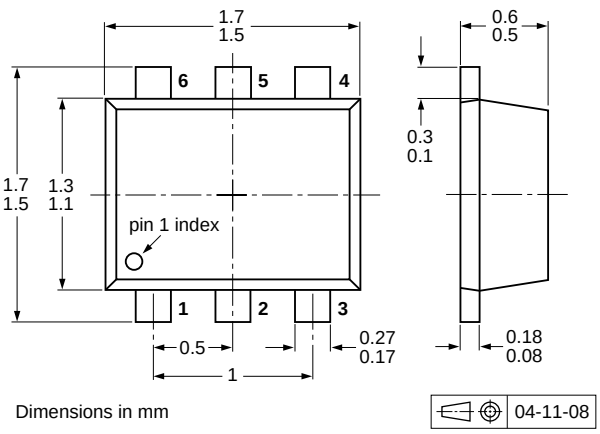


Fig 16. Package outline PEMD12 (SOT666)

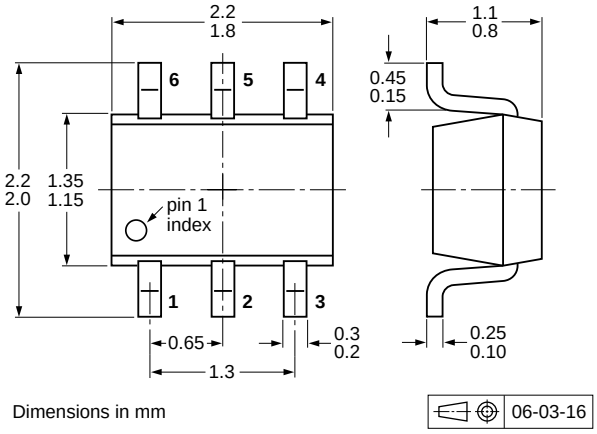


Fig 17. Package outline PUMD12 (SOT363)

10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description		Packing quantity			
				3000	4000	8000	10000
PEMD12	SOT666	2 mm pitch, 8 mm tape and reel		-	-	-315	-
		4 mm pitch, 8 mm tape and reel		-	-115	-	-
PUMD12	SOT363	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-	-	-165

[1] For further information and the availability of packing methods, see Section 14.

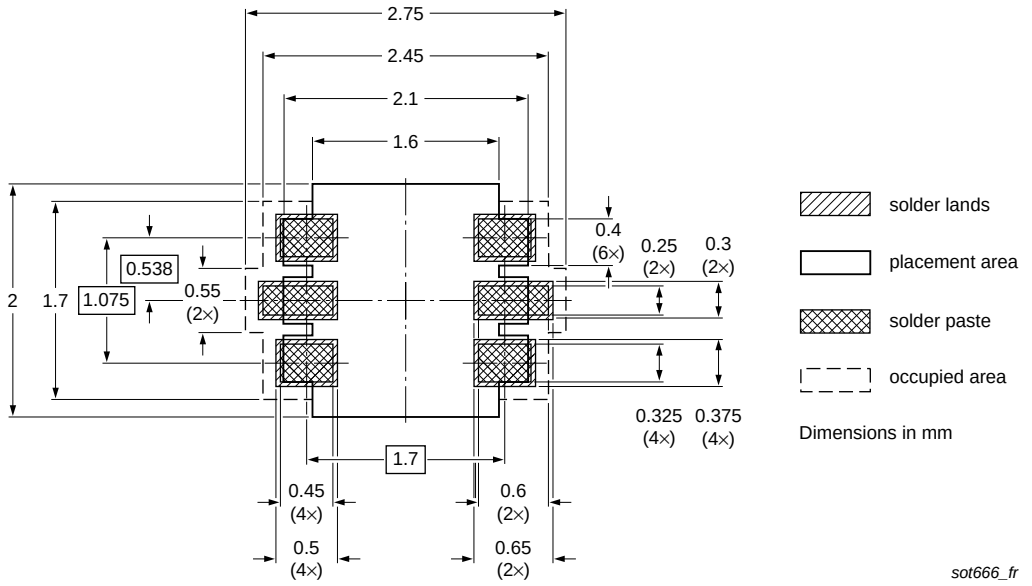
[2] T1: normal taping

[3] T2: reverse taping

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11. Soldering



Reflow soldering is the only recommended soldering method.

Fig 18. Reflow soldering footprint PEMD12 (SOT666)

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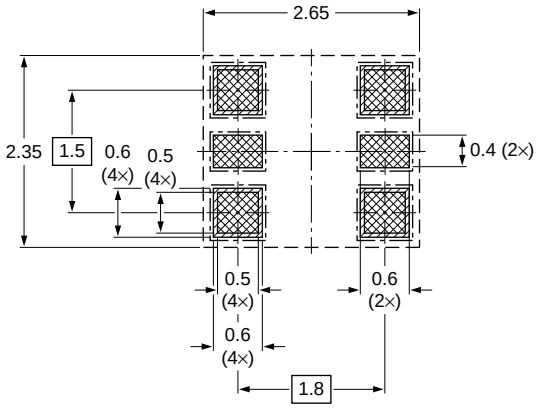


Fig 19. Reflow soldering footprint PUMD12 (SOT363)

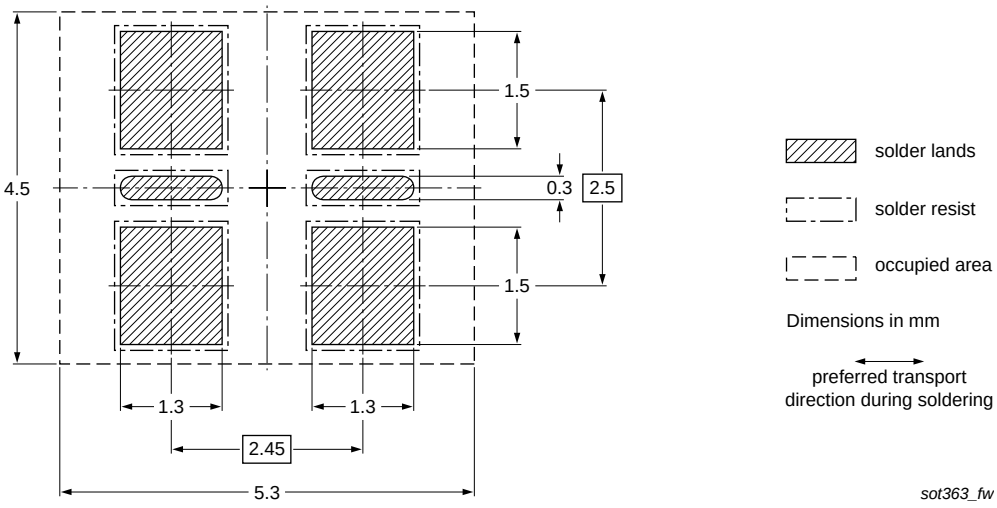


Fig 20. Wave soldering footprint PUMD12 (SOT363)

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12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMD12_PUMD12 v.4	20111121	Product data sheet	-	PEMD12_PUMD12 v.3
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 1 “Product profile”: updated • Section 4 “Marking”: updated • Figure 1 to 15: added • Section 6 “Thermal characteristics”: updated • Table 8 “Characteristics”: $V_{i(on)}$ redefined to $V_{I(on)}$ on-state input voltage, $V_{i(off)}$ redefined to $V_{I(off)}$ off-state input voltage, I_{CEO} updated, f_T added • Section 8 “Test information”: added • Section 9 “Package outline”: superseded by minimized package outline drawings • Section 10 “Packing information”: added • Section 11 “Soldering”: added • Section 13 “Legal information”: updated			
PEMD12_PUMD12 v.3	20031008	Product data sheet	-	PEMD12 v.2
PEMD12 v.2	20011107	Product specification	-	PEMD12 v.1
PEMD12 v.1	20010830	Preliminary specification	-	-
PUMD12 v.2	20010216	Product specification	-	PUMD12 v.1
PUMD12 v.1	19990426	Product specification	-	-

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13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 1
1.4 Quick reference data 1
2 Pinning information 2
3 Ordering information 2
4 Marking 2
5 Limiting values 3
6 Thermal characteristics 4
7 Characteristics 6
8 Test information 10
8.1 Quality information 10
9 Package outline 10
10 Packing information 10
11 Soldering 11
12 Revision history 13
13 Legal information 14
13.1 Data sheet status 14
13.2 Definitions 14
13.3 Disclaimers 14
13.4 Trademarks 15
14 Contact information 15
15 Contents 16

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