ESDA6V1-5W6

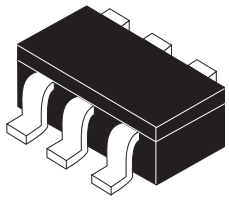
TRANSIL™ ARRAY FOR ESD PROTECTION

Application Specific Discretes
A.S.D.™

APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Other telephone sets
- Set top boxes



SOT323-6L

DESCRIPTION

The ESDA6V1-5W6 is a 5-bit wide monolithic suppressor which is designed to protect components connected to data and transmission lines against ESD.

FEATURES

- 5 UNIDIRECTIONAL TRANSIL™ FUNCTIONS
- BREAKDOWN VOLTAGE: VBR = 6.1V min
- LOW LEAKAGE CURRENT: I_R max < 1 µA
- VERY SMALL SIZE FOR PCB SPACE SAVING: 4.2mm^2 TYPICALLY

BENEFITS

- High integration
- Suitable for high density boards

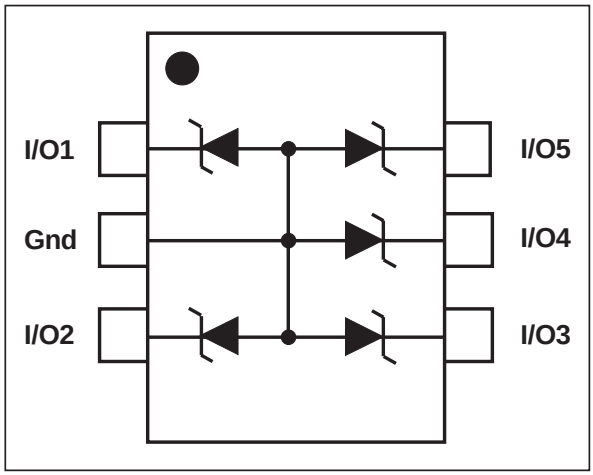
COMPLIES WITH THE FOLLOWING STANDARDS:

- IEC 61000-4-2: level 4

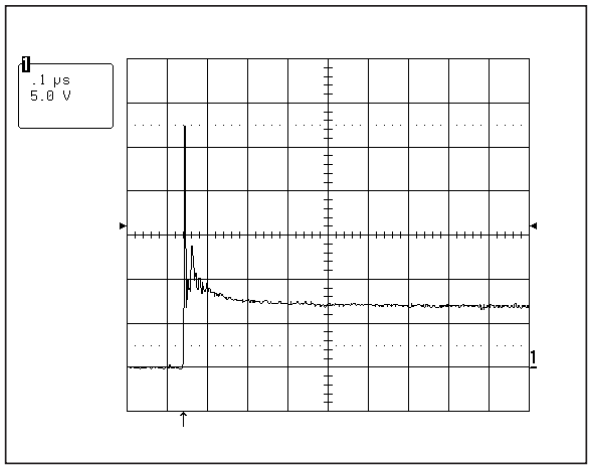
  15 kV (air discharge)
  8 kV (contact discharge)

- MIL STD 883C-Method 3015-6: class3
  (human body model)

FUNCTIONAL DIAGRAM



ESD response to IEC61000-4-2
(air discharge 16kV, positive surge)



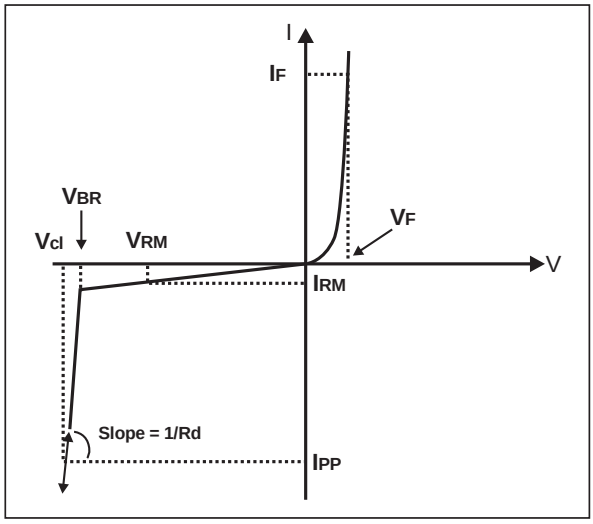
ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Symbol	Test conditions	Value	Unit
V_{PP}	ESD discharge - MIL STD 883C - Method 3015-6 IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge	25 20 15	kV
P_{PP}	Peak pulse power (8/20µs)	100	W
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature range	-55 to +150	°C
T_L	Lead solder temperature (10 seconds duration)	260	°C
T_{op}	Operating temperature range (note 1)	-40 to +125	°C

Note 1: The evolution of the operating parameters versus temperature is given by curves and αT parameter.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Capacitance
Rd	Dynamic impedance
V_F	Forward voltage drop



Type	V_{BR} @ I_R			I_{RM} @ V_{RM}		Rd	αT	C	V_F @ I_F	
	min.	max.		max.		typ. note 2	max. note 3	typ. 0V bias	max	
	V	V	mA	µA	V	mΩ	10^{-4}/°C	pF	V	mA
ESDA6V1-5W6	6.1	7.2	1	1	3	610	6	50	1.25	200

Note 2 : Square pulse, Ipp = 15A, tp=2.5µs.

Note 3: $\Delta V_{BR} = \alpha T * (T_{amb} - 25°C) * V_{BR}$ (25°C)

Fig. 1: Peak power dissipation versus initial junction temperature.

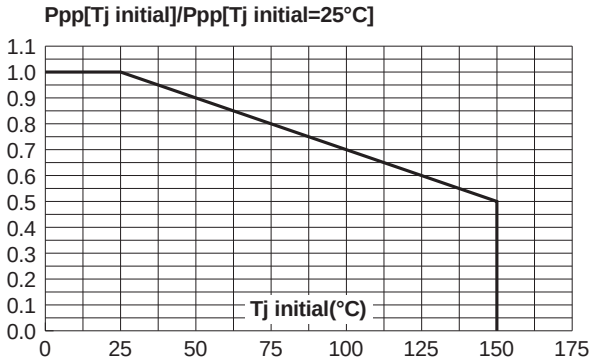


Fig. 2: Peak pulse power versus exponential pulse duration (Tj initial = 25°C).

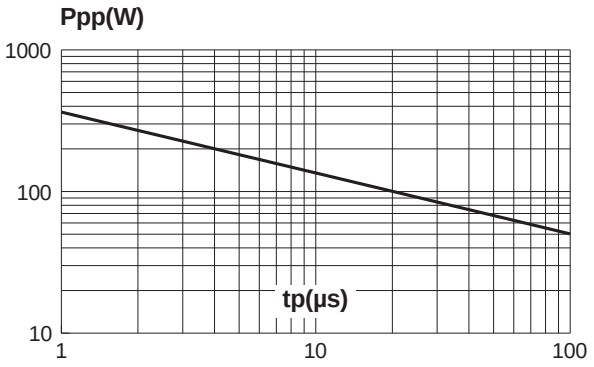


Fig. 3: Clamping voltage versus peak pulse current (Tj initial = 25°C) Rectangular waveform tp = 2.5µs.

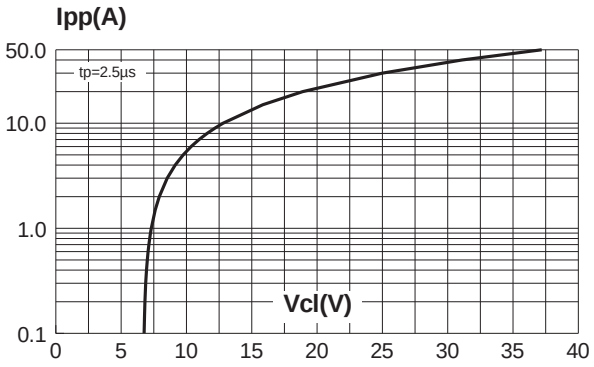


Fig. 4: Capacitance versus reverse applied voltage (typical values).

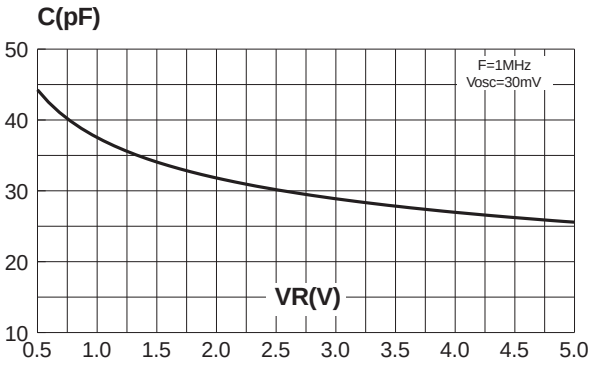


Fig. 5: Relative variation of leakage current versus junction temperature (typical values).

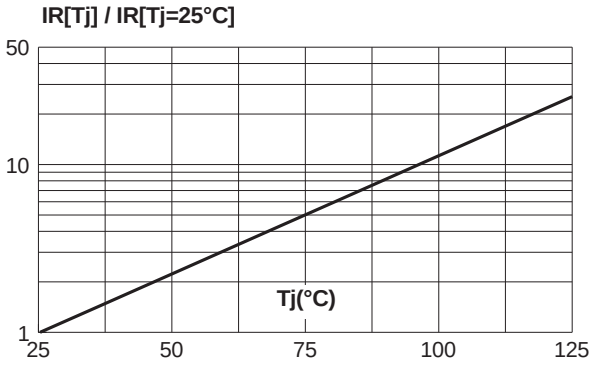
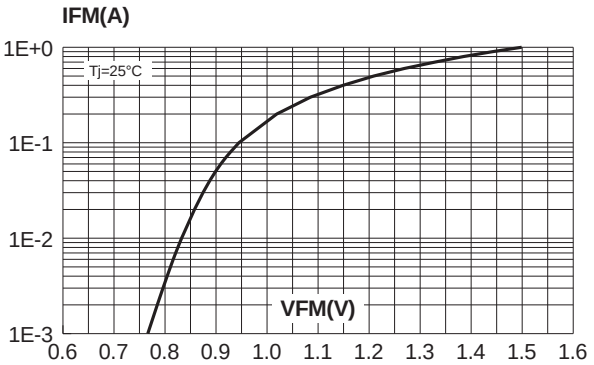
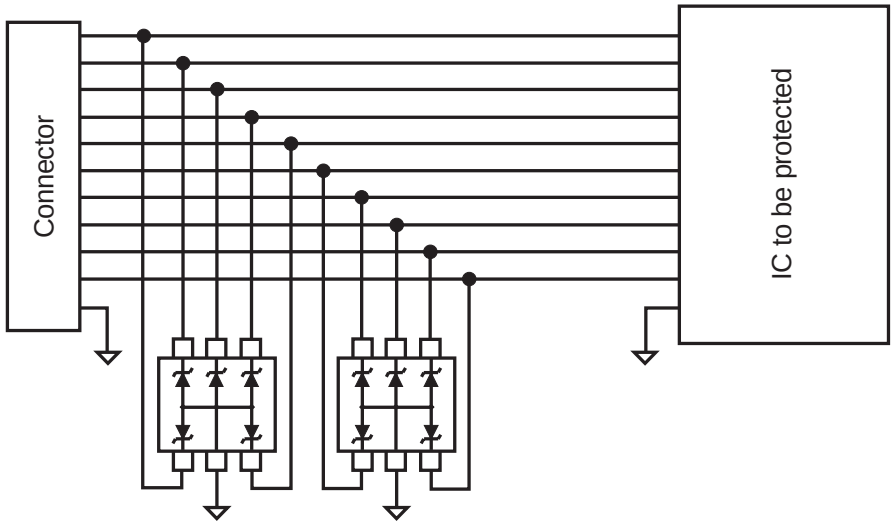


Fig. 6: Peak forward voltage drop versus peak forward current (typical values).



APPLICATION EXAMPLE



Implementation of ESDA6V1-5W6 in a typical application

TECHNICAL INFORMATION

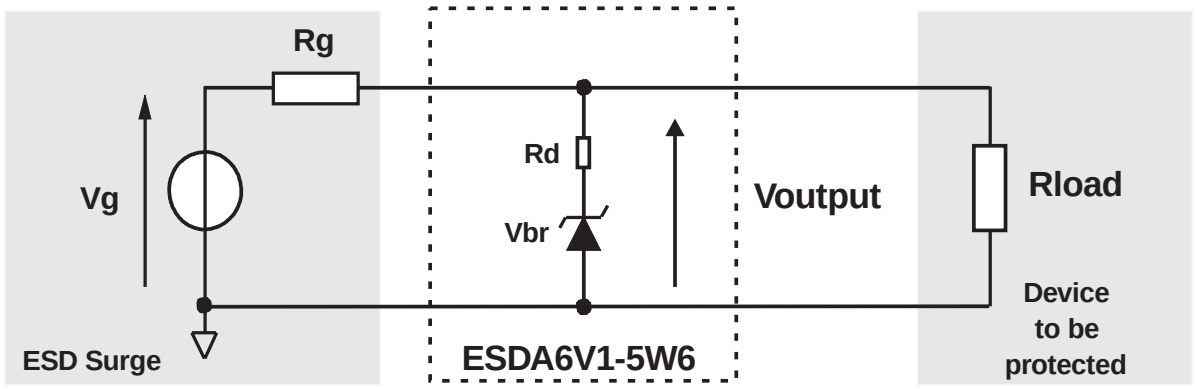
ESD PROTECTION

The **ESDA6V1-5W6** is particularly optimized to perform ESD protection. ESD protection is achieved by clamping the unwanted overvoltage. The clamping voltage is given by the following formula :

$$V_{cl} = V_{br} + R_d \cdot I_{pp}$$

As shown in figure A1, the ESD strikes are clamped by the transient voltage suppressor.

Fig. A1: ESD clamping behavior



To have a good approximation of the remaining voltages at both Vi/o side, we provide the typical dynamical resistance value Rd. By taking into account the following hypothesis :

Rg > Rd and Rload > Rd

we have:

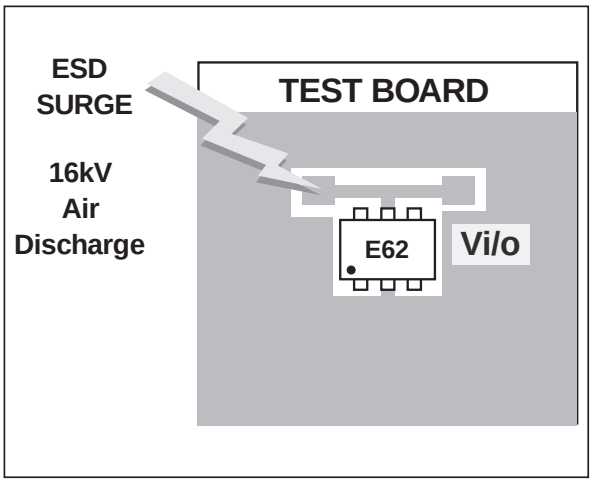
$$Vin = V_{br} + R_d \times \frac{V_g}{R_g}$$

The results of the calculation done for Vg = 8 kV, Rg = 330 Ω (IEC 61000-4-2 standard), Vbr = 6.4 V (typ.) and Rd = 0.61 Ω (typ.) give:

Vouput = 21.2 V

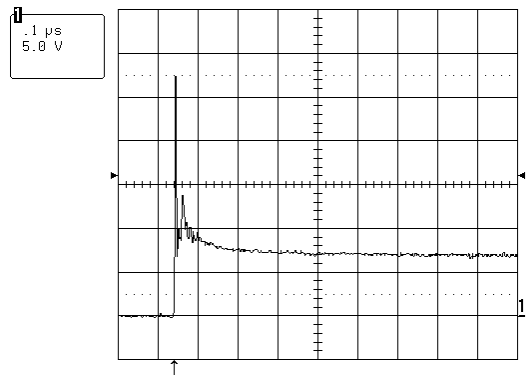
This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be a few tenths of volts during a few ns at the Vi/o side.

Fig. A2: Measurement conditions:

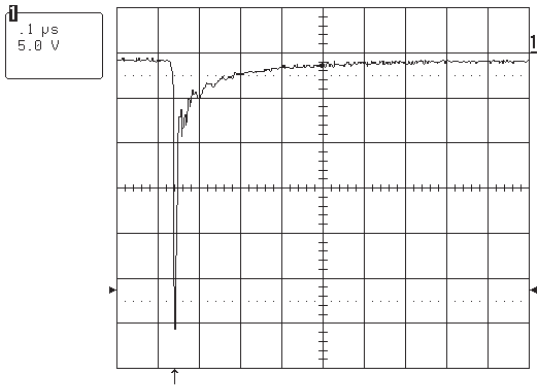


The measurements done here after show very clearly (Fig. A3) the high efficiency of the ESD protection: the clamping voltage Vout becomes very close to Vbr (positive way, Fig. A3a) and -Vf (negative way, Fig. A3b).

Fig. A3: Remaining voltage during ESD surge



a: Vi/o during positive surge

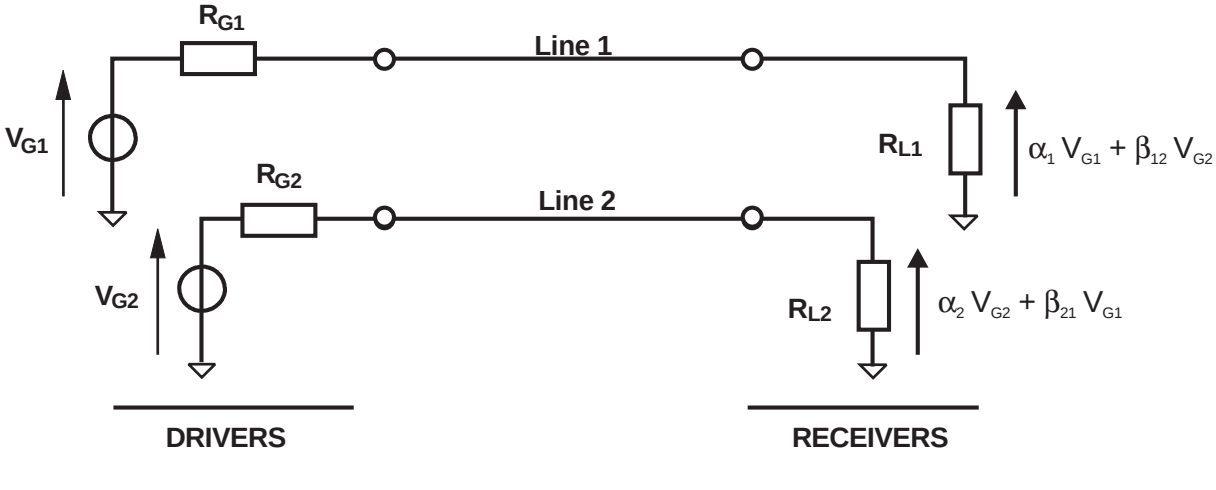


b: Vi/o during negative surge

One can note that the **ESDA6V1-5W6** is not only acting for positive ESD surges but also for negative ones. For these kind of disturbances it clamps close to ground voltage as shown in Fig. A3b.

CROSSTALK BEHAVIOR

Fig. A4: Crosstalk phenomenon



The crosstalk phenomena are due to the coupling between 2 lines. The coupling factor (β_{12} or β_{21}) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G1}$. In fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Fig. A5: Analog crosstalk measurements

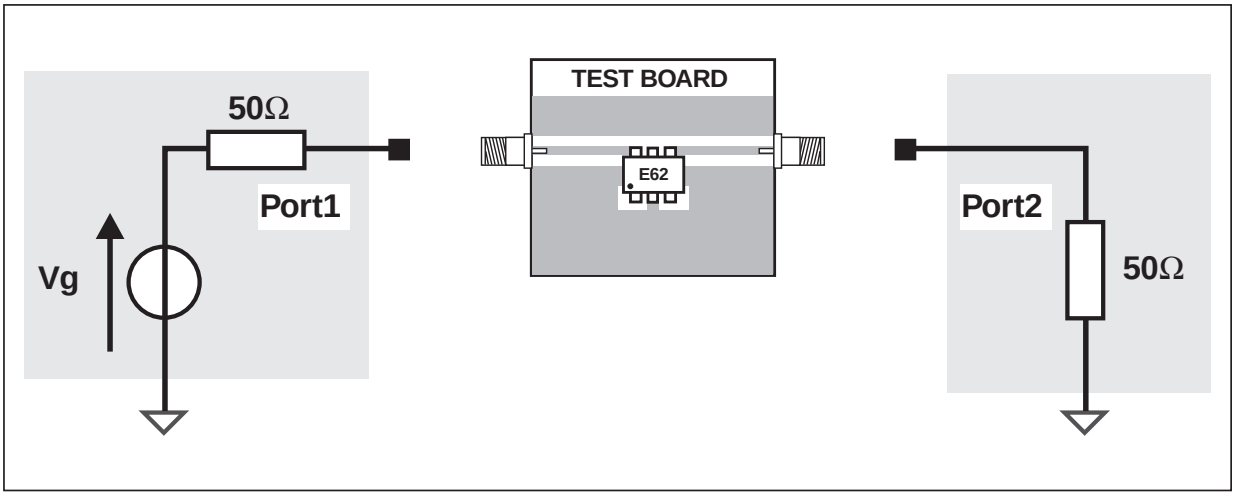


Fig. A6: Typical analog crosstalk measurements

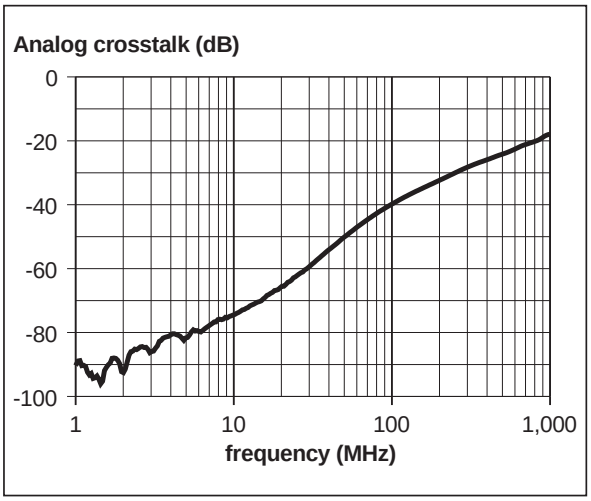


Figure A5 gives the measurement circuit for the analog crosstalk application. In figure A6, the curve shows the effect of the cell I/O5 on the cell I/O3. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -40dB.

Fig. A7: Digital crosstalk measurements configuration

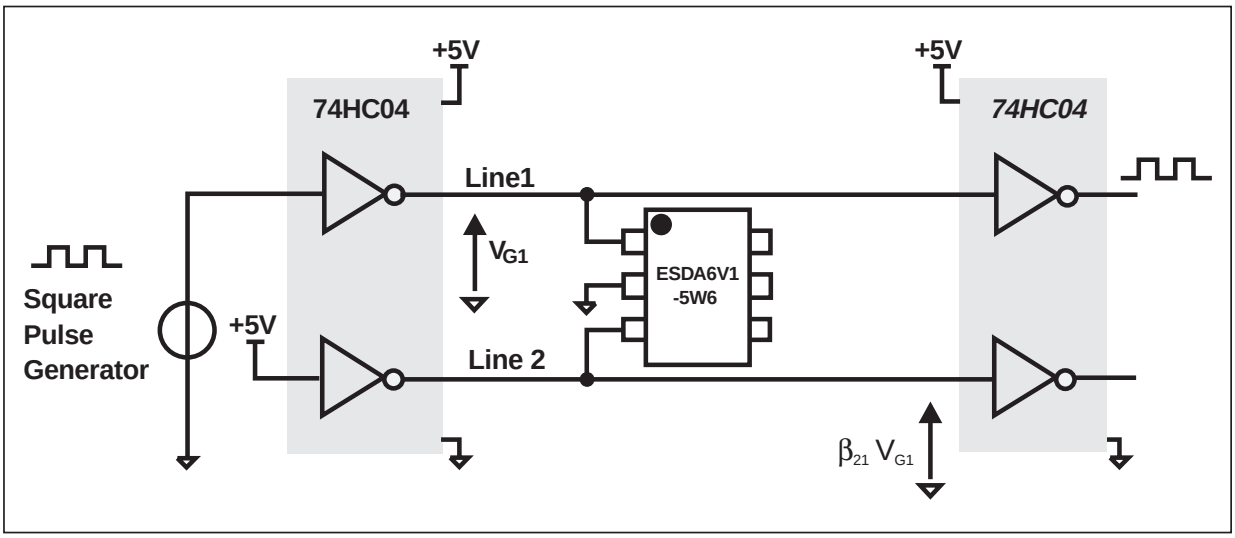


Fig. A8: Digital crosstalk measurements configuration

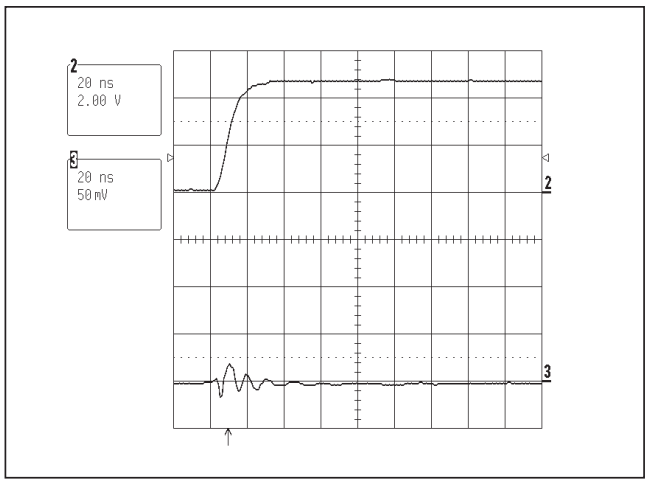
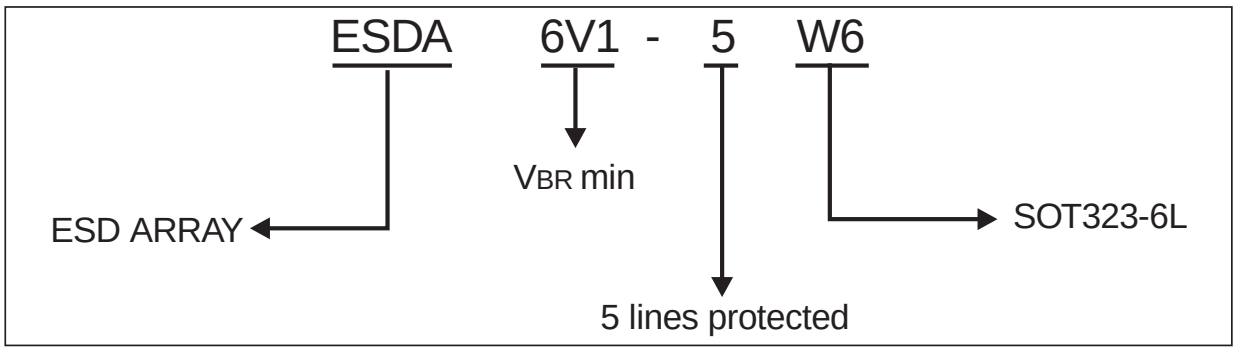


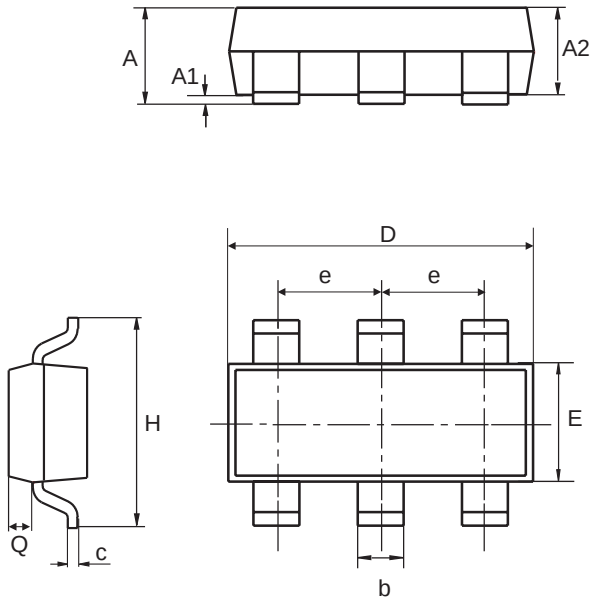
Figure A7 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.
Figure A8 shows that in such a condition, i.e signal from 0 to 5V and rise time of a few ns, the impact on the disturbed line is less than 50 mV peak to peak. No data disturbance was noted on the concerned line. The measurements performed with falling edges give an impact within the same range.

ORDER CODE



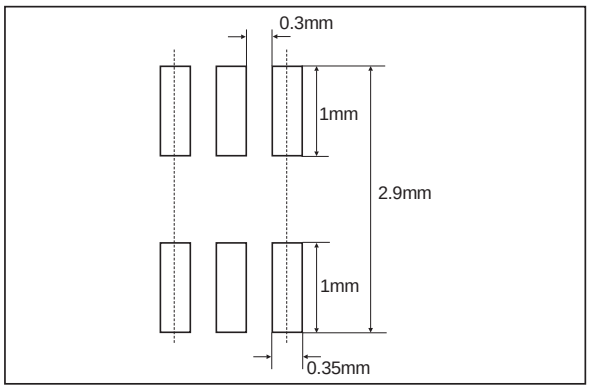
PACKAGE MECHANICAL DATA

SOT323-6L



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.8	1.1	0.031	0.043
A1	0	0.1	0	0.004
A2	0.8	1	0.031	0.039
b	0.15	0.3	0.006	0.012
c	0.1	0.18	0.004	0.007
D	1.8	2.2	0.071	0.086
E	1.15	1.35	0.045	0.053
e	0.65 Typ.		0.025 Typ.	
H	1.8	2.4	0.071	0.094
Q	0.1	0.4	0.004	0.016

FOOT PRINT



MARKING

Type	Marking	Package	Weight	Base Qty	Delivery mode
ESDA6V1-5W6	E62	SOT323-6L	5.4 mg	3000	Tape & Reel

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