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Description

The AP6508 is a 500kHz switching frequency internal compensated synchronous DCDC buck converter. It has integrated compensation, and low R_{DSON} high and low side MOSFETs.

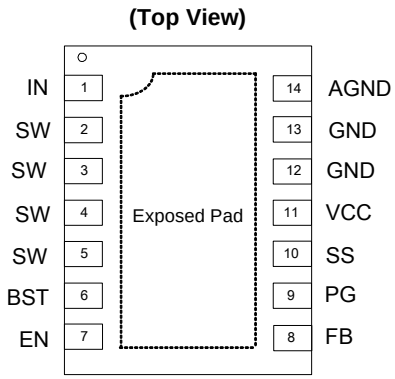
The AP6508 enables continues load current of up to 3A with efficiency as high as 93%.

The AP6508 features current mode control operation, which enables fast transient response times and easy loop stabilization.

The AP6508 has external programmable softstart and a Power Good indicator enabling sequencing and ramp control.

The AP6508 simplifies board layout and reduces space requirements with its high level of integration and minimal need for external components, making it ideal for distributed power architectures.
The AP6508 is available in a standard Green DFN4030-14 package with exposed PAD for improved thermal performance and is RoHS compliant.

Pin Assignments



DFN4030-14

Features

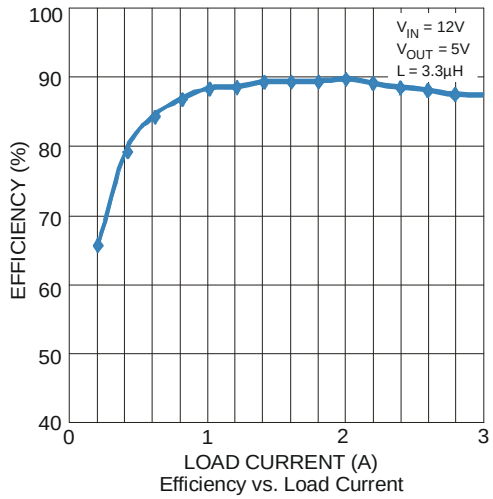
- V_{IN} 4.5V to 21V
- V_{OUT} adjustable to 0.8V
- 500kHz switching frequency
- Enable pin
- External Softstart
- Power Good
- Protection
  - o OCP
  - o Thermal Shutdown
- Lead Free Finish/ RoHS Compliant (Note 1)

Applications

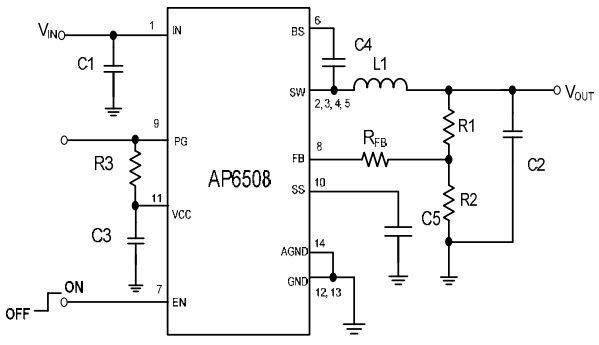
- Gaming Consoles
- TV sets and Monitors
- Set Top Boxes
- Distributed power systems
- Home Audio
- Consumer electronics

Note: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

Typical Application Circuit



Efficiency vs. Load Current



Typical Application Circuit

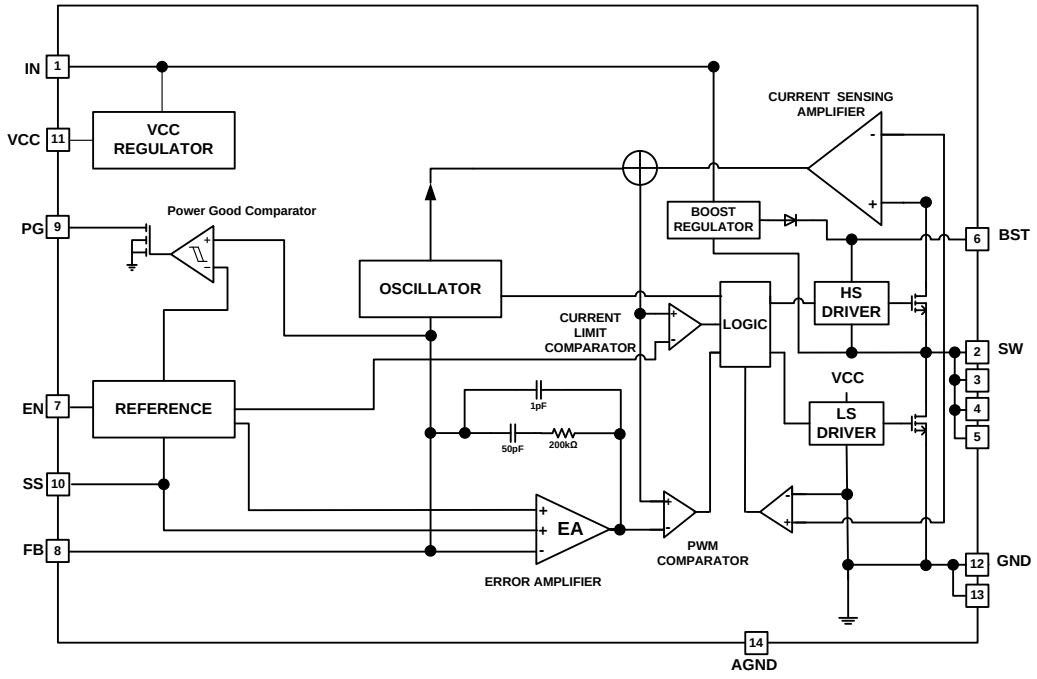
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Pin Descriptions

Pin #	Name	Description
1	IN	Supply Voltage. The AP6508 operates from a 4.5V to 21V input rail. C1 is needed to decouple the input rail. Use wide PCB trace to make the connection.
2,3,4,5	SW	Switch Output. Use wide PCB trace to make the connection.
6	BST	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
7	EN	EN=1 to enable the chip. For automatic start-up, connect EN pin to VIN by proper EN resistor divider as Figure 1 shows.
8	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 500mV.
9	PG	Power Good
10	SS	External Softstart
11	V_{CC}	BIAS Supply. Decouple with 0.µ1F – 0.22µF cap. And the capacitance should be no more than 0.22µF
12, 13	GND	System Ground. This pin is the reference ground for the regulated output voltage. For this reason care must be taken in its PCB layout. Suggested to be connected to GND with copper and vias.
14	AGND	Analog Ground
	Exposed PAD	No internal connection. It is recommended to connect exposed pad to GND plane for optimal thermal performance

Functional Block Diagram



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Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	22	V
V_{SW}	Switch Node Voltage	-0.3 to 23	V
V_{BS}	Bootstrap Voltage	VSW + 6	V
V_{FB}	Feedback Voltage	–0.3V to +6	V
V_{EN}	Enable/UVLO Voltage	–0.3V to +6	V
V_{COMP}	Comp Voltage	–0.3V to +6	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 3)			
HBM	Human Body Model	3	kV
MM	Machine Model	300	V

Thermal Resistance (Note 4)

Symbol	Parameter	Rating	Unit
θ_{JA}	Junction to Ambient	52	°C/W
θ_{JC}	Junction to Case	11	°C/W

Recommended Operating Conditions (Note 5)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	4.5	21	V
T_A	Operating Ambient Temperature Range	-40	+85	°C

Notes:
2. Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
3. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these device.
4. Test condition for SO-8EP: Device mounted on 2"*2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
5. The device function is not guaranteed outside of the recommended operating conditions.

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Electrical Characteristics (V_{IN} = 12V, T_A = +25°C, unless otherwise noted)

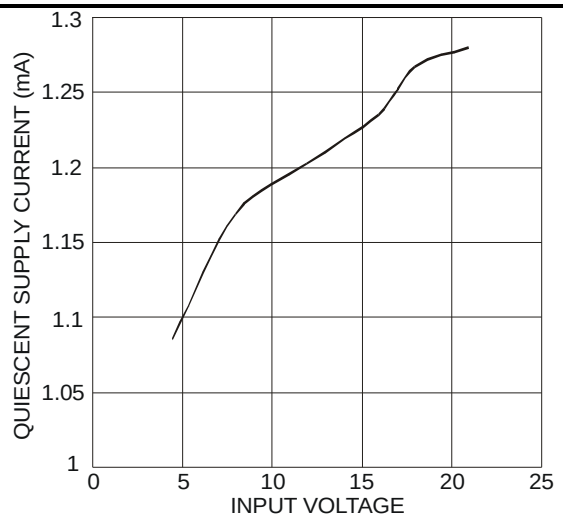
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_{IN}	Shutdown Supply Current	V_{EN} = 0V		0		μA
I_{IN}	Supply Current (Quiescent)	V_{EN} = 2.0V, V_{FB} = 1.0V		1.2		mA
$R_{DS(ON)1}$	High-Side Switch On-Resistance (Note 6)			120		mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance (Note 6)			20		mΩ
SW_{LKG}	Switch Leakage Current	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
I_{Limit}	Current Limit			5.8		A
F_{SW}	Oscillator Frequency	V_{FB} = 0.75V	350	500	650	kHz
F_{FB}	Fold-back Frequency	V_{FB} = 300mV		0.3		f_{SW}
D_{MAX}	Maximum Duty Cycle	V_{FB} = 700mV	80	85		%
V_{FB}	Feedback Voltage	T_A = -40°C to +85°C	791	807	823	mV
I_{FB}	Feedback Current	V_{FB} = 800mV		10	50	nA
V_{EN_Rising}	EN Rising Threshold		1.1	1.3	1.5	V
V_{EN_HYS}	EN Threshold Hysteresis			0.4		V
I_{EN}	EN Input Current	V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
EN_{TD-Off}	EN Turn Off Delay (Note 6)			5		μs
PG_{Vth-Hi}	Power Good Rising Threshold			0.9		V_{FB}
PG_{Vth-Lo}	Power Good Falling Threshold			0.7		V_{FB}
PG_{TD}	Power Good Delay			20		μs
V_{PG}	Power Good Sink Current Capability			0.4		V
I_{PG_LEAK}	Power Good Leakage Current				50	nA
I_{SS}	Soft-Start Current			10.5		μA
$INUV_{Vth}$	V_{IN} Under Voltage Threshold Rising		4.0	4.2	4.4	V
$INUV_{HYS}$	V_{IN} Under Voltage Threshold Hysteresis			200		mV
V_{CC}	V_{CC} Regulator			5		V
	V_{CC} Load Regulation	Icc=5mA		5		%
T_{SD}	Thermal Shutdown			140		°C

Note: 6. Guaranteed by design

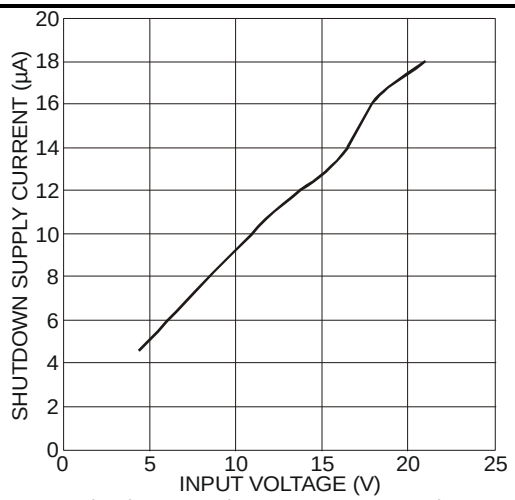
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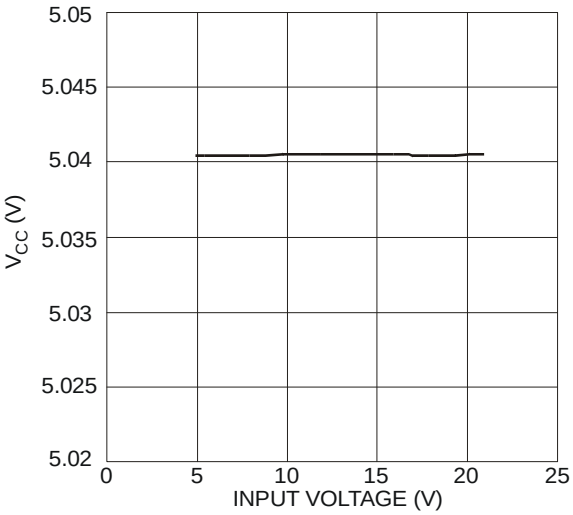
Typical Performance Characteristics



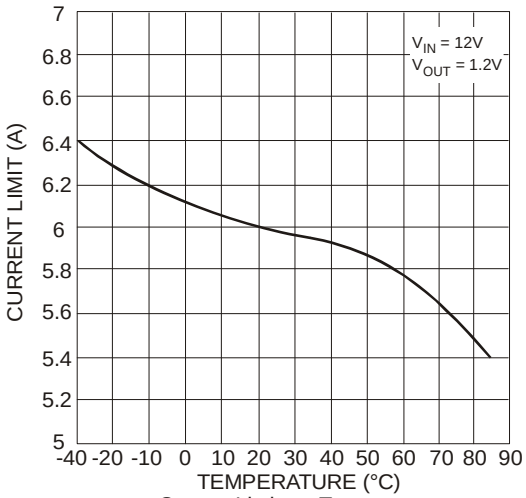
Quiescent Supply Current vs. Input Voltage



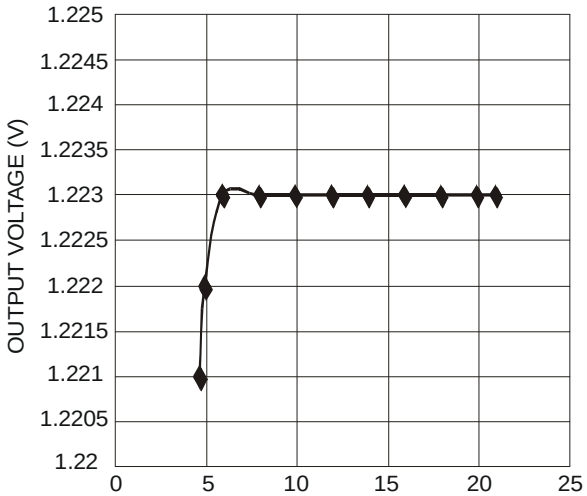
Shutdown Supply Current vs. Input Voltage



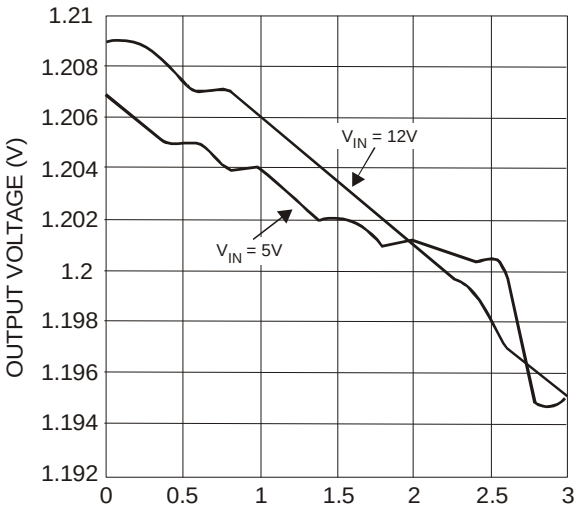
V_{CC} Regulator Line Regulation



Current Limit vs. Temperature



Line Regulation vs. Output Current

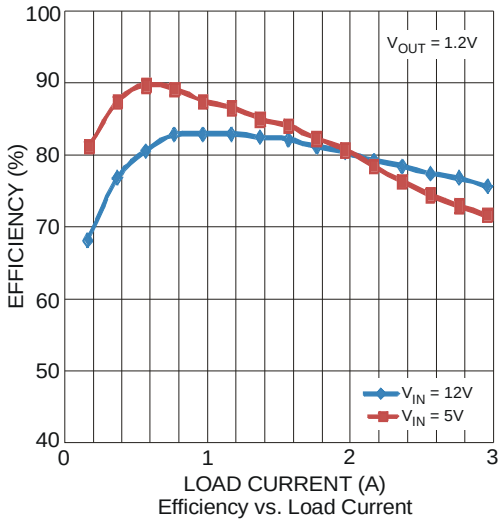


Load Regulation vs. Output Current

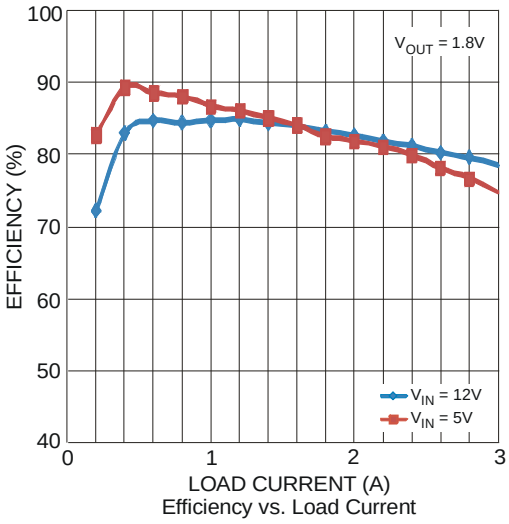
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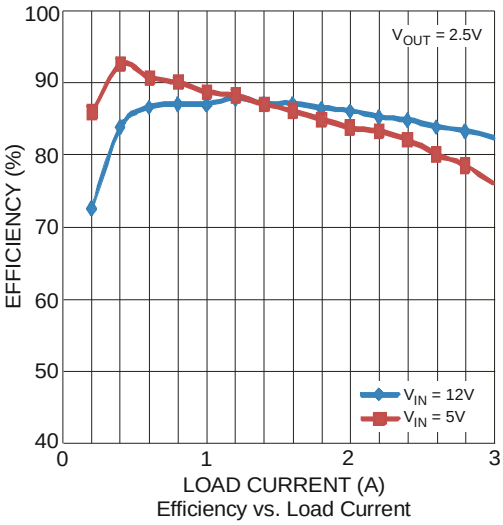
Typical Performace Characteristics (cont.)



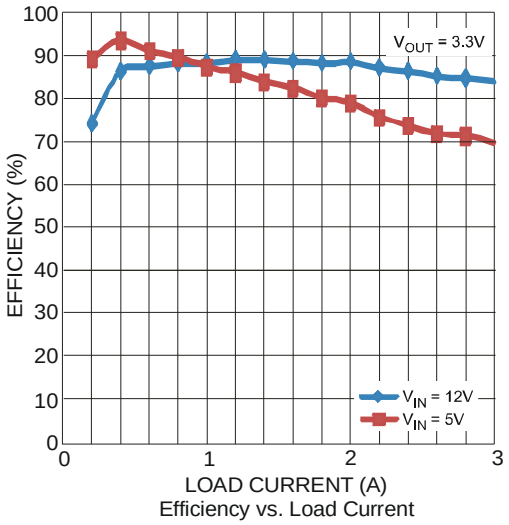
Efficiency vs. Load Current



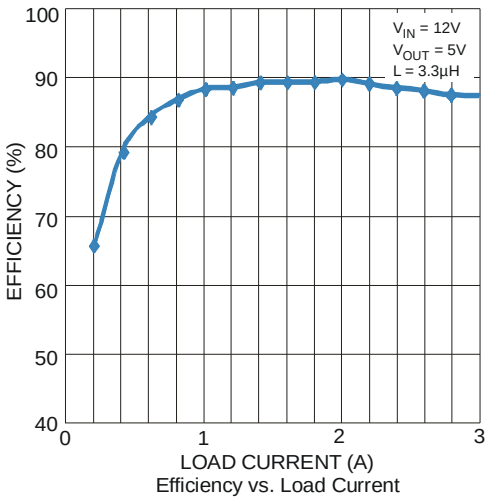
Efficiency vs. Load Current



Efficiency vs. Load Current



Efficiency vs. Load Current



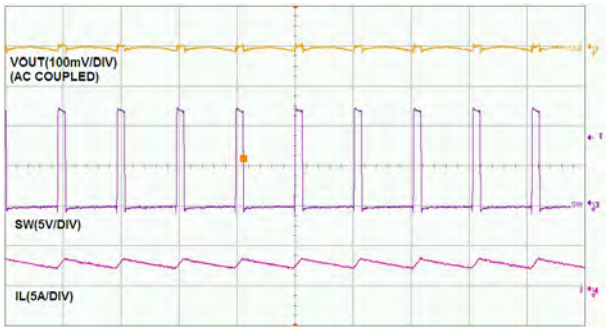
Efficiency vs. Load Current

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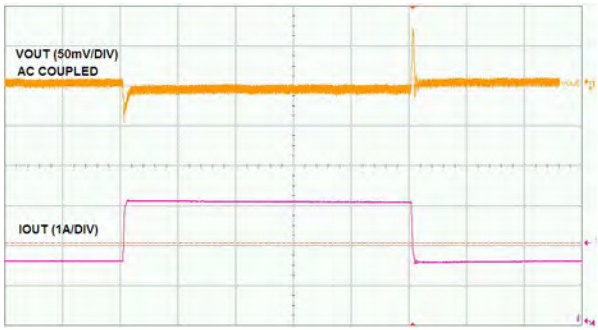
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Typcal Performance Characteristics

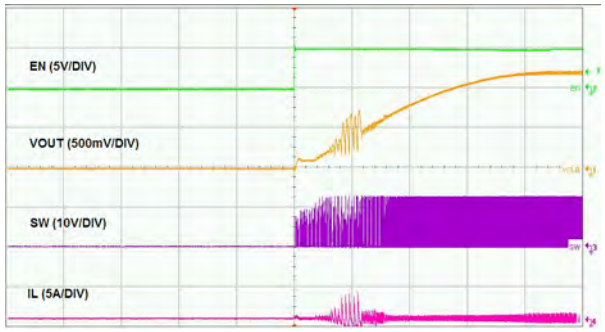
V_{IN} = 12V, V_{OUT} = 1.2V, L = 3.3µH, C1 = 22µF, C2 = 47µF, T_A = +25°C, unless otherwise noted.



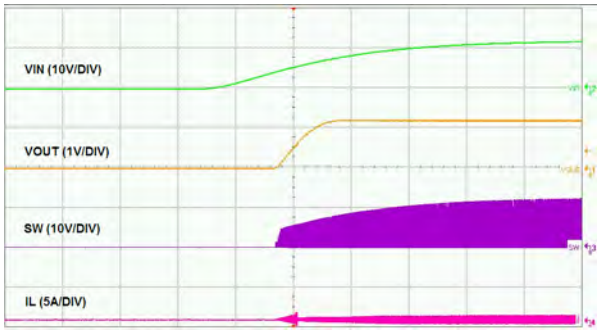
Time- 2µs/div
Steady State Test
I_{OUT} = 3A



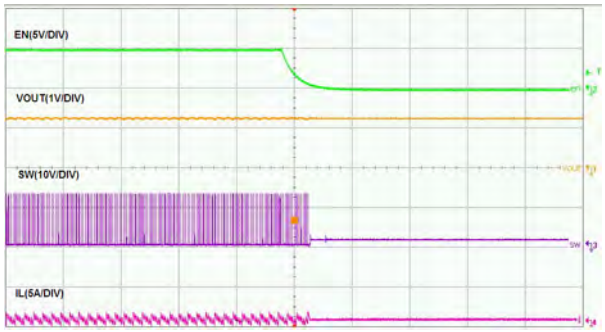
Time- 200µs/div
Load Transient Test
I_{OUT} = 1.5A to 3A. Step at 0.8A/µs



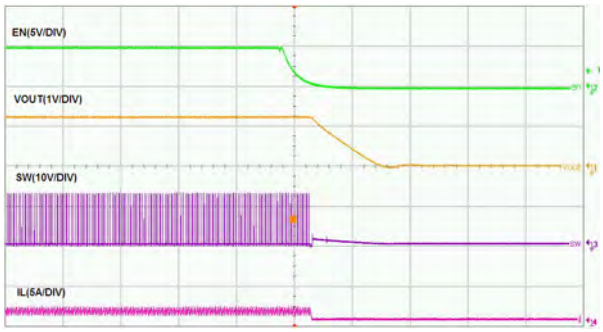
Time- 500µs/div
Start-up Through Enable (No Load)



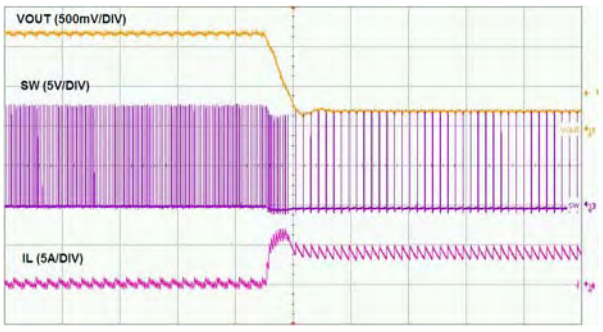
Time- 2ms/div
Start-up through V_{IN} (No load)



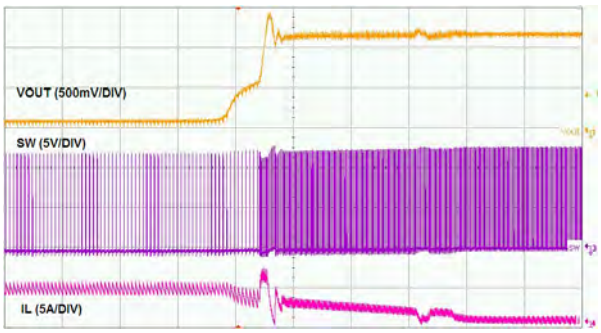
Time- 50µs/div
Shutdown Through Enable (No Load)



Time- 50µs/div
Shutdown Through Enable (Iout =1A)



Time- 50µs/div
Short Circuit Entry



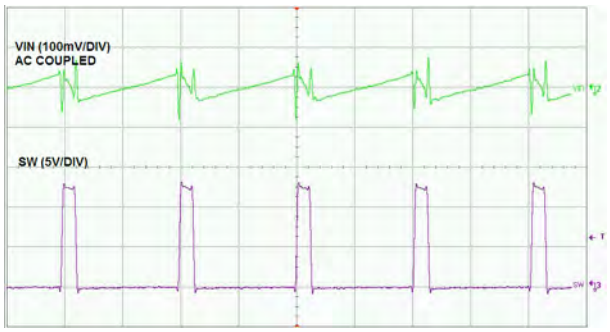
Time- 100µs/div
Short Circuit Recovery

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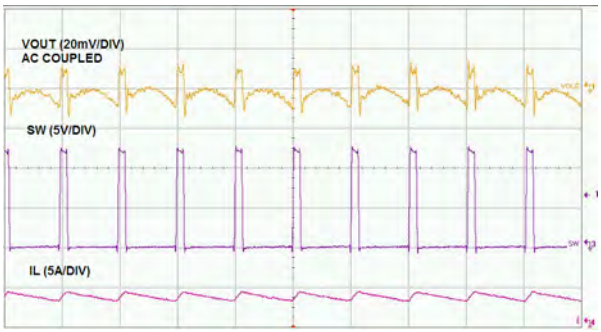
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Typcal Performance Characteristics

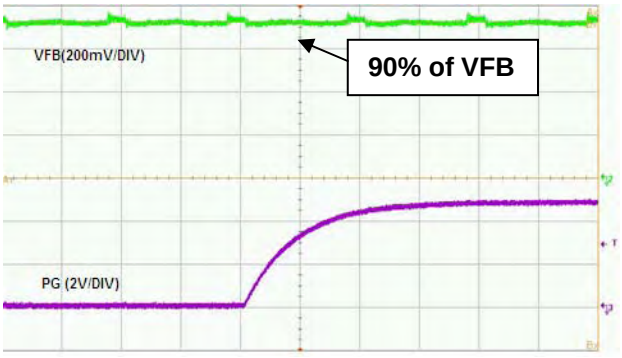
V_{IN} = 12V, V_{OUT} = 1.2V, L = 3.3µH, C1 = 22µF, C2 = 47µF, T_A = +25°C, unless otherwise noted.



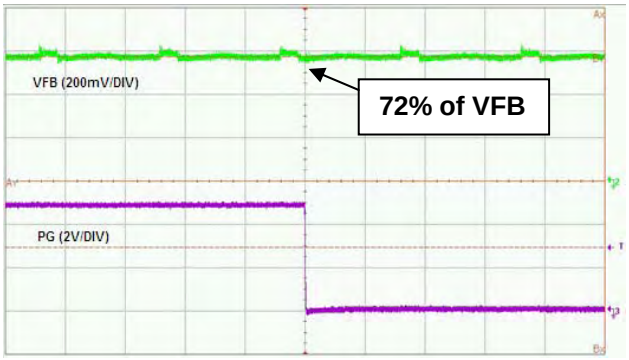
Time- 1µs/div
Input Voltage Ripple



Time- 2µs/div
Output Voltage Ripple



Time- 1us/div
Powergood Rising Threshold



Time- 1µs/div
Powergood FallingThreshold

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Application Information

Theory of Operation

The AP6508 is a 3A current mode, synchronous buck regulator with built in power MOSFETs. current mode control assures excellent line and load regulation and a wide loop bandwidth for fast response to load transients. Figure. 2 depicts the functional block diagram of AP6508.

The operation of one switching cycle can be explained as follows. At the beginning of each cycle, HS (high-side) MOSFET is off. The EA output voltage is higher than the current sensing amplifier output, and the current comparator's output is low. The rising edge of the 500kHz oscillator clock signal sets the RS Flip-Flop. Its output turns on HS MOSFET. The current sensing amplifier is reset for every switching cycle.

When the HS MOSFET is on, inductor current starts to increase. The current sensing amplifier senses and amplifies the inductor current. Since the current mode control is subject to sub-harmonic oscillations that peak at half the switching frequency, slope compensation is utilized. This will help to stabilize the power supply. This slope compensation is summed to the current sensing amplifier output and compared to the error amplifier output by the PWM comparator. When the sum of the current sensing amplifier output and the slope compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and HS MOSFET is turned off.

For one whole cycle, if the sum of the current sensing amplifier output and the slope compensation signal does not exceed the EA output, then the falling edge of the oscillator clock resets the flip-flop. The output of the error amplifier increases when feedback voltage (VFB) is lower than the reference voltage of 0.807V. This also increases the inductor current as it is proportional to the EA voltage.

When the HS MOSFET turns off, the synchronous LS MOSFET turns on until the next clock cycle begins. There is a "dead time" between the HS turn off and LS turn on that prevents the switches from "shooting through" from the input supply to ground.

The voltage loop is internally compensated with the 50pF and 200kΩ RC network. The maximum EAMP voltage output is precisely clamped at 2.1V.

Internal Regulator

Most of the internal circuitry including the bottom driver are powered from the 5V internal regulator. When Vin is less than 5V, this internal regulator cannot maintain the 5V regulation and hence the output voltage would also drop from regulation.

Enable

The enable (EN) input allows the user to control turning on or off the converter. To enable the converter EN must be pulled above the 'EN Rising Threshold' and to disable the converter EN must be pulled below 'EN falling Threshold' (EN rising threshold – EN threshold Hysteresis).

Few conditions on EN function:
1) EN must be pulled low for at least 5us to disable the regulator.
2) The voltage on EN cannot exceed 5V.
3) The AP6508 can be enabled by Vin through a voltage divider as shown in the figure 1 below.

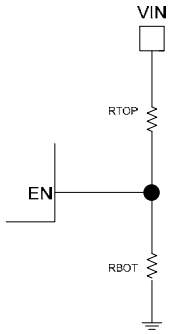


Figure 1. EN Divider Network

$$V_{IN-RISE} = V_{EN-RISE} \frac{(R_{TOP} + R_{BOT} \,||\, 1M\Omega}{R_{BOT} \,||\, 1M\Omega}$$

Where $V_{EN-RISE}$ = 1.3V(TYP)

$$V_{IN-FALL} = V_{EN-FALL} \frac{(R_{TOP} + R_{BOT} \,||\, 1M\Omega}{R_{BOT} \,||\, 1M\Omega}$$

Where $V_{EN-FALL}$ = 0.9V(TYP)

Power Good

Power Good (PGOOD) is an open drain and active high output. This output can be pulled up high to the appropriate level with an external resistor. The PGOOD is flagged low when Vfb=0.7V and is an open drain output when Vfb=0.9V. The PGOOD output can deliver a max of 4 mA sink current at 0.4 V when de- asserted. The PGOOD pin is held low during soft-start. Once output voltage reaches 90% of its final value, PGOOD goes high if there are no faults.

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Application Information (cont.)

External Soft Start

Soft start is traditionally implemented to prevent the excess inrush current. This in turn prevents the converter output voltage from overshooting when it reaches regulation. The AP6508 has an internal current source with a soft start capacitor to ramp the reference voltage from 0V to 0.807V. The soft start time is internally fixed at 2ms (TYP). The soft start time can be extended > 2ms by adding a soft start capacitor externally. The soft start sequence is reset when there is a thermal shutdown, Under Voltage Lockout (UVLO) or when the part is disabled using the EN pin.

External soft start can be calculated from the formula below:

$$I_{SS} = C * \frac{DV}{DT}$$

Where;

Iss = Soft Start Current

C = External Capacitor

DV=change in feedback voltage from 0V to maximum voltage

DT = Soft Start Time

Current Limit Protection

The AP6508 has cycle-by-cycle current limiting implementation. The voltage drop across the internal HS MOSFET is sensed and compared with the internally set current limit threshold. This voltage drop is sensed at about 30ns after the HS turns on. This voltage drop is proportional to the peak inductor current. When the peak inductor current exceeds the set current limit threshold, current limit protection is activated. During this time the feedback voltage (VFB) drops down. When the voltage at the FB pin reaches 0.3V, the internal oscillator shifts the frequency from the normal operating frequency of 500kHz to a fold-back frequency of 150kHz. The current limit is reduced to 70% of nominal current limit when the part is operating at 150kHz. This low fold-back frequency prevents current runaway.

Under Voltage Lockout (UVLO)

Under Voltage Lockout is implemented to prevent the IC from operating under insufficient input voltages. The AP6508 has a UVLO comparator that monitors the input voltage and internal bandgap reference. If the input voltage falls below 3.8V, the AP6508 will latch an under voltage fault. In this event the AP6508 will be disabled and power has to be re-cycled to reset the UVLO fault.

Thermal Shutdown

The AP6508 has on-chip thermal protection that prevents damage to the IC when the die temperature exceeds safe margins. It implements a thermal sensing to monitor the operating junction temperature of the IC. Once the die temperature rises to approximately 140°C, the thermal protection feature gets activated .The internal thermal sense circuitry turns the IC off thus preventing the power switch from damage.

A hysteresis in the thermal sense circuit allows the device to cool down to approximately 120°C before the IC is enabled again through soft start. This thermal hysteresis feature prevents undesirable oscillations of the thermal protection circuit.

Setting the Output Voltage

The output voltage can be adjusted from 0.807V to 15V using an external resistor divider. Table 1 shows a list of resistor selection for common output voltages. Resistor R1 is selected based on a design tradeoff between efficiency and output voltage accuracy. For high values of R1 there is less current consumption in the feedback network. However the trade off is output voltage accuracy due to the bias current in the error amplifier. R2 can be determined by the following equation:

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{0.807} - 1 \right)$$

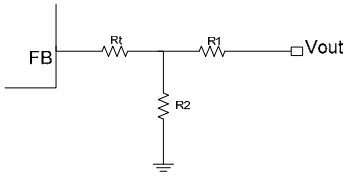


Figure 2. Feedback Divider Network

When output voltage is low, a T-type network as shown in Figure 2 is recommended.

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	R_t (kΩ)
1.2	4.99	10.2	24.9
1.8	4.99 (1%)	4.02 (1%)	35.7
2.5	40.2 (1%)	19.1 (1%)	24.9
3.3	40.2 (1%)	13 (1%)	24.9
5	40.2 (1%)	7.68 (1%)	35.7

Table 1.Resistor Selection for Common Output Voltages

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value;

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{SW}}$$

Where ΔI_L is the inductor ripple current.

And f_{SW} is the buck converter switching frequency.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

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Application Information (cont.)

Inductor (cont.)

Peak current determines the required saturation current rating, which influences the size of the inductor.

Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence choosing an inductor with appropriate saturation current rating is important.

A 1µH to 10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications.

For highest efficiency, the inductor's DC resistance should be less than 200mΩ. Use a larger inductance for improved efficiency under light load conditions.

Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on time on the upper MOSFET. It must hence have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has an RMS rating that is greater than half of the maximum load current.

Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur. For most applications, a 4.7µF ceramic capacitor is sufficient.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshoot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

Maximum capacitance required can be calculated from the following equation:

$$C_o = \frac{L(I_{out} + \frac{\Delta I_{inductor}}{2})^2}{(\Delta V + V_{out})^2 - V_{out}^2}$$

Where ΔV is the maximum output voltage overshoot.

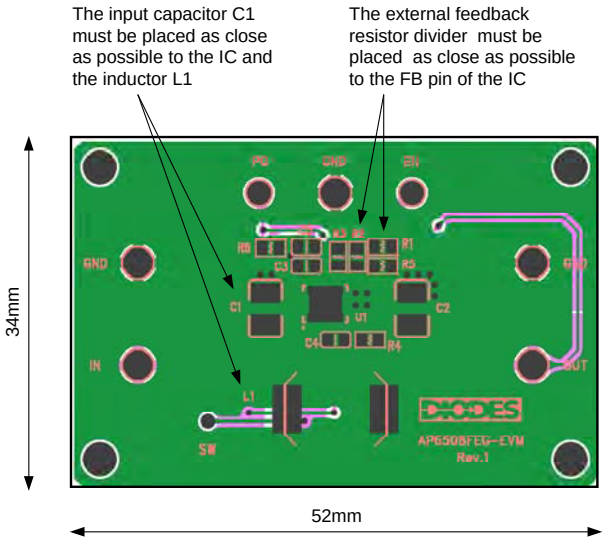
ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated from the equation below:

$$Vout_{capacitor} = \Delta I_{inductor} * ESR$$

An output capacitor with ample capacitance and low ESR is the best option. For most applications, a 22µF ceramic capacitor will be sufficient.

PC Board Layout

This is a high switching frequency converter. Hence attention must be paid to the switching currents interference in the layout. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces.



AP6508 is exposed at the bottom of the package and must be soldered directly to a well designed thermal pad on the PCB. This will help to increase the power dissipation.

External Bootstrap Diode

It is recommended that an external bootstrap diode be added when the input voltage is lower than or equal to 5V and the duty cycle is greater than 65%. This external diode can be connected to the input or a 5V rail that is available in the system. This helps improve the efficiency of the converter. The bootstrap diode can be a low cost one such as BAT54 or a Schottky that has a low Vf.

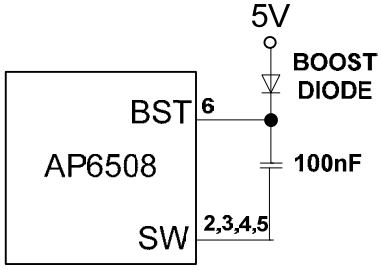


Figure 3. External Bootstrap Diode

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Ordering Information

AP6508 FE - 13

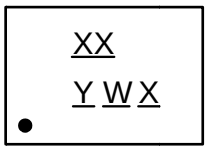
Package	Packing
FE : DFN4030	13 : Tape & Reel

Device	Package Code	Packaging (Note 7)	13" Tape and Reel	
			Quantity	Part Number Suffix
AP6508FE-13	FE	DFN4030-14	3000/Tape & Reel	-13

Note: 7. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

Marking Information

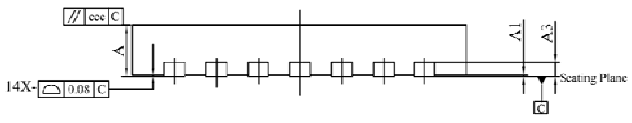
(Top View)



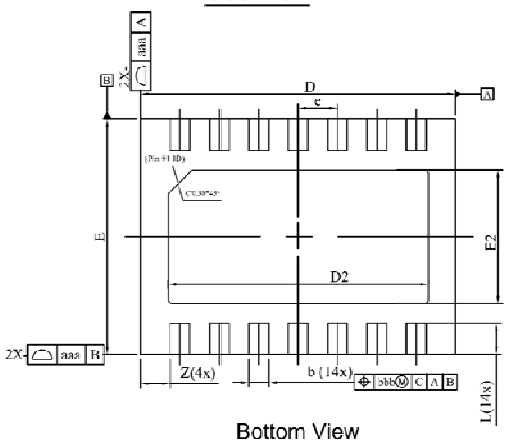
XX : E8 : AP6508
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week;
z : represents 52 and 53
X : A~Z : Green

Part Number	Package	Identification Code
AP6508FE	DFN4030-14	E8

Package Outline Dimensions (All Dimensions in mm)



Side View



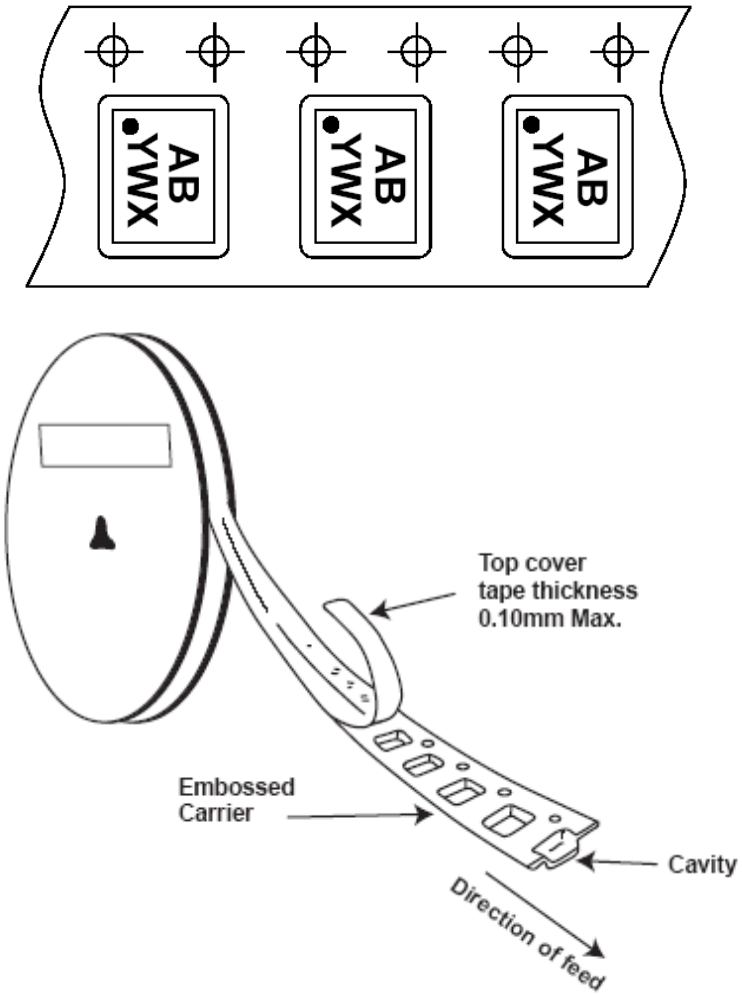
Bottom View

Dim	Min	Max	Typ
D	3.95	4.05	4.00
E	2.95	3.05	3.00
D2	3.20	3.40	3.30
E2	1.60	1.80	1.70
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	—	—	0.15
b	0.20	0.30	0.25
L	0.35	0.45	0.40
e	—	—	0.50
Z	—	—	0.375
aaa	0.25		
bbb	0.10		
ccc	0.10		

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Tape Orientation (Note 8)



Note: 8. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf

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