Programmable Output Voltage Single Synchronous Buck Controller

General Description

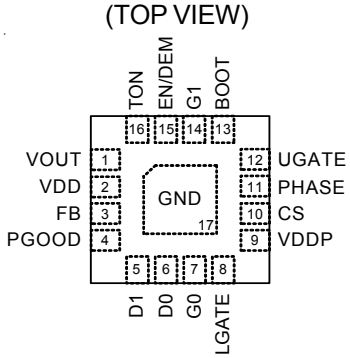
The RT8208A/B is a constant-on-time PWM controller which provides four resistor programmable DC output voltages by controlling the G0 and G1 digital input. The output voltage is programmable from 0.75V to 3.3V. The RT8208A/B offers the lowest total solution cost in systems where need output voltage slewing. The RT8208A/B provides an automatic masking power good output during output voltage transition.

The constant-on-time PWM control scheme handles wide input/output ratios with ease and provides 100ns "instant-on" response to load transient while maintaining a relatively constant frequency. It provides the high efficiency, excellent transient response, and DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, graphics, I/O and chipset RAM supplies in notebook computers.

The RT8208A/B achieves high efficiency at a reduced cost by eliminating the current sense resistor in traditional current mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs. The buck conversion allows this device to directly step down from high voltage batteries for the highest possible efficiency. Additional features include soft-start, under voltage protection, programmable over current protection and non-overlapping gate drive. The RT8208A/B is available in a WQFN-16L 3x3 package.

Pin Configurations

(TOP VIEW)



WQFN-16L 3x3

Features

- **Ultra-High Efficiency**
- **Resistor Programmable Output Voltage from 0.75V to 3.3V with Integrated Transition Support**
- **Quick Load Step Response within 100ns**
- **1% V_{FB} Accuracy over Line and Load**
- **4.5V to 26V Battery Input Range**
- **Resistor Programmable Frequency**
- **Integrated Bootstrap Switch**
- **Resistor Programmable Positive Current Limit by Low Side $R_{DS(ON)}$ Sense (Lossless Limit)**
- **Negative Current Limiter**
- **Voltage Transient Overshoot Eliminator***
- **Over Voltage Protection**
- **Under Voltage Protection**
- **4 Steps Current Limit During Soft-Start**
- **Power Good Indicator**
- **RoHS Compliant and Halogen Free**

* Paten Pending

Applications

- Notebook Computers
- System Power Supplies
- I/O Supplies
- Programmable-Output Power Supplies

Ordering Information

RT8208 □□□

- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)
- Turn-on D0/D1 MOSFET
  A : G0/G1 High
  B : G0/G1 Low

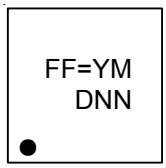
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

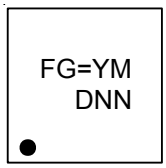
RT8208AGQW



FF= : Product Code

YMDNN : Date Code

RT8208BGQW



FG= : Product Code

YMDNN : Date Code

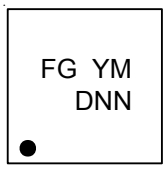
RT8208AZQW



FF : Product Code

YMDNN : Date Code

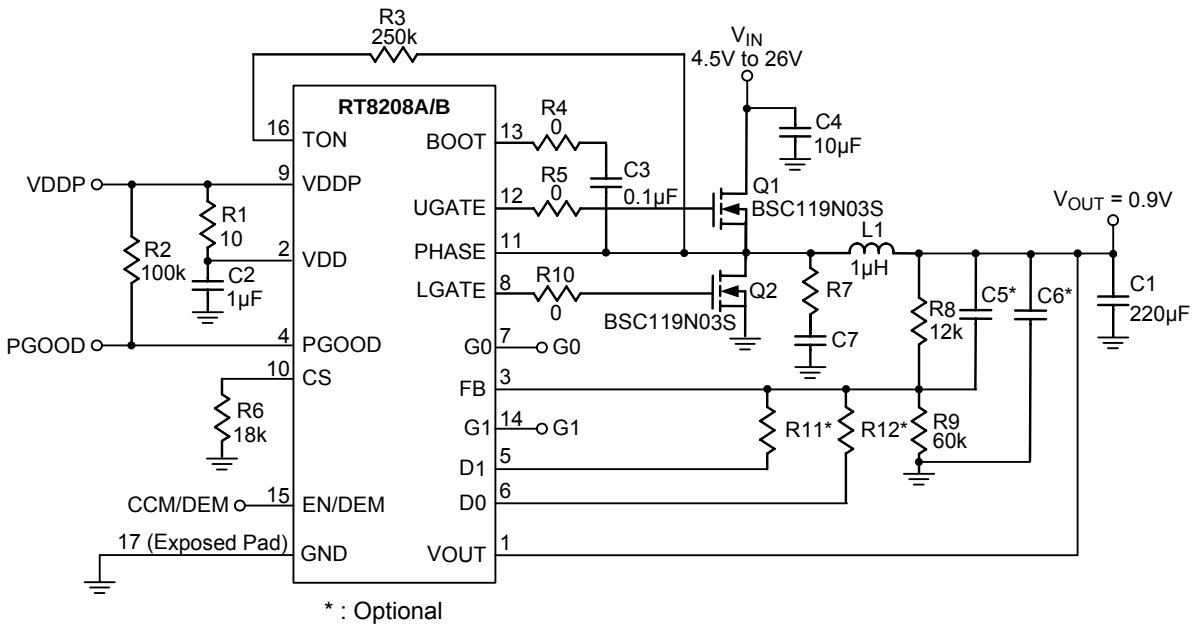
RT8208BZQW



FG : Product Code

YMDNN : Date Code

Typical Application Circuit



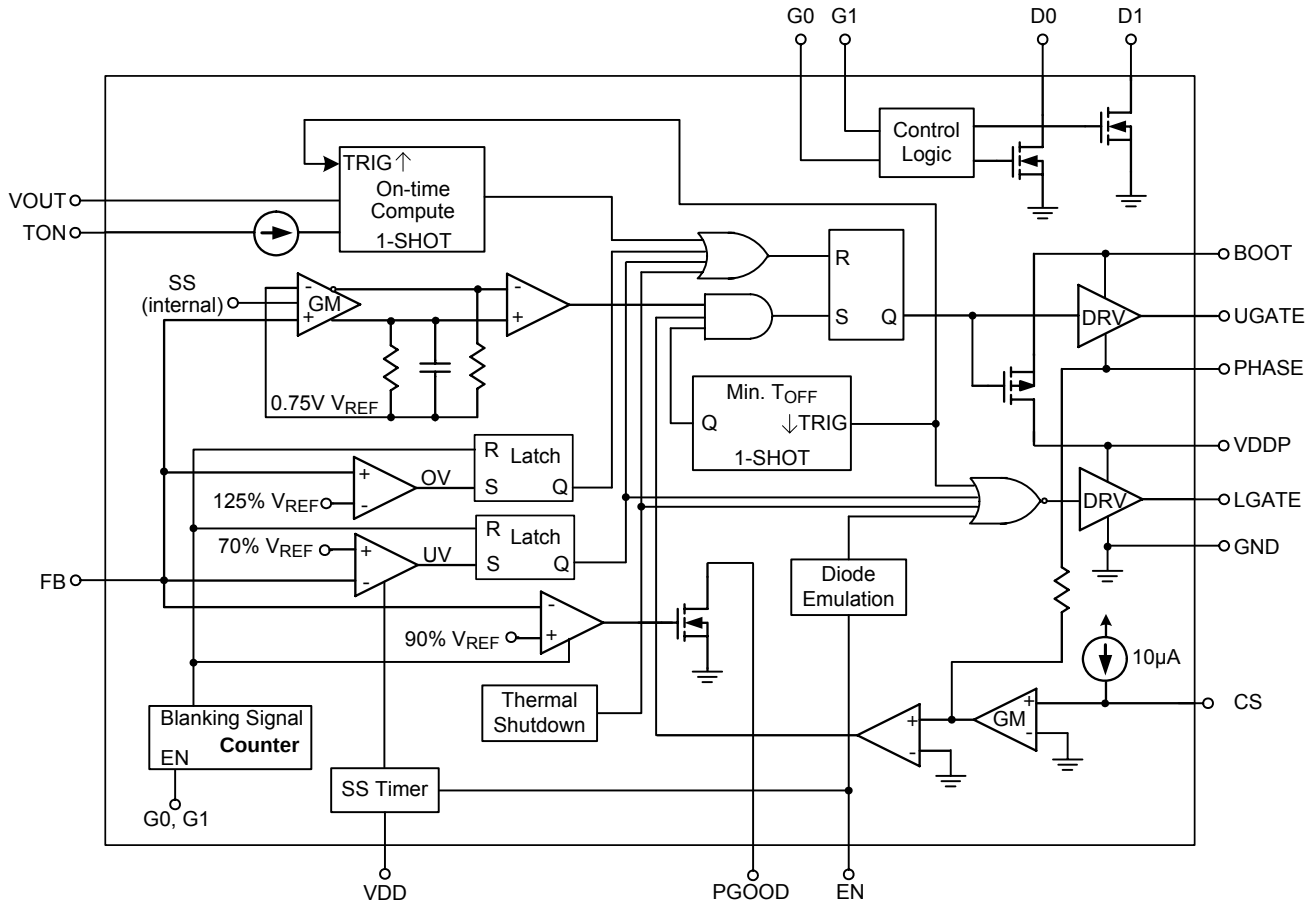
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VOUT	Output Voltage Pin. Connect to the output of PWM converter. VOUT is an input of the PWM controller.
2	VDD	Analog supply voltage input for the internal analog integrated circuit. Bypass to GND with a 1µF ceramic capacitor.
3	FB	Feedback Input Pin. Connect FB to a resistor voltage divider from VOUT to GND to adjust output voltage from 0.75V to 3.3V
4	PGOOD	Power good signal open-drain output of PWM converter. This pin will be pulled high when the output voltage is within the target range.
5	D1	Drain of the internal MOSFET which is controlled by G1.
6	D0	Drain of the internal MOSFET which is controlled by G0.

To be continued

Pin No.	Pin Name	Pin Function
7	G0	Control Input Pin for the D0 MOSFET. A logic high for RT8208A and low for RT8208B turn on the D0 MOSFET on, pulling D0 to the ground.
8	LGATE	Low side N-MOSFET gate driver output for PWM. This pin swings between GND and VDDP.
9	VDDP	VDDP is the gate driver supply for external MOSFETs. Bypass to GND with a 1μF ceramic capacitor.
10	CS	Over Current Trip Point Set Input. Connect a resistor from this pin to signal ground to set threshold for both over current and negative over current limit.
11	PHASE	The UGATE High Side Gate Driver Return. Also serves as anode of over current comparator.
12	UGATE	High side N-MOSFET floating gate driver output for the PWM converter. This pin swings between PHASE and BOOT.
13	BOOT	Boost Capacitor Connection for PWM Converter. Connect to an external ceramic capacitor to PHASE.
14	G1	Control Input Pin for the D1 MOSFET. A logic high for RT8208A and low for RT8208B turn on the D1 MOSFET on, pulling D1 to the ground.
15	EN/DEM	Enable/Diode Emulation Mode Control Input. Connect to VDD for diode–emulation mode, connect to GND for shutdown and floating the pin for CCM mode.
16	TON	On Time/Frequency Adjustment Pin. Connect to PHASE through a resistor. TON is an input for the PWM controller.
17 (Exposed pad)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- BOOT to GND ---------- –0.3V to 38V
- BOOT to PHASE ---------- –0.3V to 6V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - < 20ns ---------- –8V to 38V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - < 20ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to 6
  - < 20ns ---------- –2.5V to 7.5V
- VDD, VDDP, VOUT, EN/DEM, FB, PGOOD, TON to GND ---------- –0.3V to 6V
- CS to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–16L 3x3 ---------- 1.471W
- Package Thermal Resistance (Note 2)
  - WQFN–16L 3x3, θ_{JA} ---------- 68°C/W
  - WQFN–16L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 4.5V to 26V
- Supply Voltage, V_{DD}, V_{DDP} ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 15V, V_{DD} = V_{DDP} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
Quiescent Supply Current	I_Q	VDD + VDDP, V_{FB} = 0.8V	--	--	1250	μA
Shutdown Current	I_{SHDN}	V_{DD} + V_{DDP}	--	1	10	μA
		EN/DEM = GND	–10	–1	--	
FB Reference Voltage	V_{REF}	V_{DD} = 4.5V to 5.5V	0.742	0.750	0.758	V
FB Input Bias Current		V_{FB} = 0.75V	–1	0.1	1	μA
Output Voltage Range	V_{OUT}		0.75	--	3.3	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
D0 Pull-Down Resistance		D0 to GND, G0 = 5V	--	10	--	Ω
D1 Pull-Down Resistance		D1 to GND, G1 = 5V	--	10	--	Ω
On-Time		V_{PHASE} = 12V, V_{OUT} = 2.5V, R_{TON} = 250kΩ	336	420	504	ns
Minimum Off-Time			250	400	550	ns
VOUT Shutdown Discharge Resistance		EN/DEM = GND	--	20	--	Ω
Current Sensing						
Current Limiter Source Current		CS to GND	9	10	11	μA
Current Comparator Offset			−10	--	10	mV
Zero Crossing Threshold		PHASE to GND, EN/DEM = 5V	−10	--	5	mV
Fault Protection						
Current Limit (Threshold)		GND to PHASE, V_{CS} = 50mV	40	50	60	mV
		GND to PHASE, V_{CS} = 200mV	190	200	210	
Current Limit Setting Range		CS to GND	50	--	200	mV
Output UV Threshold		UVP Detection	60	70	80	%
OVP Threshold	V_{FB_OVP}	OVP Detection	120	125	130	%
OV Fault Delay		FB forced above OV threshold	--	20	--	μs
VDD Under Voltage Lockout Threshold		Rising edge, PWM disabled below this level	4.1	4.3	4.5	V
		Hysteresis	--	80	--	mV
Current Limit Step Duration at Soft-Start		Each step	--	128	--	clks
UVP Blanking Time		From EN signal going high	--	512	--	clks
Thermal Shutdown	T_{SHDN}		--	155	--	°C
Thermal Shutdown Hysteresis			--	10	--	°C
Driver On-Resistance						
UGATE Drive Source	$R_{UGATEsr}$	BOOT to PHASE = 5V	--	2	5	Ω
UGATE Drive Sink	$R_{UGATEsk}$	BOOT to PHASE = 5V	--	1	5	Ω
LGATE Drive Source	$R_{LGATEsr}$	LGATE, High State	--	1	5	Ω
LGATE Drive Sink	$R_{LGATEsk}$	LGATE, Low State	--	0.5	2.5	Ω
UGATE Gate Driver Source/Sink Current		UGATE to PHASE = 2.5V, BOOT to PHASE = 5V	--	1	--	A
LGATE Gate Driver Source Current		LGATE forced to 2.5V	--	1	--	A
LGATE Gate Driver Sink Current		LGATE forced to 2.5V	--	3	--	A
Dead Time		LGATE Rising (Phase = 1.5V)	--	30	--	ns
		UGATE Rising	--	30	--	
Internal Boost Charging Switch On-Resistance		VDDP to BOOT, 10mA	--	--	80	Ω

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic I/O						
EN/DEM Logic Input Voltage		EN/DEM Low	--	--	0.8	V
		EN/DEM High	2.9	--	--	
		EN/DEM Floating	--	2	--	
G0 Logic Input Voltage		G0 Low	--	--	0.8	V
		G0 High	2	--	--	
G1 Logic Input Voltage		G1 Low	--	--	0.8	V
		G1 High	2	--	--	
Logic Input Current		EN/DEM = VDD	--	1	5	μA
		EN/DEM = 0	–5	1	--	
		G0 = G1 = VDD or GND	–1	--	5	
PGOOD						
PGOOD Threshold		V_{FB} with respect to Reference, PGOOD from Low to High	87	90	93	%
		V_{FB} with respect to Reference, PGOOD from High to Low	--	125	--	
		Hysteresis	--	3	--	
Fault Propagation Delay		Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage		I_{SINK} = 1mA	--	--	0.4	V
Leakage Current		High state, forced to 5V	--	--	1	μA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

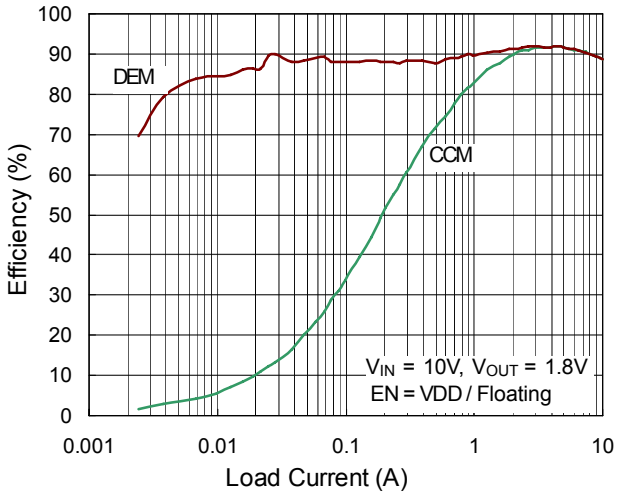
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a four layers high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

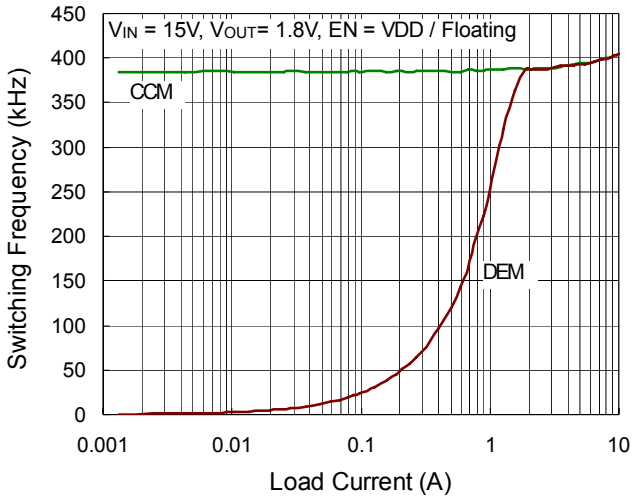
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

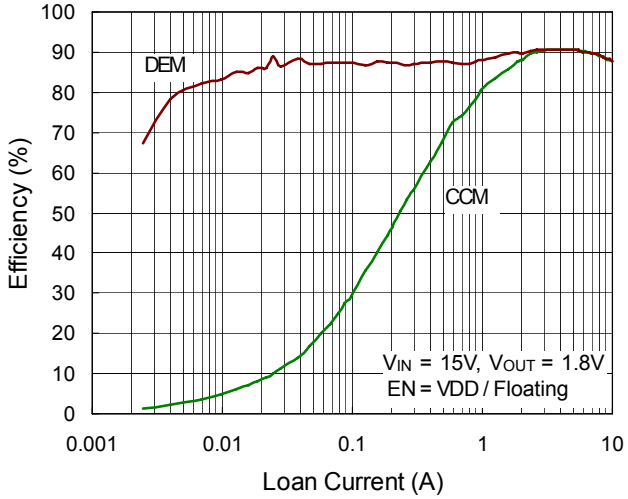
1.8V Efficiency vs. Load Current



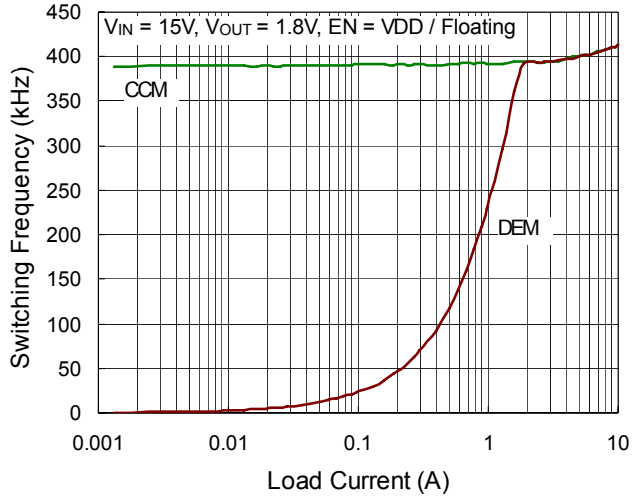
Switching Frequency vs. Output Current



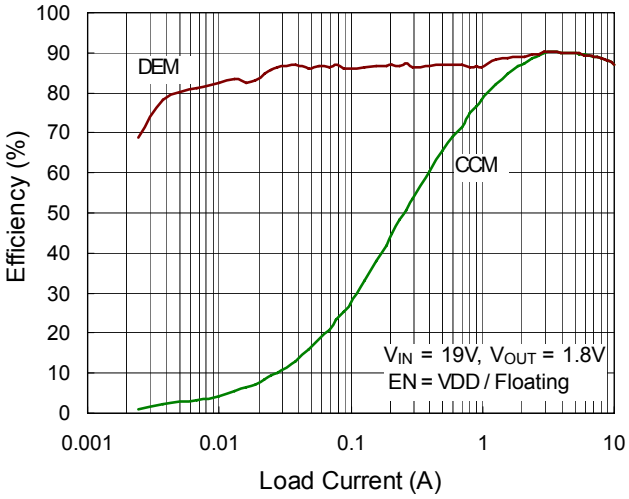
1.8V Efficiency vs. Load Current



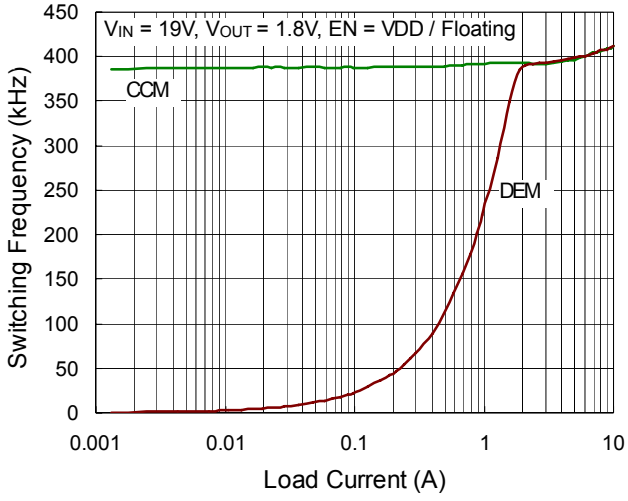
Switching Frequency vs. Output Current



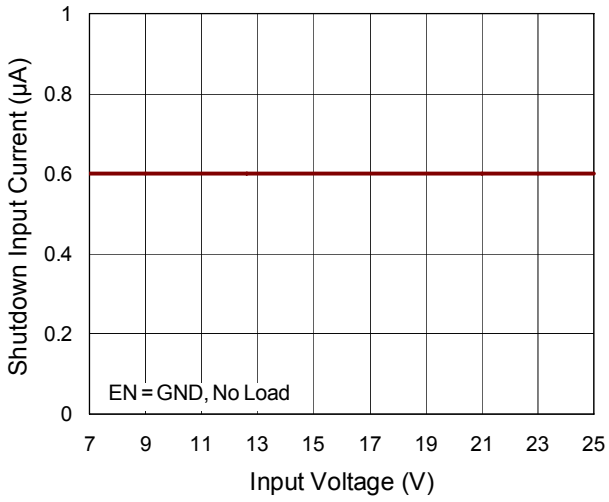
1.8V Efficiency vs. Load Current



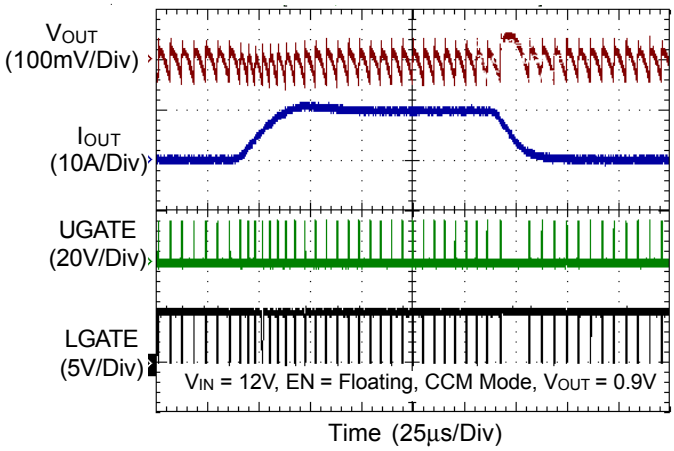
Switching Frequency vs. Output Current



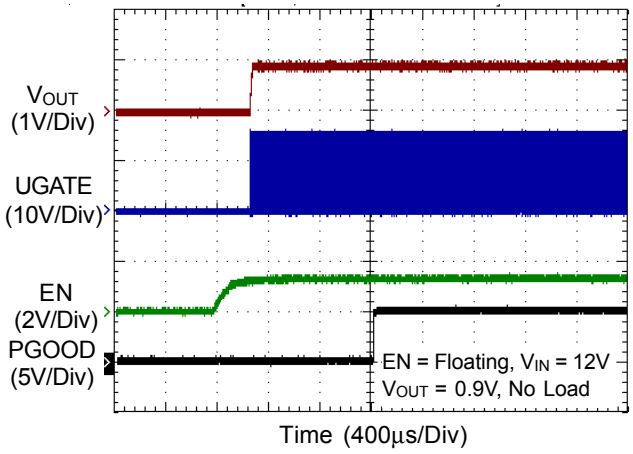
Shutdown Input Current vs. Input Voltage



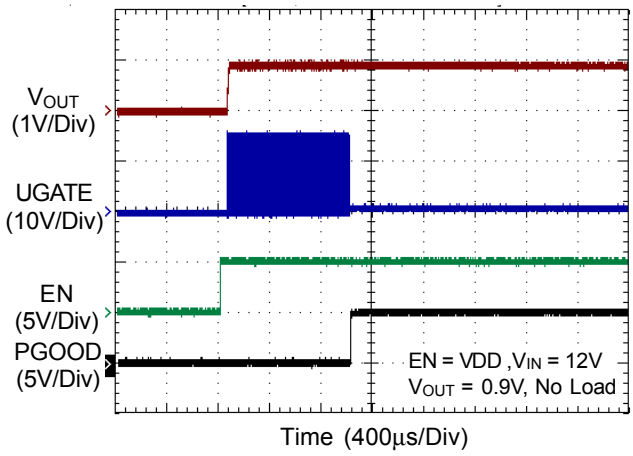
0.9V Load Transient Response



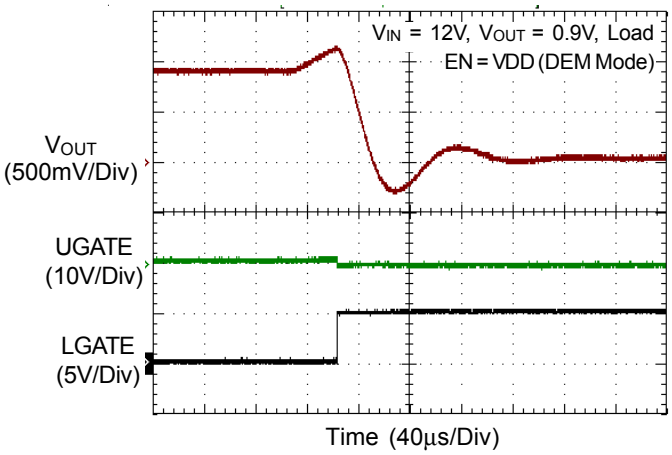
Power On From EN (CCM)



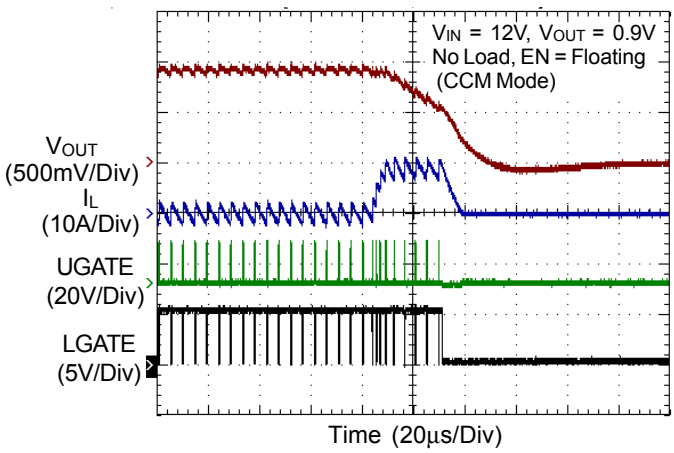
Power On From EN (DEM)



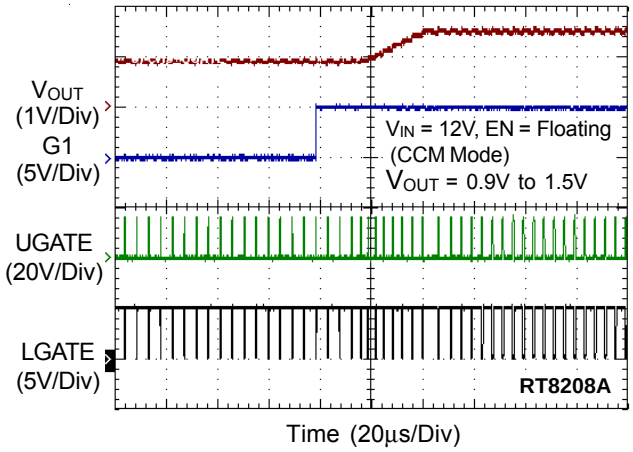
OVP Waveforms



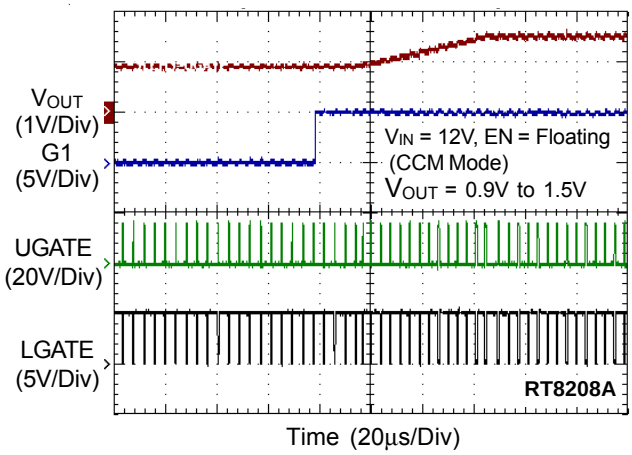
UVP Waveforms



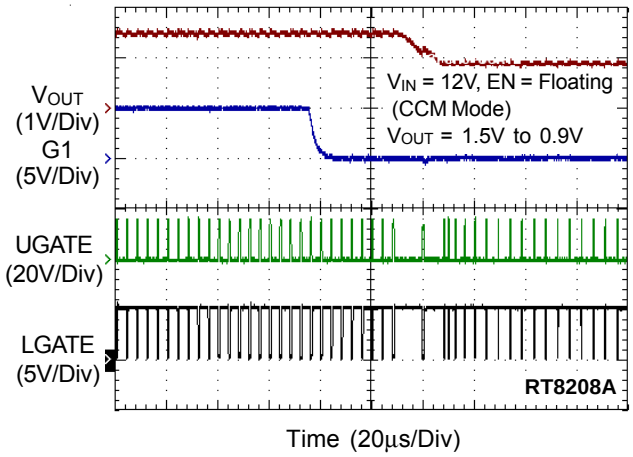
V_{OUT} Up Transient (No Load)



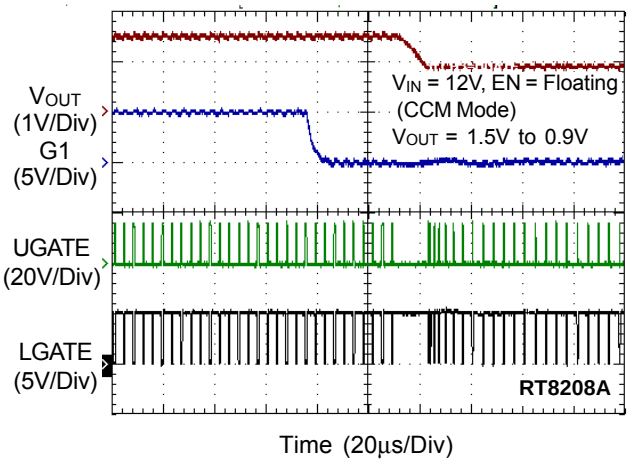
V_{OUT} Up Transient (Load=10A)



V_{OUT} Down Transient (No Load)



V_{OUT} Down Transient (Load=10A)



Application Information

The RT8208A/B is a constant-on-time PWM controller which provides four resistor-programmable DC output voltages by controlling the G0 and G1 digital input. The output voltage is programmable from 0.75V to 3.3V. The constant on-time PWM control scheme handles wide input/ output rations with ease and providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load transient timing problems of fixed-frequency current mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

PWM Operation

The Mach Response™, DRV™ mode controller relies on the output filter capacitor' s effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. Refer to the function diagrams of the RT8208A/B, the synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET is turned off. The pulse width of this one shot is determined by the converter' s input and output voltages to keep the frequency fairly constant over the input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

On-Time Control (t_{ON})

The on-time one-shot comparator has two inputs. One input monitors the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. The implementation results in a nearly constant switching frequency without the need of a clock generator.

t_{ON} = 9.6p x R_{TON} x (V_{OUT} + 0.1) / (V_{IN} – 0.3) + 50ns

Although this equation provides a good approximation to start with, the accuracy depends on each design and selection of the high side MOSFET.

And then the switching frequency (f) is:

$$f = \frac{V_{OUT}}{V_{IN} \times t_{ON}}$$

R_{TON} is a resistor connected from the PHASE to TON pin.

Mode Selection (EN) Operation

The EN pin enables the supply. When EN/DEM is tied to VDD, the controller is enabled and operates in diode-emulation mode. When the EN pin is floating, the RT8208A/B will operate in forced-CCM mode.

Diode-Emulation Mode (EN = High)

In diode-emulation mode, the RT8208A/B automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increasing VOUT ripple or load regulation. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial of negative current when the inductor freewheeling current reach negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level than requires the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light-load operation can be calculated as follows (Figure 1) :

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is On-time.

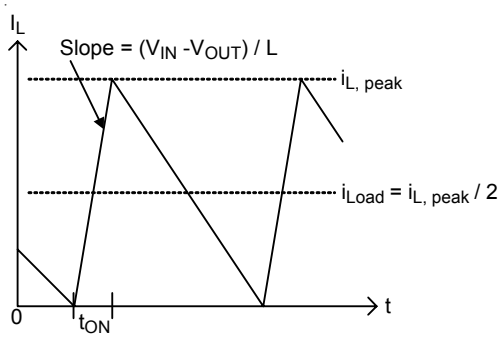


Figure 1. Boundary Condition of CCM/DEM

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

Forced-CCM Mode (EN = floating)

The low noise, forced-CCM mode (EN=floating) disables the zero-crossing comparator, which controls the low side switch on-time. This causes the low side gate drive waveform to become the complement of the high side gate-drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio VOUT/VIN. The benefit of forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost: The no-load battery current can be up to 10mA to 40mA, depending on the external MOSFETs.

Output Voltage Setting (FB)

The output voltage can be adjusted from 0.75V to 3.3V by setting the feedback resistor R1 and R2, see Figure 2. With G0 and G1 in low state, the output voltage is at the lowest value. Choose R2 to be approximately 20kΩ, and solve for R1 using the equation :

$$V_{OUT} = V_{REF} \times \left(1+\frac{R1}{R2}\right)$$

where V_{REF} is 0.75V in typical.

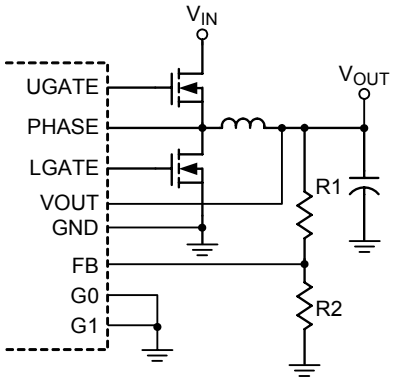


Figure 2. Setting V_{OUT} with a Resistor Divider

Output Voltage Transition Control

The RT8208A/B provides two digital control input G0 and G1 to allow selection among four output voltages. The output voltage is regulated by comparing the FB pin (connected to VOUT via an external resistor divider) to the internal 0.75V reference. The G0 and G1 digital input control the gate of internal respective MOSFET whose drain is connected to D0 and D1 respectively. Using Gx, the user controls whether Dx is grounded or open, which then controls the resistor divider ratio for V_{OUT}. A logic high signal on Gx will connect Dx to ground.

When the Gx input changes state, this change quickly causes three actions:

1. D0 changes state.
2. The power good PGOOD output is temporarily latched into its present state. This prevents chattering or false tripping while V_{OUT} moves to the new level.
3. When the Gx changes state whether DEM is set or not, then enter the PWM mode and counts 32 clock cycles. For the duration of 32 clock cycles, the OVP and UVP function is masked. This behavior allows the output to slew down to the new level without tripping the OVP or UVP function when the Gx change causes rapid change of Dx, which in turns cause a rapid change at FB.

Output voltage is regulated through the FB pin via resistors R1 through R4 as shown in Figure 3.

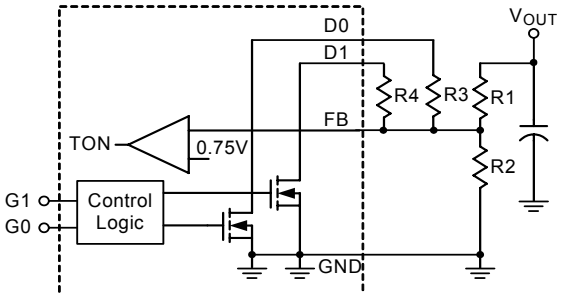
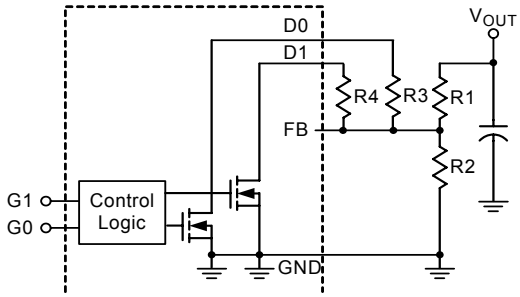


Figure 3. Output Voltage Selection By G0 and G1 Input



The following table shows the equations for VOUT as a function of digital control input G0 and G1.

RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

Note that the $R_{DS(ON)}$ of the internal MOSFET is in series with external resistor, which adds typically 10Ω in series.

Output Voltage Transition Operation

The digital input control pin Gx allows VOUT to transition to both higher and lower values. For a down transition, the rapid change Gx from high to low as sudden release either of external resistors (R3 or R4) will cause FB to go above the 0.75V threshold. At this time, the LGATE will drive high to turn on the low side MOSFET and draw current from the output capacitor via the inductor. LGATE will remain on until FB falls to 0.75V, at which point a normal UGATE switching cycle begins, see Figure4. For a down transition, the low side MOSFET stays on before FB reaches to 0.75V, thus the negative inductor current will be increased. If the negative current is too large to trigger NOCP, the low side MOSFET is turned off which can avoid too much negative current to damage component. Refer to the Negative Over Current Limit section for a full description.

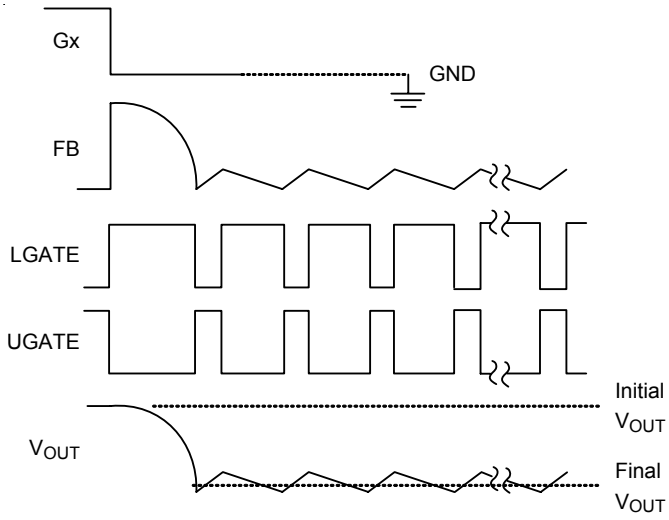


Figure 4. Output Voltage Down Transition

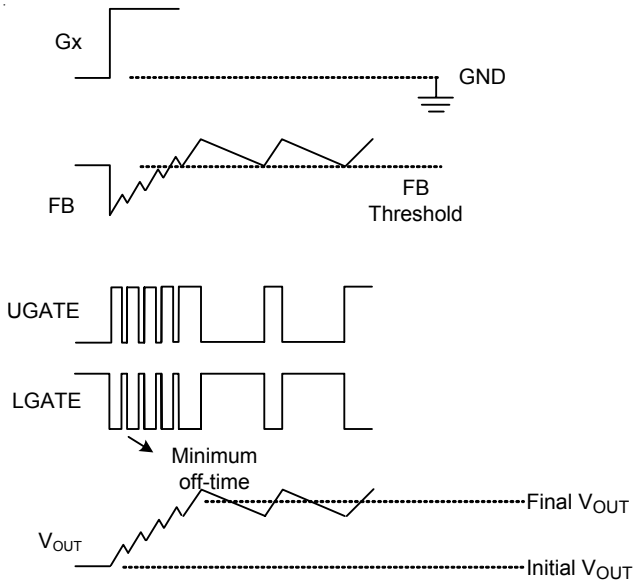


Figure 5. Output Voltage Up Transition

For an up transition (from lower to higher VOUT) as shown in Figure5, the Gx change affects Dx and causes FB to drop below the 0.75V trip point. This quickly trips the FB comparator regardless of whether DEM is active or not, generating an UGATE on-time and a subsequent LGATE will be turned on. At the end of the minimum off-time (400ns), if FB is still below 0.75V then another UGATE on-time is started. This sequence continues until the FB pin exceeds 0.75V.

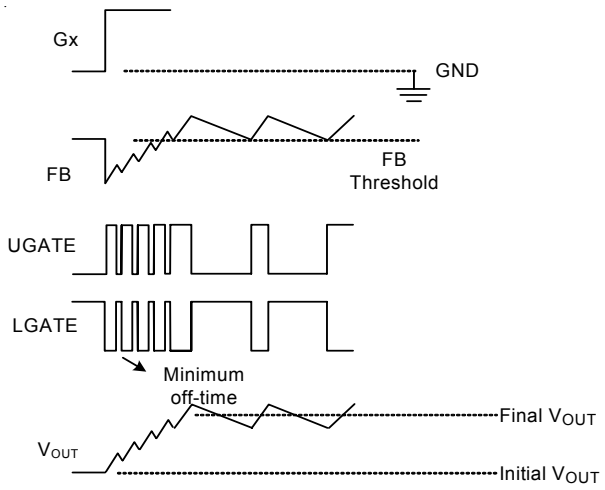


Figure 6. Output Voltage Up Transition with Overshooting

If the VOUT change is significant, there can be several consecutive cycle of UGATE on-time followed by minimum LGATE time. This can cause a rapid increase in inductor current: typically it takes only a few switching cycles for inductor current to rise up to the current limit. At some point the FB voltage will rise up to the 0.75V reference and the UGATE pulses will cease, but the inductor' s LI^2 energy must then flow into the output capacitor. This can create a significant overshoot as shown in Figure6.

The overshooting can be approximated by the following equation, where I_{CL} is the current limit, V_{FINAL} is the desired set point for the final voltage, L is in μH and C_{OUT} is in μF.

$$V_{MAX} = \sqrt{\left(\left(\frac{I_{CL}^2 \times L}{C_{OUT}}\right) + V_{FIANL}^2\right)}$$

The Overshoot eliminator (Patent Pending) prevents output voltage overshooting after rapid changes of Gx. This results in a gradual change from $V_{OUT(INITIAL)}$ to $V_{OUT(FINAL)}$ and prevents the buildup of high inductor current and reducing overshoot.

Current Limit Setting (OCP)

RT8208A/B has cycle-by-cycle current limiting control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at CS is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 7).in order to provide both good accuracy and a cost effective solution, the RT8208A/B supports temperature compensated MOSFET $R_{DS(ON)}$ sensing. The CS pin should be connected to GND through the trip voltage setting resistor, R_{CS}. The CS terminal source 10μA I_{CS} current, and the trip level is set to the CS trip voltage, V_{CS} as in the following equation.

$$V_{CS}(mV) = R_{CS}(k\Omega) \times 10(\mu A)$$

Inductor current is monitored by the voltage between the PGND pin and the PHASE pin. So the PHASE pin should be connected to the drain terminal of the low-side MOSFET. I_{CS} has temperature coefficient to compensate the temperature dependency of the $R_{DS(ON)}$. PGND is used as the positive current sensing node. So PGND should be connected to the source terminal of the bottom MOSFET.

As the comparison is done during the OFF state, V_{CS} sets the valley level of the inductor current. Thus, the load current at over current threshold, I_{LOAD_OC}, can be calculated as follows ;

$$I_{LOAD_OC} = \frac{V_{CS}}{R_{DS(ON)}} + \frac{I_{Ripple}}{2}$$

$$= \frac{V_{CS}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

In an over current condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall. Eventually, it crosses the under-voltage protection threshold and shutdown.

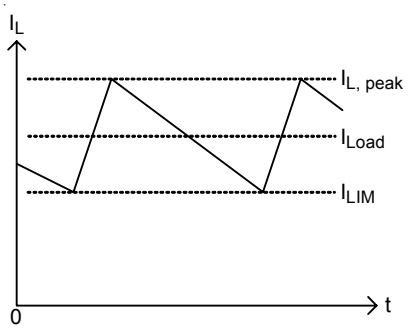


Figure 7. "Valley" Current Limit

Negative Over Current Limit (CCM Mode Only)

The RT8208A/B also supports cycle-by-cycle negative over current limiting in CCM Mode only. The over-current limit is set to be negative but is the same absolute value as the positive over current limit. If output voltage continues to rising, the low side MOSEFT stays on, thus inductor current is reduced and reverses direction after it reaches zero. When there is too much negative current in the inductor, the low side MOSFET is turned off and the current flows to VIN through the body diode of the high side MOSFET. Because this protection limits current to discharge the output capacitor, output voltage tends to rise, eventually hitting the over-voltage protection threshold and shutdown. In order to prevent false OVP from triggering, the low side MOSFET is turned on again 400ns after it is turned off. If the device hits the negative over-current threshold again before output voltage is discharged to the target level, the low side MOSFET is turned off and process repeats. It ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output is discharged to the target level before negative current threshold is reached, the low side MOSFET is turned off, the high side MOSFET is then turn on, and the device resumes normal operation.

MOSFET Gate Driver (UGATE, LGATE)

The high-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from VDDP supply. The average drive current is proportional to the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOT and PHASE pins. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low side MOSFET on, and low-side MOSFET off to high side MOSFET on. The low-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFETs. The internal pull-down transistor that drives LGATE low is robust, with a 0.6Ω typical on resistance. A 5V bias voltage is delivered from VDDP supply. The instantaneous drive current is supplied by the flying capacitor between VDDP and PGND.

For high current applications, some combinations of high and low side MOSFETs might be encountered that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time (Figure 8).

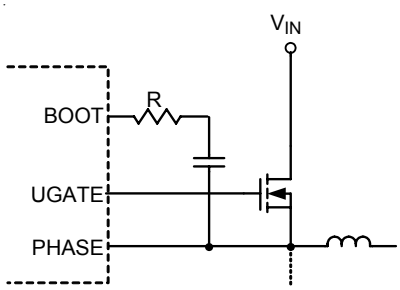


Figure 8. Reducing the UGATE Rise Time

Power Good Output (PGOOD)

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 25% above or 10% below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to within these tolerances once more. In soft-start, PGOOD is actively held low and is allowed to transition high until soft-start is over and the output reaches 93% of its set voltage. There is a 2.5μs delay built into PGOOD circuitry to prevent false transition.

When Gx changes state, PGOOD is immediately latched into its present state for 32 clock cycle while VOUT and FB are changed to the new level. After that the latch will be disabled.

POR, UVLO and Soft-Start

Power On Reset (POR) occurs when VDD rises above to approximately 4.3V. after POR is triggered. And then, the RT8208A/B will reset the fault latch and prepare the PWM for operation. Below 4.1V (MIN), the VDD under voltage lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low. A built-in soft-start is used to prevent surge current from power supply input after EN is enabled. The maximum allowed current limit is segmented in 4 steps: 25%, 50%, 75% and 100% during this period, each step is 128 UGATE clks. The current limit steps can eliminate the V_{OUT} folded-back in the soft-start duration.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage protection. When the output voltage exceeds 25% of the its set voltage threshold, over voltage protection is triggered and the low side MOSFET is latched on. This activates the low side MOSFET to discharge the output capacitor. The RT8208A/B is latched once OVP is triggered and can only be released by VDD or EN power on reset. There is 20μs delay built into the over voltage protection circuit to prevent false transitions.

When Gx changes state, the OVP function is masked for 32 clock cycle while VOUT and FB are changed to the new level. After that the mask will be disabled.

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When the output voltage is less than 70% of its set voltage threshold, under voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. In order to remove the residual charge on the output capacitor during the under voltage period, if PHASE is greater than 1V, the LGATE is forced high until PHASE is lower than 1V. There is 2.5μs delay built into the under voltage protection circuit to prevent false transitions. During soft-start, the UVP blanking time is 512 UGATE clks.

When Gx changes state, the UVP function is masked for 32 clock cycle while VOUT and FB change to the new level, after which the mask is disable.

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows :

$$L = \frac{T_{ON} \times (V_{IN} - V_{OUT})}{L_{IR} \times I_{LOAD(MAX)}}$$

Where L_{IR} is the ratio of peak-to-peak ripple current to the maximum average inductor current. Find a low-pass inductor having the lowest possible DC resistance that fits in the allowed dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough and not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left[\left(\frac{L_{IR}}{2}\right) \times I_{LOAD(MAX)}\right]$$

Output Capacitor Selection

The output filter capacitor must have low enough Equivalent Series Resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must also be high enough to absorb the inductor energy while transiting from full-load to no-load conditions without tripping the overvoltage fault latch.

Although Mach Response™ DRV™ dual ramp valley mode provides many advantages such as ease-of-use, minimum external component configuration, and extremely short response time, due to not employing an error amplifier in the loop, a sufficient feedback signal needs to be provided by an external circuit to reduce the jitter level. The required signal level is approximately 15mV at the comparing point. This generates V_{Ripple} = (V_{OUT} / 0.75) x 15mV at the output node. The output capacitor ESR should meet this requirement.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high value ceramic capacitors directly across the outputs without taking precautions to ensure stability.

Large ceramic capacitors can have a high-ESR zero frequency and cause erratic and unstable operation. However, it is easy to add sufficient series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting VOUT or FB divider close to the inductor. There are two related but distinct ways including double-pulsing and feedback loop instability to identify the unstable operation. Double-pulsing occurs due to noise on the output or because the ESR is too low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillation at the output after line or load perturbations that can trip the over voltage protection latch or cause the output voltage to fall below the tolerance limit. The easiest method for stability checking is to apply a very zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with AC probe. Do not allow more than one ringing cycle after the initial step-response under- or over-shoot.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of the RT8208A/B, the maximum junction temperature of the die is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-16L 3x3 packages, the thermal resistance θ_{JA} is 68°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)} = (125°C - 25°C)/(68°C/W) = 1.471W$ for

WQFN-16L 3x3 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8208A/B package, the Figure 9 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

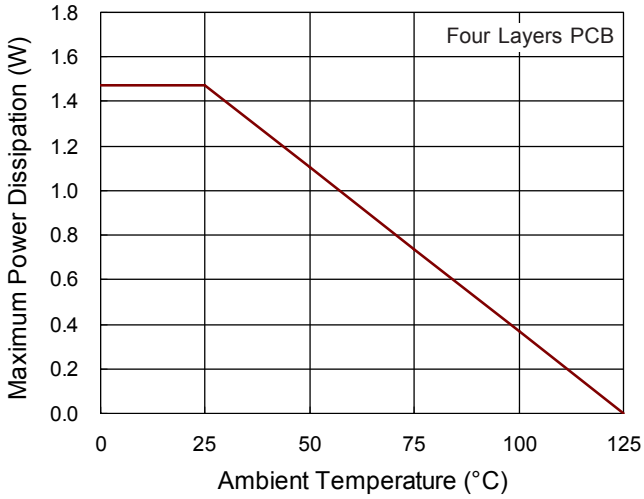


Figure 9. Derating Curve for RT8208A/B Package

Layout Considerations

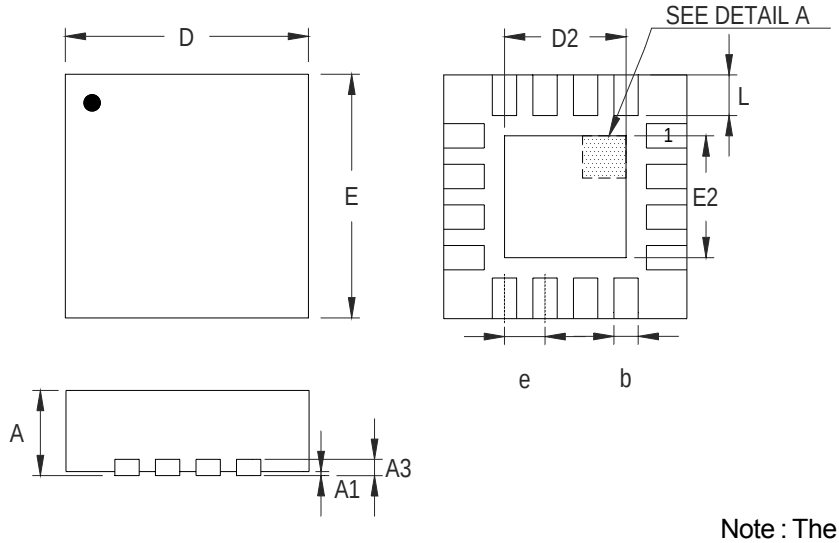
Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability.

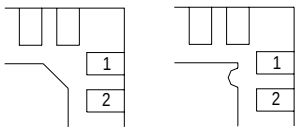
For best performance of the RT8208A/B, the following guidelines should be strictly followed.

- Connect an RC low pass filter from VDDP to VDD, 1μF and 10Ω are recommended. Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should be kept away from to high voltage switching nodes to prevent it from coupling.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.

- All sensitive analog traces and components such as VOUT, FB, GND, EN/DEM, PGOOD, OC, VDD, and TON should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to prevent it from coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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