5A, 24V, 570kHz Step-Down Converter

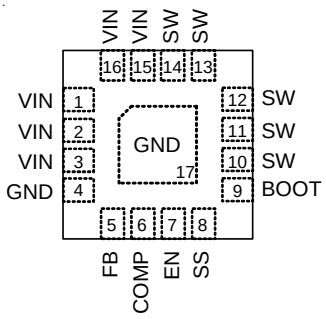
General Description

The RT8251 is a monolithic step-down switch mode converter with a built-in internal power MOSFET. It achieves 5A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization.

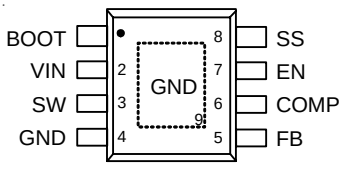
The RT8251 provides protection functions such as cycle-by-cycle current limiting and thermal shutdown. In shutdown mode, the regulator draws 25μA of supply current. Programmable soft-start minimizes the inrush supply current and the output overshoot at initial startup. The RT8251 requires a minimum number of external components. The RT8251 is available in WQFN-16L 3x3 and SOP-8 (Exposed Pad) packages.

Pin Configurations

(TOP VIEW)



WQFN-16L 3x3



SOP-8 (Exposed Pad)

Features

- **Wide Operating Input Voltage Range : 4.75V to 24V**
- **Adjustable Output Voltage Range : 0.8V to 15V**
- **Output Current up to 5A**
- **25μA Low Shutdown Current**
- **Internal Power MOSFET : 70mΩ**
- **High Efficiency up to 95%**
- **570kHz Fixed Switching Frequency**
- **Stable with Low ESR Output Ceramic Capacitors**
- **Thermal Shutdown Protection**
- **Cycle-By-Cycle Over Current Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Distributed Power Systems
- Battery Charger
- DSL Modems
- Pre-regulator for Linear Regulators

Ordering Information

RT8251 □□

Package Type
QW : WQFN-16L 3x3 (W-Type)
SP : SOP-8 (Exposed Pad-Option 1)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

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Marking Information

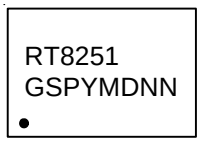
RT8251GQW



GE= : Product Code

YMDNN : Date Code

RT8251GSP



RT8251GSP : Product Number

YMDNN : Date Code

Typical Application Circuit

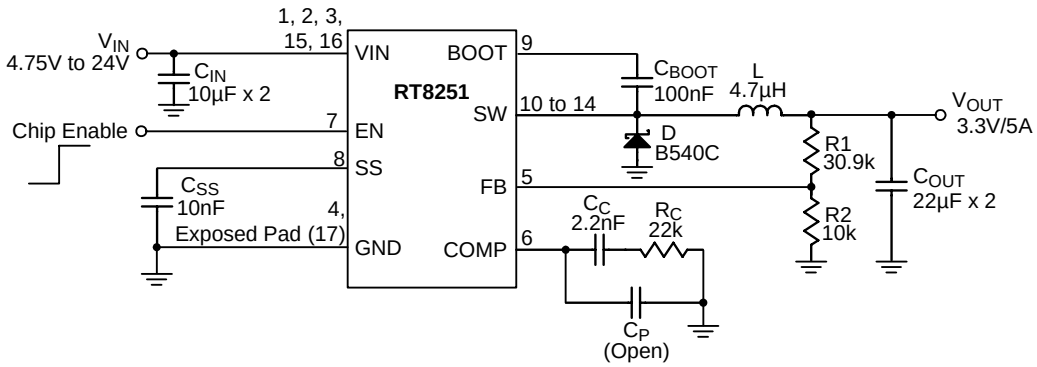


Figure 1. Typical Application Circuit for WQFN-16L 3x3

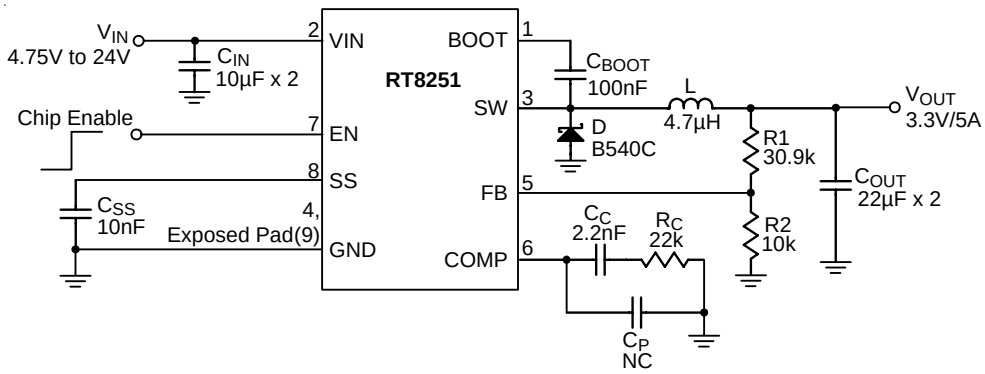


Figure 2. Typical Application Circuit for SOP-8 (Exposed Pad)

Table 1. Recommended Component Selection

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_C (kΩ)	C_C (nF)	L1 (µH)	C_{OUT} (µF)
15	182	10	51	1	22	44
10	115	10	43	1.2	10	44
8	91	10	39	1.5	10	44
5	52.3	10	30	1.5	6.8	44
3.3	30.9	10	22	2.2	4.7	44
2.5	21.5	10	16	2.2	4.7	44
1.8	12.4	10	13	2.2	2.2	44
1.2	4.99	10	13	2.2	2.2	44

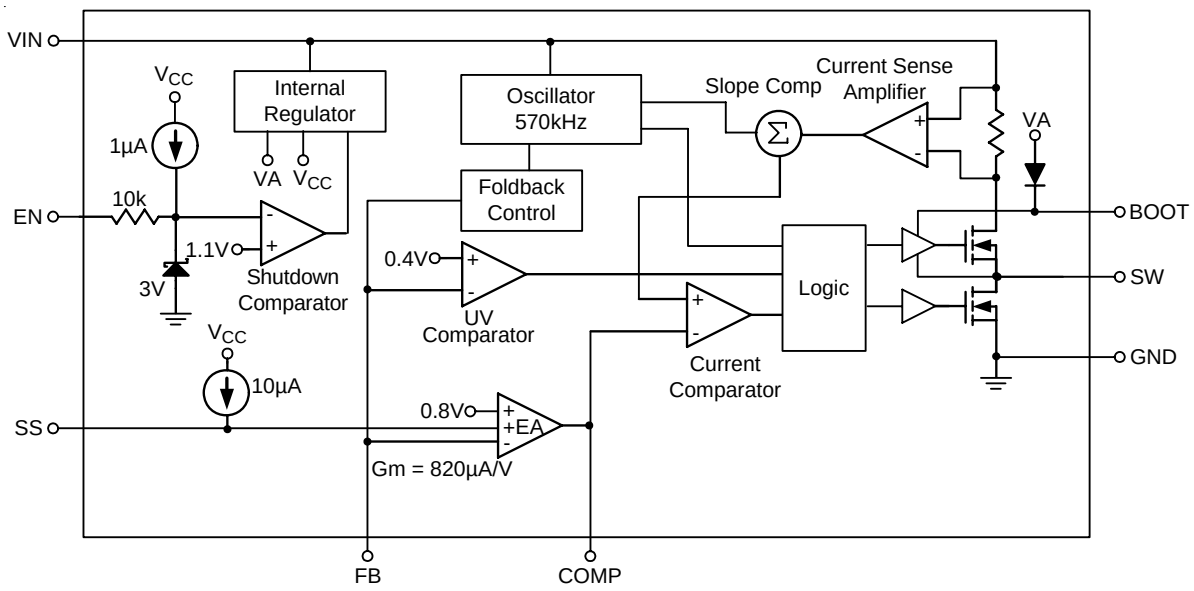
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Functional Pin Description

Pin No.		Pin Name	Pin Function
WQFN-16L 3x3	SOP-8 (Exposed Pad)		
1, 2, 3, 15, 16	2	VIN	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Connect VIN with a 4.75V to 24V power source. Connect VIN to GND with a capacitor that the capacitance is large enough to eliminate noise on the input to the IC.
4, 17 (Exposed Pad)	4, 9 (Exposed Pad)	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason, care must be taken in its layout. This node should be placed outside of the D1 to C_{IN} ground path to prevent switching current spikes from inducing voltage noise into the part. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	5	FB	Feedback Input. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
6	6	COMP	Compensation Node. This node is the output of the transconductance error amplifier and the input to the current comparator. Frequency compensation is done at this node by connecting a series R-C to ground.
7	7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN higher than 1.4V to turn on the regulator, lower than 0.4V to turn it off. For automatic startup, leave EN unconnected.
8	8	SS	Soft-Start Control Input. SS controls the soft start period. Connect a capacitor ($\geqq$10nF) from SS to GND to set the soft-start period. A 10nF capacitor sets the Soft-Start period to 1ms.
9	1	BOOT	Bootstrap. This capacitor C_{BOOT} is needed to drive the power switch's gate above the supply voltage. It is connected between the SW and BS pins to form a floating supply across the power switch driver. The voltage across C_{BOOT} is about 5V and is supplied by the internal +5V supply when the SW pin voltage is low.
10, 11, 12, 13, 14	3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BOOT to power the high-side switch.

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Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{IN} ---------- –0.3V to 26V
- Switching Voltage, V_{SW} ---------- –0.3V to (V_{IN} + 0.3V)
- BOOT Voltage, V_{BOOT} ---------- (V_{SW} – 0.3V) to (V_{SW} + 6V)
- All Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-16L 3x3 ---------- 1.471W
  - SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 2)
  - WQFN-16L 3x3, θ_{JA} ---------- 68°C/W
  - WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
  - SOP-8 (Exposed pad), θ_{JA} ---------- 75°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ---------- 4.75V to 24V
- Enable Voltage, V_{EN} ---------- 0V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

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Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Reference Voltage		V_{FB}	4.75V ≦ V_{IN} ≦ 24V	0.784	0.8	0.816	V
High-Side Switch-On Resistance		$R_{DS(ON)1}$		--	70	--	mΩ
Low-Side Switch-On Resistance		$R_{DS(ON)2}$		--	15	--	Ω
High-Side Switch Leakage			V_{EN} = 0V, V_{SW} = 0V	--	--	10	μA
Current Limit		I_{LIM}	Duty = 85%; $V_{BOOT-SW}$ = 4.8V	--	6.8	--	A
Current Sense Transconductance		G_{CS}	Output Current to V_{COMP}	--	4.6	--	A/V
Error Amplifier Tansconductance		gm	ΔI_C = ±10μA	--	920	--	μA/V
Oscillator Frequency		f_{SW}		420	570	720	kHz
Short Circuit Oscillation Frequency			V_{FB} = 0V	--	185	--	kHz
Maximum Duty Cycle		D_{MAX}	V_{FB} = 0.7V	--	85	--	%
Minimum On-Time		t_{ON}		--	100	--	ns
UVLO Threshold Rising				--	4.1	--	V
UVLO Threshold Hysteresis				--	200	--	mV
EN Input Voltage	Logic Low	V_{IL}		--	--	0.4	V
	Logic High	V_{IH}		1.4	--	5.5	
Enable Pull Up Current			V_{EN} = 0V	--	1	--	μA
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	25	--	μA
Quiescent Current		I_Q	V_{EN} = 2V, V_{FB} = 1V	--	0.8	1	mA
Soft-Start Current		I_{SS}	V_{SS} = 0V	--	10	--	μA
Soft-Start Period			C_{SS} = 10nF	--	1	--	ms
Thermal Shutdown		T_{SD}		--	150	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

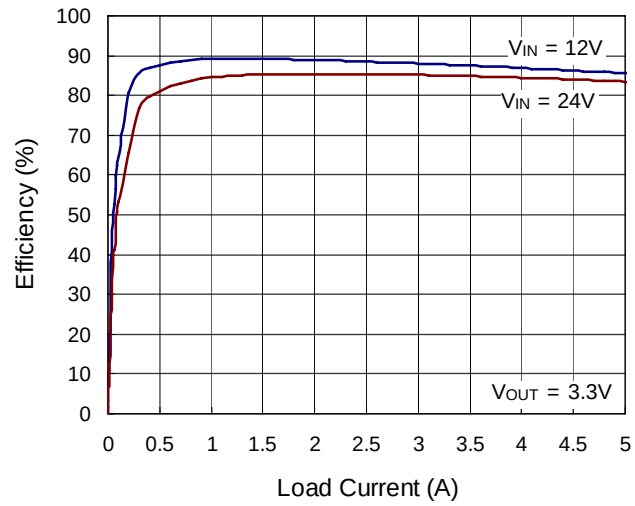
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

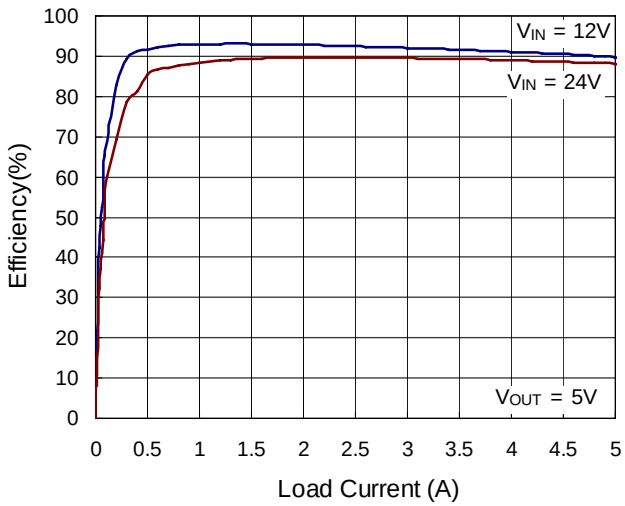
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Typical Operating Characteristics

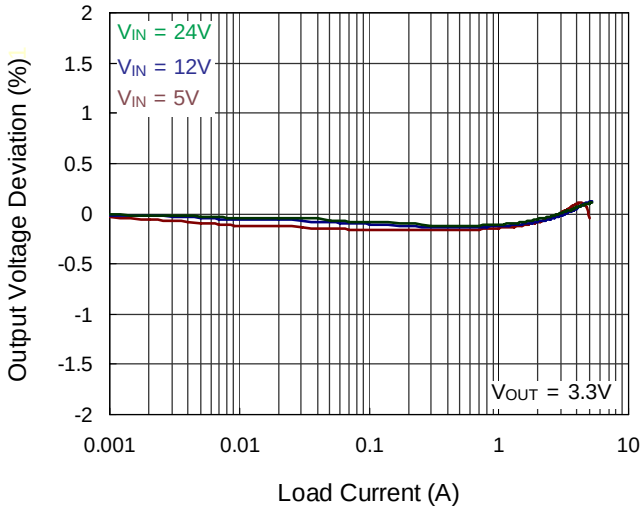
Efficiency vs. Load Current



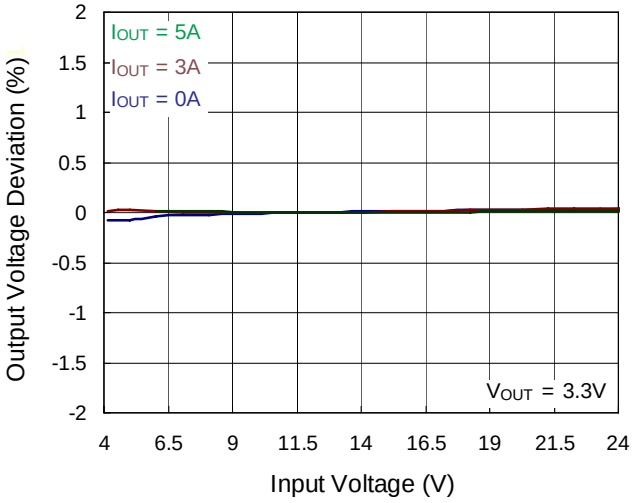
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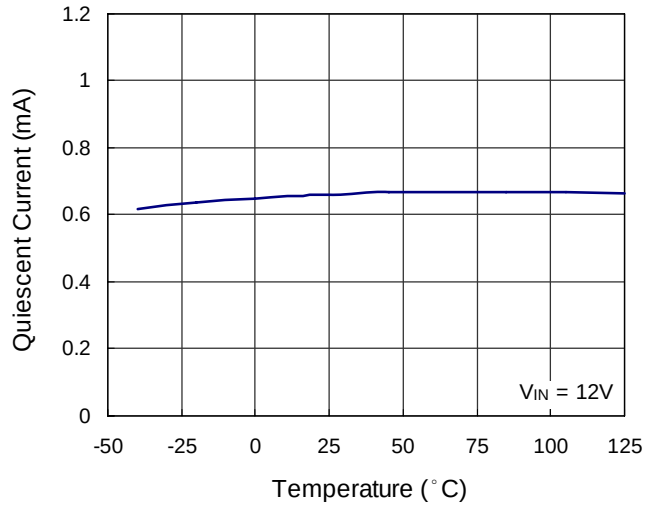
Output Voltag Deviation vs. Load Current



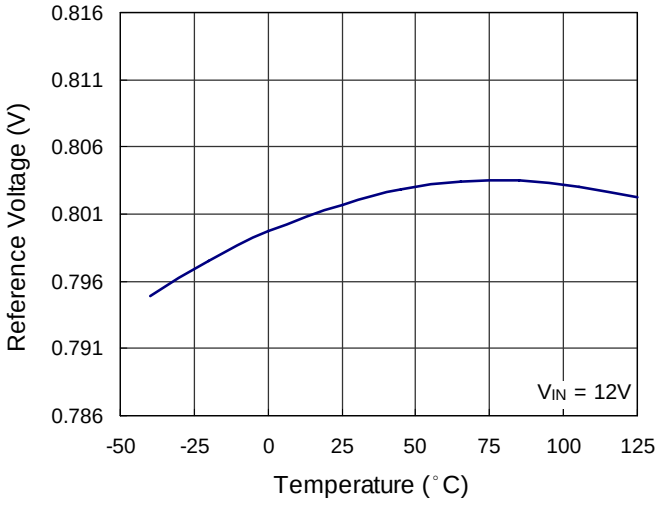
Output Voltage Deviation vs. Input Voltage



Quiescent Current vs. Temperature

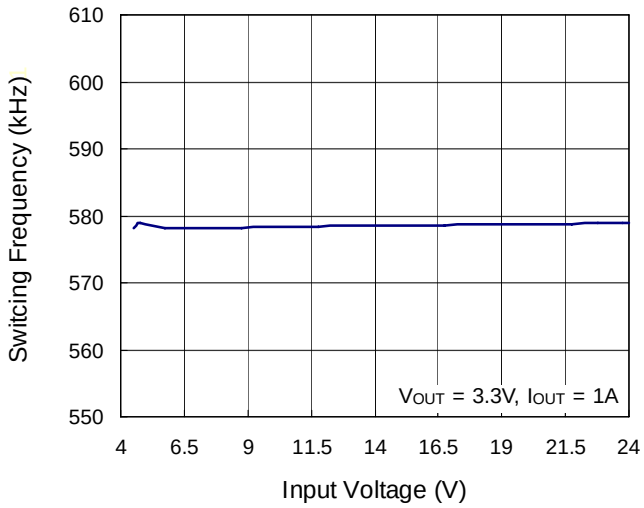


Reference Voltage vs. Temperature

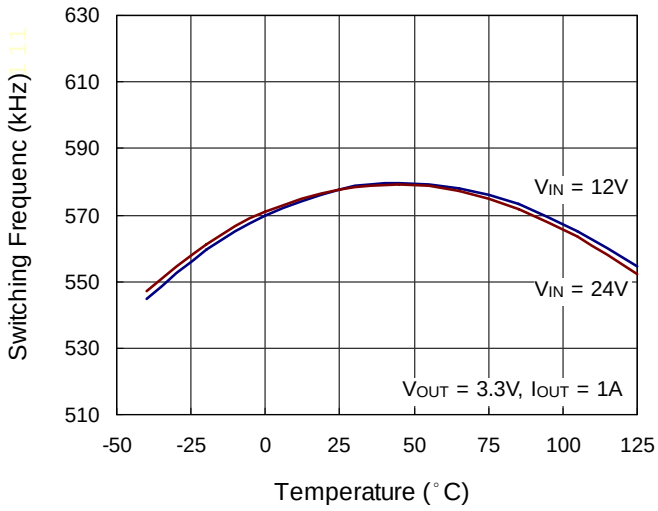


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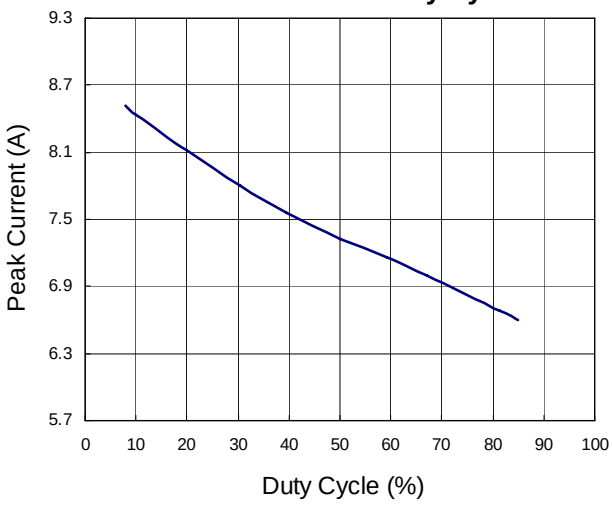
Switching Frequency vs. Input Voltage



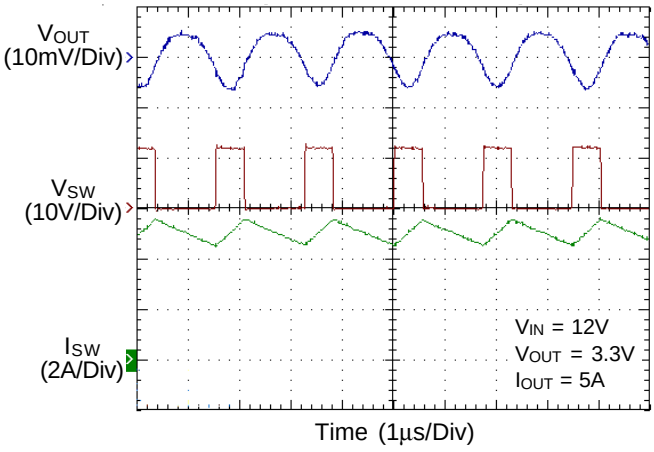
Switching Frequency vs. Temperature



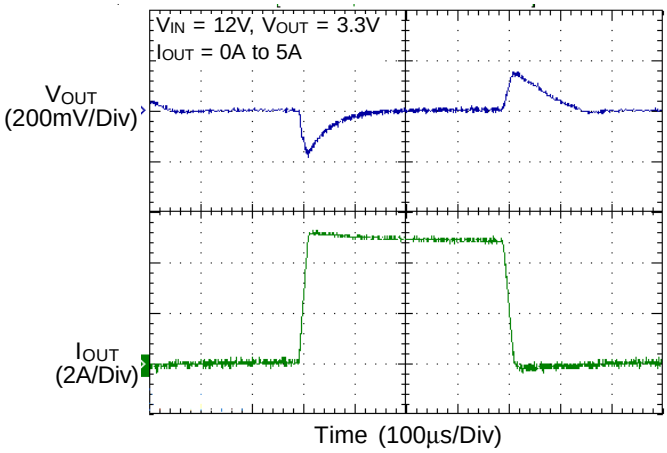
Current Limit vs. Duty Cycle



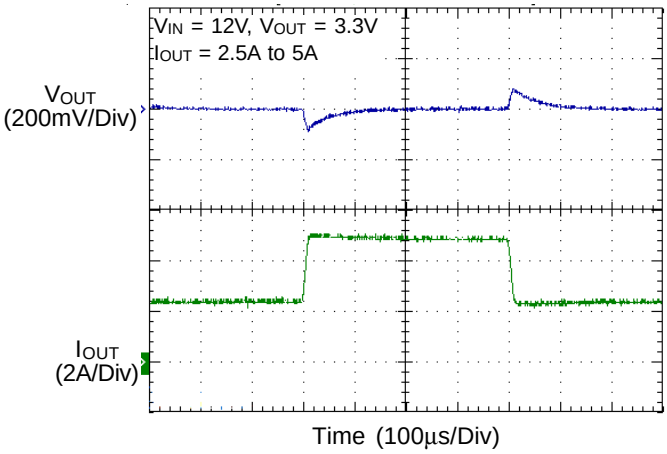
Output Ripple



Load Transient Response

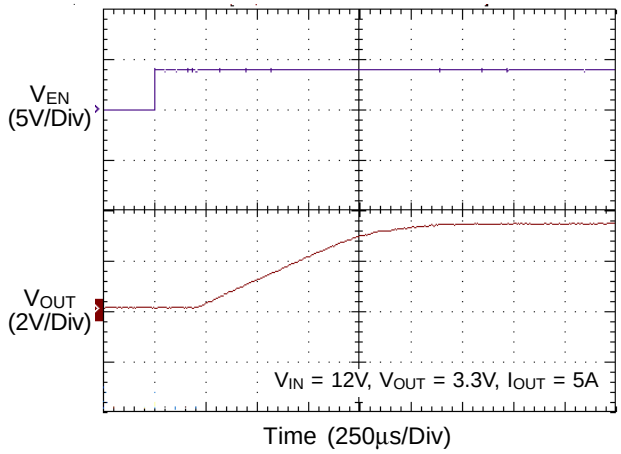


Load Transient Response

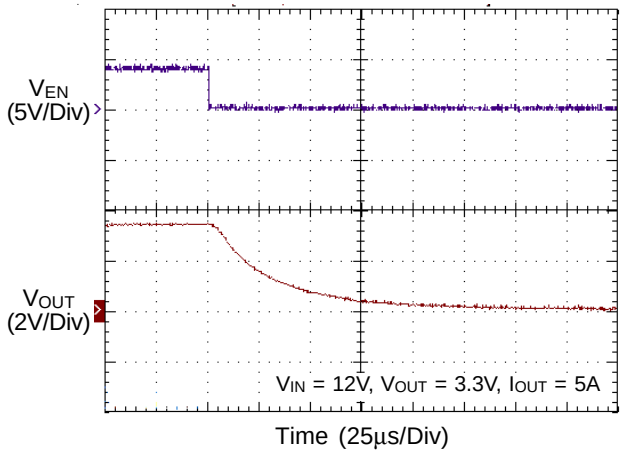


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Power On from EN



Power Off from EN



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Application Information

The RT8251 is an asynchronous high voltage buck converter that can support the input voltage range from 4.75V to 24V and the output current can be up to 5A.

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 3.

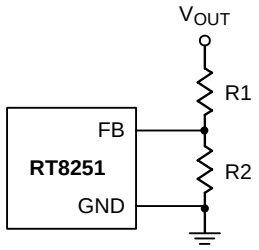


Figure 3. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

Where V_{FB} is the feedback reference voltage (0.8V typ.).

External Bootstrap Diode

Connect a 100nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty cycle is higher than 65%. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

The external 5V can be a 5V fixed input from system or a 5V output of the RT8251.

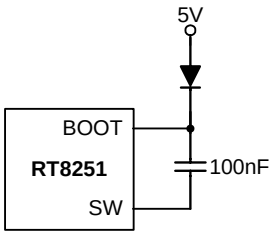


Figure 4. External Bootstrap Diode

Soft-Start

The RT8251 contains an external soft-start clamp that gradually raises the output voltage. The soft-start timming can be set by the external capacitor between SS pin and GND. The chip provides a 10μA charge current for the external capacitor. If 10nF capacitor is used to set the soft-start time, its period will be 1ms (typ.).

Chip Enable Operation

The EN pin is the chip enable input. Pull the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT8251 quiescent current drops to lower than 25μA. Drive the EN pin to high (>1.4V, < 5.5V) will turn on the device again. If the EN pin is open, it will be pulled to high by internal circuit. For external timing control (e.g.RC), the EN pin can also be externally pulled to High by adding a100kΩ or greater resistor from the VIN pin (see Figure 5).

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1-\frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1-\frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor 's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

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Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	SLF10165	10.1x10.1x7
TAIYO YUDEN	NR10050	10x9.8x5
TDK	VLF12060	12x11.7x6

Diode Selection

When the power switch turns off, the path for the current is through the diode connected between the switch output and ground. This forward biased diode must have a minimum voltage drop and recovery times. Schottky diode is recommended and it should be able to handle those current. The reverse voltage rating of the diode should be greater than the maximum input voltage, and current rating should be greater than the maximum load current. For more detail please refer to Table 4.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, two 10µF low ESR ceramic capacitors are recommended. For the recommended capacitor, please refer to table 3 for more detail.

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator

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to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on the SW pin when high-side MOSFET is turned-on/off, this spike voltage on SW may impact on EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One is to place an R-C snubber between SW and GND and make them as close as possible to the SW pin (see Figure 5). Another method is to add a resistor in series with the bootstrap capacitor, C_{BOOT}. But this method will decrease the driving capability to the high-side MOSFET. It is strongly recommended to reserve the R-C snubber during PCB layout for EMI improvement. Moreover, reducing the SW trace area and keeping the main power in a small loop will be helpful on EMI performance. For detailed PCB layout guide, please refer to the section of Layout Consideration.

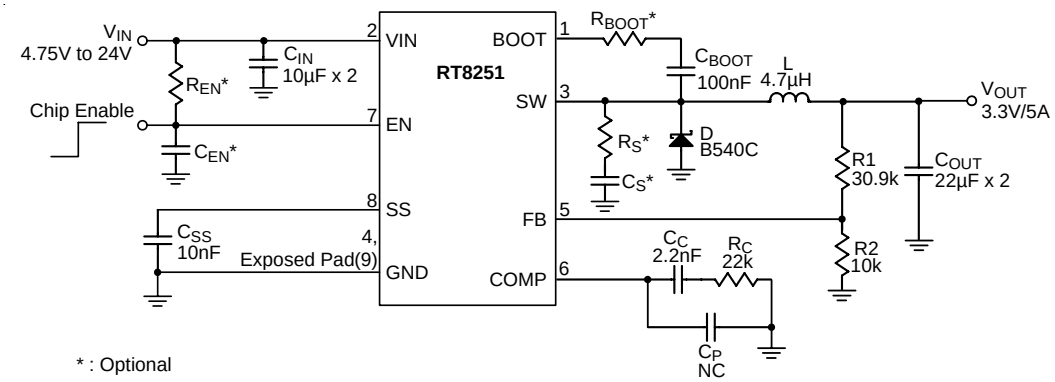


Figure 5. Reference Circuit with Snubber and Enable Timing Control

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8251, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For PSOP-8 and WQFN packages, the thermal resistance θ_{JA} are 75°C/W and 68°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for PSOP-8

$P_{D(MAX)}$ = (125°C – 25°C) / (68°C/W) = 1.471W for WQFN

(min.copper area PCB layout)

$P_{D(MAX)}$ = (125°C – 25°C) / (49°C/W) = 2.04W for PSOP-8 (70mm^{2}copper area PCB layout)

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 6, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard

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SOP-8 (Exposed Pad) pad (Figure 6a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 6.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm² (Figure 6.e) reduces the θ_{JA} to 49°C/W.

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8251 packages, the derating curves in Figure 7 and Figure 8 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

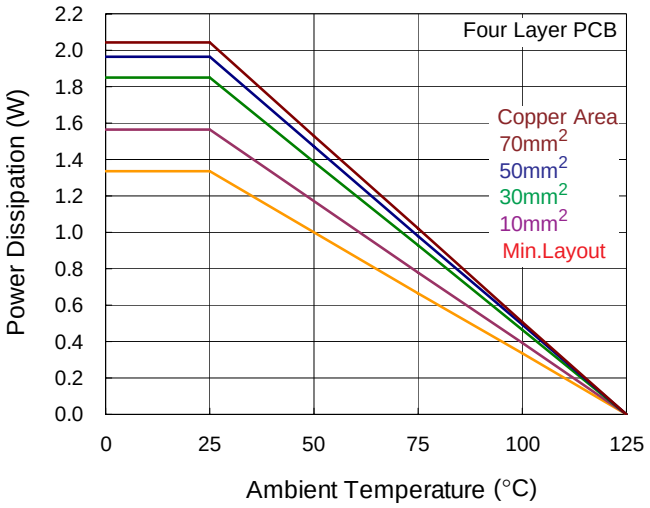


Figure 7. Derating Curves for PSOP-8 Package

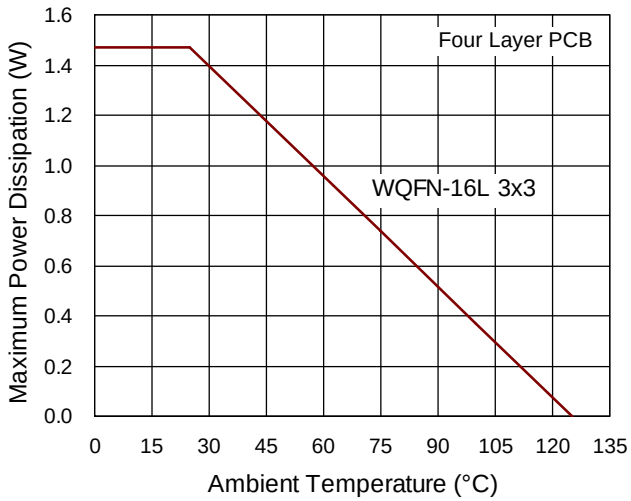
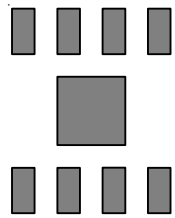
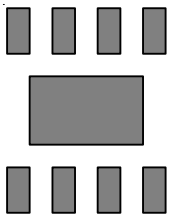


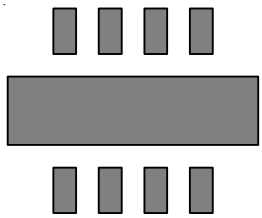
Figure 8. Derating Curves for WQFN Package



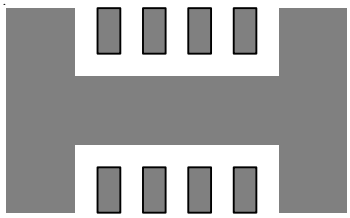
(a) Copper Area = (2.3 x 2.3) mm², θ_{JA} = 75°C/W



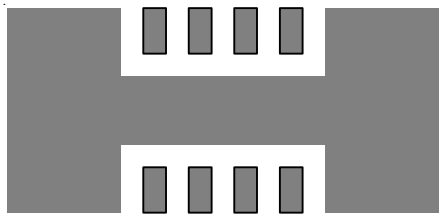
(b) Copper Area = 10mm², θ_{JA} = 64°C/W



(c) Copper Area = 30mm², θ_{JA} = 54°C/W



(d) Copper Area = 50mm², θ_{JA} = 51°C/W



(e) Copper Area = 70mm², θ_{JA} = 49°C/W

Figure 6. Themal Resistance vs. Copper Area Layout Design

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Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT8251.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8251.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.
- Examples of PCB layout guide are shown in Figure 9 and Figure 10 for reference.

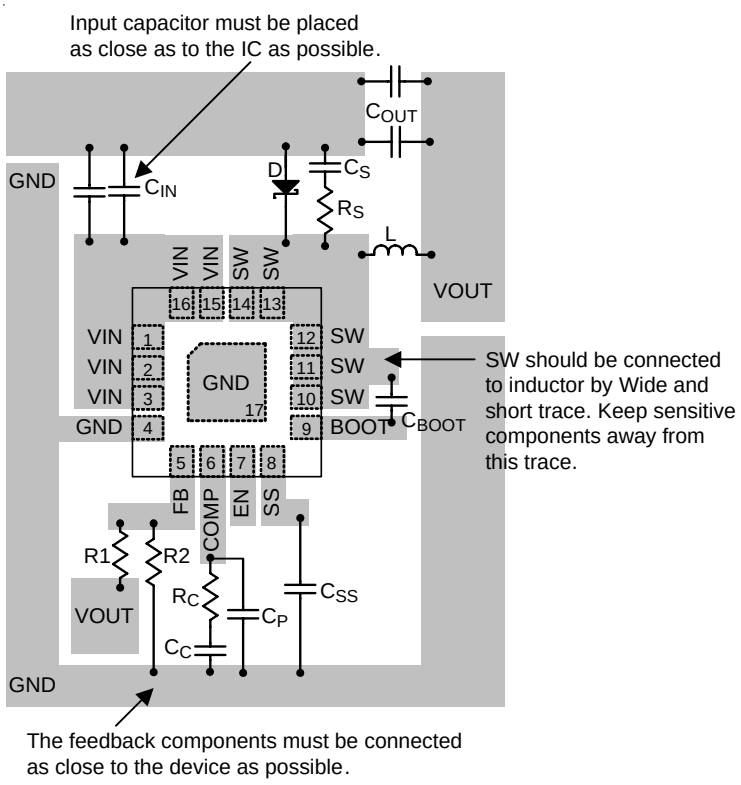


Figure 9. PCB Layout Guide for WQFN Package

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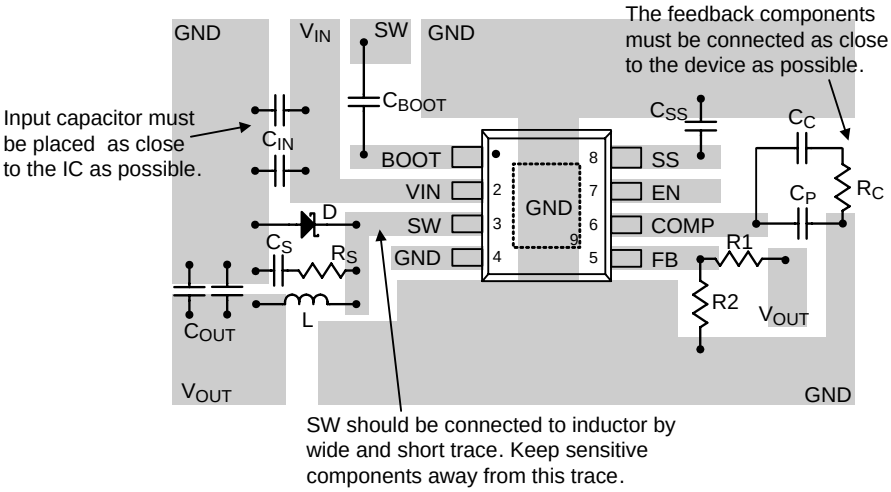


Figure 10. PCB Layout Guide for PSOP-8 Package

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

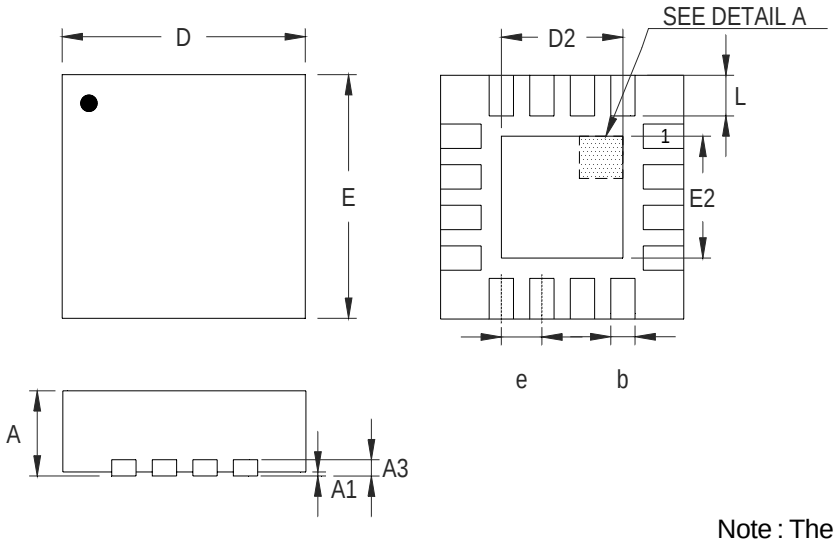
Location	Component Supplier	Part No.	Capacitance (μF)	Case Size
C_{IN}	MURATA	GRM31ER61E226K	22	1210
C_{IN}	TDK	C4535X5R1E226M	22	1812
C_{IN}	TAIYO YUDEN	TMK325BJ226MM	22	1210
C_{OUT}	MURATA	GRM32ER61C476M	47	1210
C_{OUT}	MURATA	GRM31CR60J476M	47	1206
C_{OUT}	TDK	C3216X5R0J476M	47	1206
C_{OUT}	TAIYO YUDEN	LMK316BJ476MM	47	1206

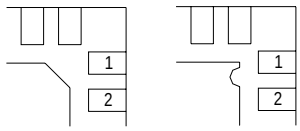
Table 4. Suggested Diode

Component Supplier	Part No.	V_{RRM} (V)	I_{OUT} (A)	Package
DIODES	B540C	40	5	SMC
ON	MBRS540T3	40	5	SMC

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Outline Dimension





DETAIL A

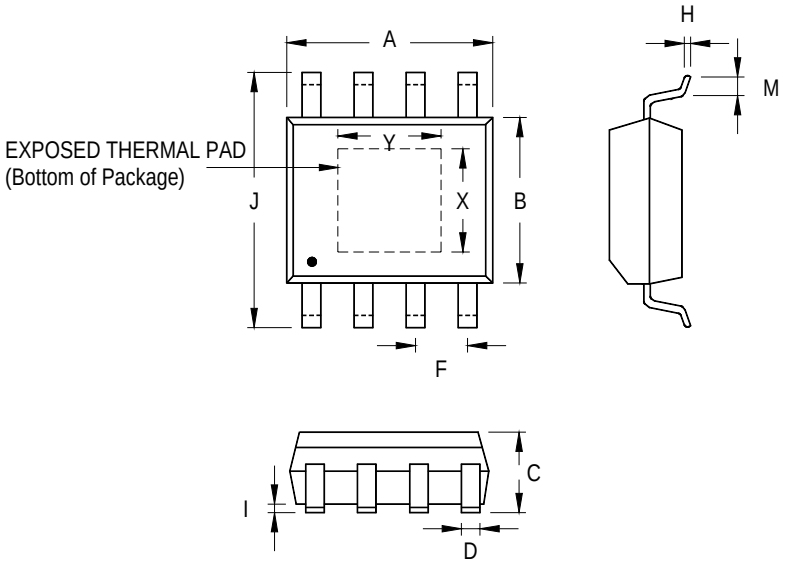
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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