# 1.5A LOAD SWITCH WITH CONTROLLED TURN-ON

## FEATURES

- Integrated 1.5A Single Channel Load Switch
- Input Voltage Range: 0.8V to 5.5V
- Low Threshold Control Input
- Quick Output Discharge Transistor
- Over-Temperature Protection
- Over Current Protection
- Short Circuit Protection
- Open-Drain Fault Flag Output
- Low ON-Resistance $R_{ON}$ = 40mΩ
- Halogen Free Product

## APPLICATIONS

- Telecom Systems
- Set-Top-Box
- Consumer Electronics
- Notebooks / Netbooks

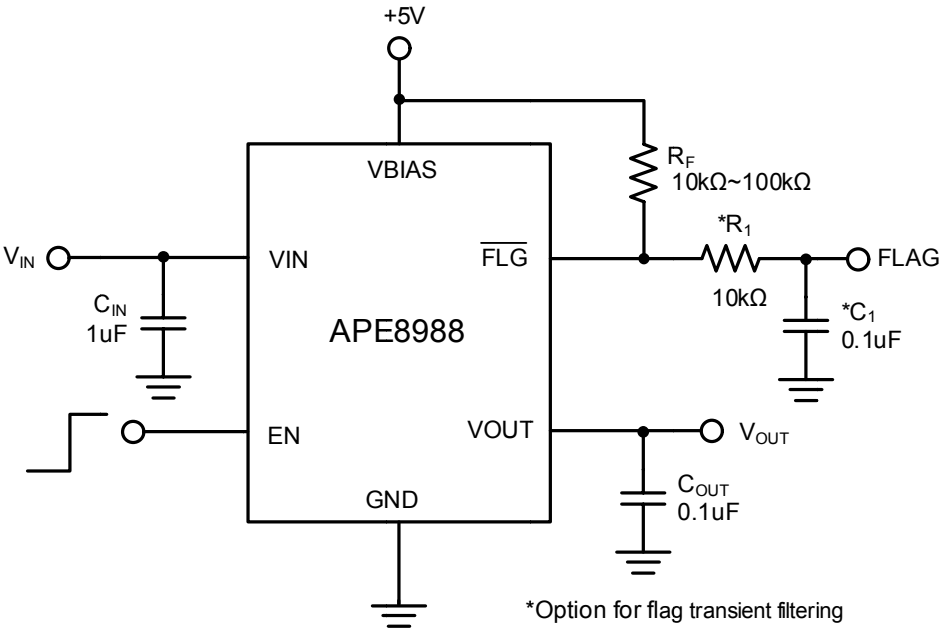
## DESCRIPTION

The APE8988 is a low $R_{ON}$ load switch with controlled turn on. It contains one N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.5V and support maximum continuous current up to 1.5A. The switch is controlled by an on/off input (EN), which is capable of interfacing directly with low-voltage control signals.

Additional features include a 330Ω on-chip load resistor is added for output quick discharge when switch is turned off. A well protection is equipped when the device enters hard short circuit and thermal shutdown.

The APE8988 is available in small SOT-26 package with smallest components.

## TYPICAL APPLICATION

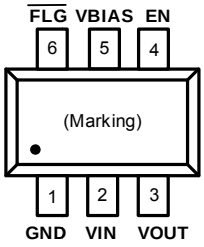


## ORDERING / PACKAGE INFORMATION

APE8988X

Package Type
Y: SOT-26

Top View
SOT-26




## ABSOLUTE MAXIMUM RATINGS (at $T_A$=25°C)

| | |
|---|---|
| VIN | -0.3V to 6V |
| VBIAS | -0.3 to 6V |
| VOUT | VIN+0.3V |
| EN, /FLG | -0.3V to 6V |
| Storage Temperature Range ($T_{ST}$) | -65 to +150°C |
| Junction Temperature ($T_J$) | 150°C |
| Lead Temperature (Soldering, 10sec.) | 260°C |
| Thermal Resistance from Junction to Ambient ($R\theta_{JA}$) | |
| SOT-26 | 250°C/W |

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| VIN | 0.8V to 5.5V |
| VBIAS | 4.5V to 5.5V (VBIAS≧VIN) |
| VOUT | $V_{IN}$ |
| CIN | ≧0.1uF |
| Junction Temperature ($T_J$) | 125°C |
| Operating Temperature Range ($T_A$) | -40°C to 85°C |

## ELECTRICAL SPECIFICATIONS

($V_{IN}$=0.8V to 5.5V, $V_{BIAS}$=5V, $C_{IN}$=1uF, $C_{OUT}$=0.1uF, $T_A$ =25°C, unless otherwise specified)

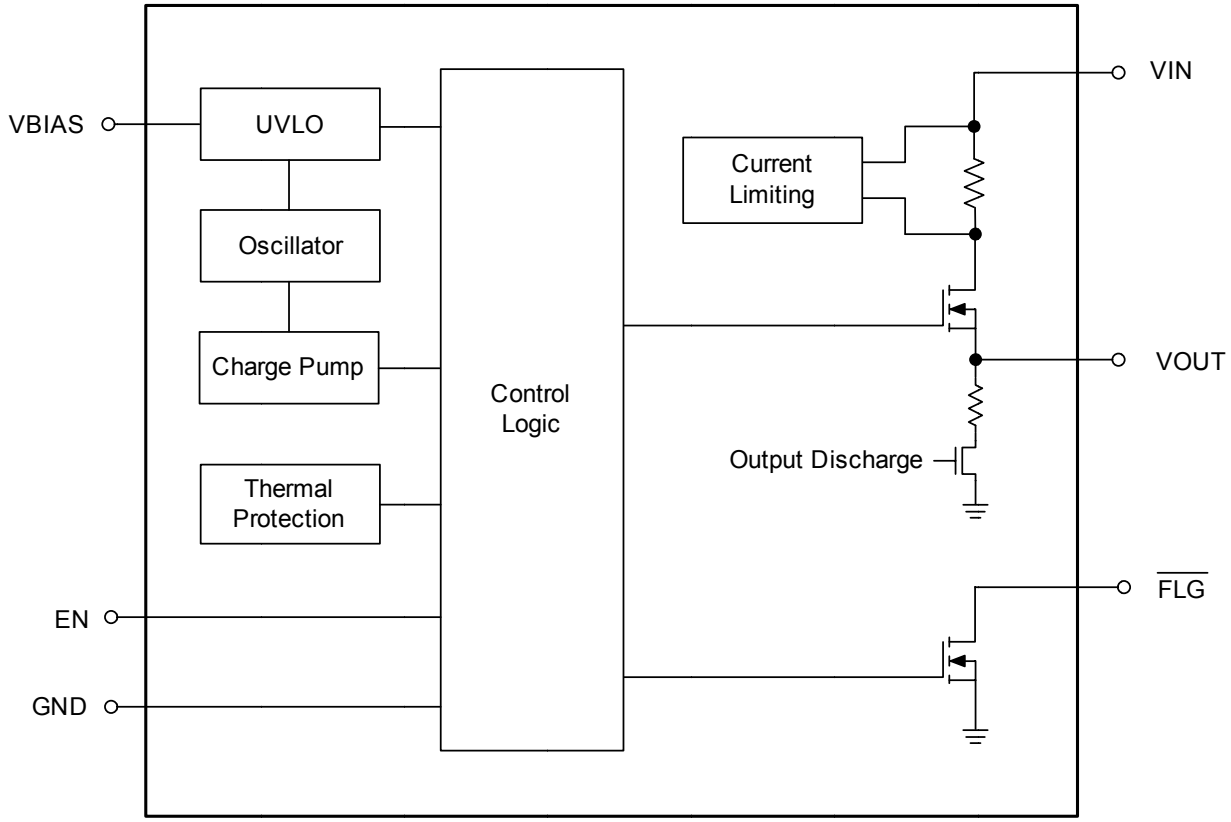
| PARAMETER | SYM | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Quiescent Current | $I_{BIAS}$ | $V_{EN}$=5V, $I_{OUT}$=0A | | 30 | 50 | uA |
| Shutdown Current | $I_{SD}$ | $V_{EN}$=GND | | | 1 | uA |
| Under-Voltage Lockout | $V_{UVLO}$ | Threshold | 3.0 | 3.6 | 4.2 | V |
| | $V_{HYS}$ | Hysteresis | | 0.4 | | V |
| Switch ON Resistance | $R_{ON}$ | $V_{EN}$=$V_{BIAS}$, $I_{OUT}$=200mA | | 40 | 50 | mΩ |
| Current Limit Threshold | $I_{LM}$ | | 1.8 | | | A |
| VOUT Rise Time | $t_{SS}$ | $V_{IN}$=5V | | 650 | | us |
| Output Pull-Down Resistance | $R_{OPD}$ | $V_{IN}$=5V, $V_{EN}$=0V | | 330 | 400 | Ω |
| FLAG Delay Time (Note1) | $t_{DELAY}$ | from fault condition to FLAG assert | | 3 | | ms |
| FLAG ON Resistance | $R_{FLG}$ | | | 20 | 50 | Ω |
| EN Input Leakage Current | $I_{EN}$ | $V_{EN}$=5V or GND | | | 1 | uA |
| EN Threshold | $V_{IH}$ | on | 1.6 | | | V |
| | $V_{IL}$ | off | | | 0.6 | V |
| Thermal Shutdown Threshold (Note1) | $T_{SD}$ | | | 140 | | °C |
| | | Hysteresis | | 30 | | °C |

Note1: Guarantee by design, not production tested.

## PIN DESCRIPTIONS

| PIN No. | PIN SYMBOL | PIN DESCRIPTION |
|---|---|---|
| 1 | GND | Ground. |
| 2 | VIN | Input Power Supply. |
| 3 | VOUT | Switch output. |
| 4 | EN | Switch control input, active high. Do not leave floating. |
| 5 | VBIAS | Bias Voltage. |
| 6 | /FLG | Open-drain fault flag output. |

## BLOCK DIAGRAM



## TYPICAL PERFORMANCE CHARACTERISTICS

$C_{IN}$=1μF, $C_{OUT}$=0.1μF, Io=0A, ch1: $V_{EN}$, ch2: $V_{OUT}$, ch3: /FLG, ch4: $I_{IN}$

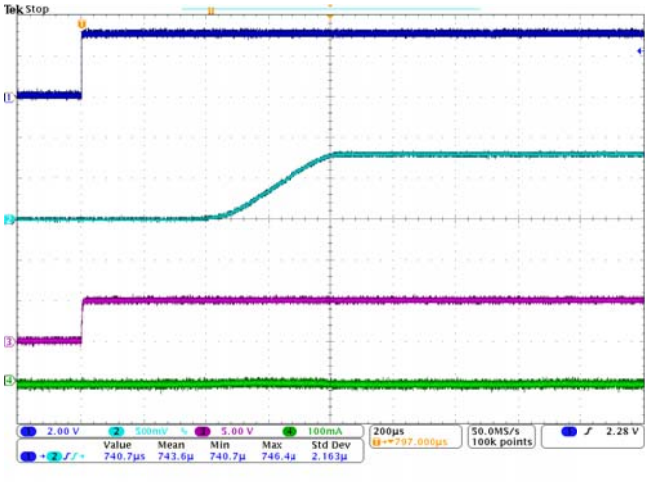


Fig.1 Turn-on Response, VIN=0.8V

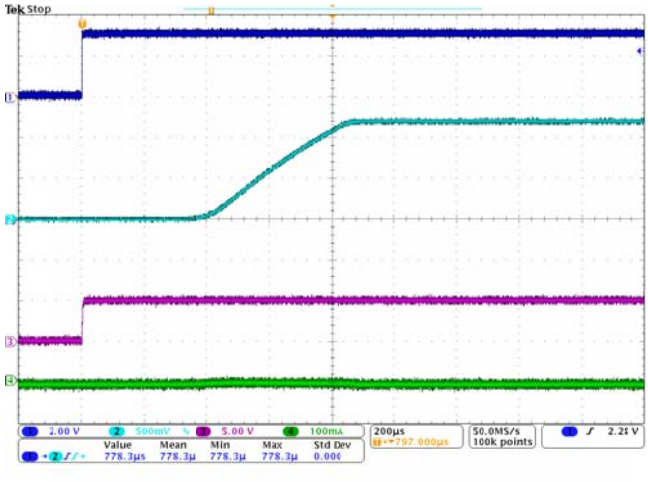


Fig.2 Turn-on Response, VIN=1.2V

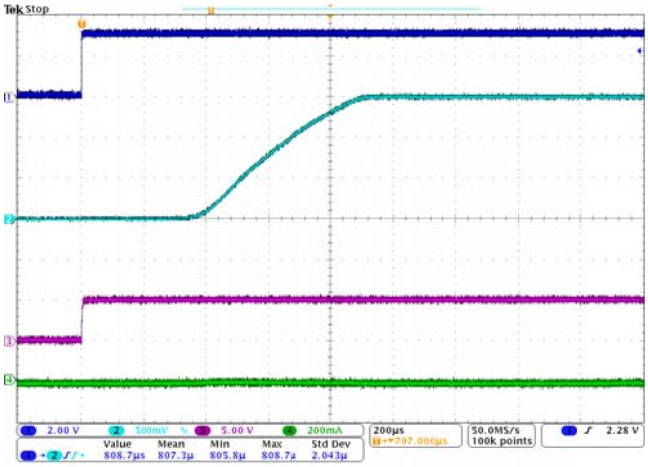


Fig.3 Turn-on Response, VIN=1.5V

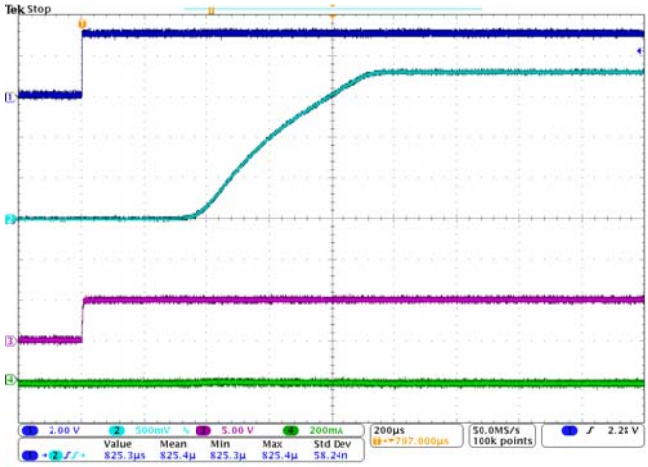


Fig.4 Turn-on Response, VIN=1.8V

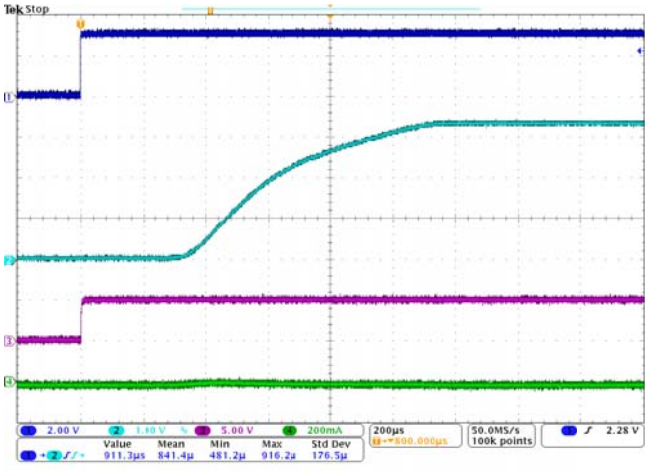


Fig.5 Turn-on Response, VIN=3.3V

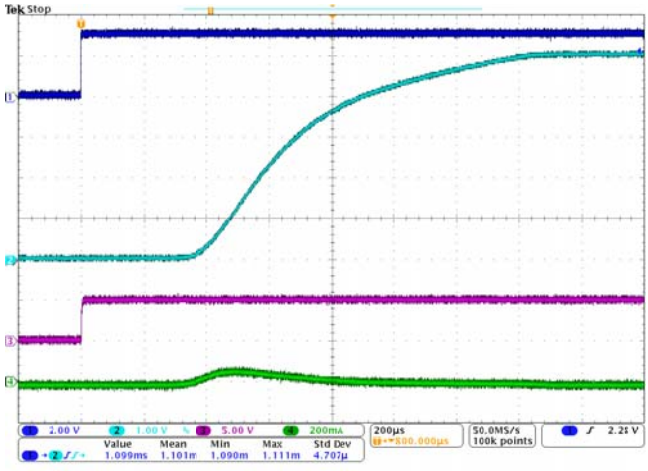


Fig.6 Turn-on Response, VIN=5.0V

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

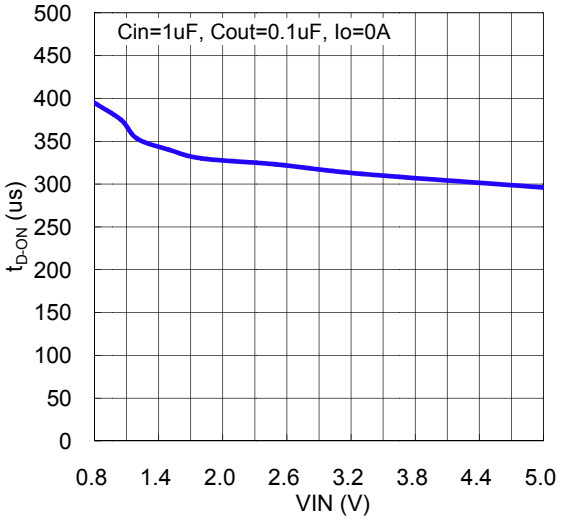



Fig.7 Turn-on Delay Time vs. VIN

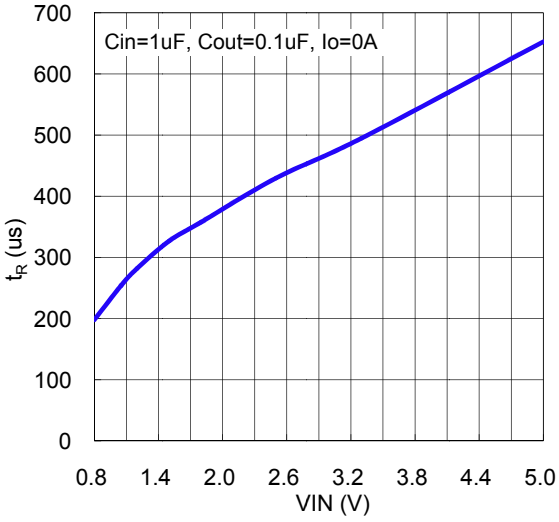



Fig.8 VOUT Rise Time vs. VIN

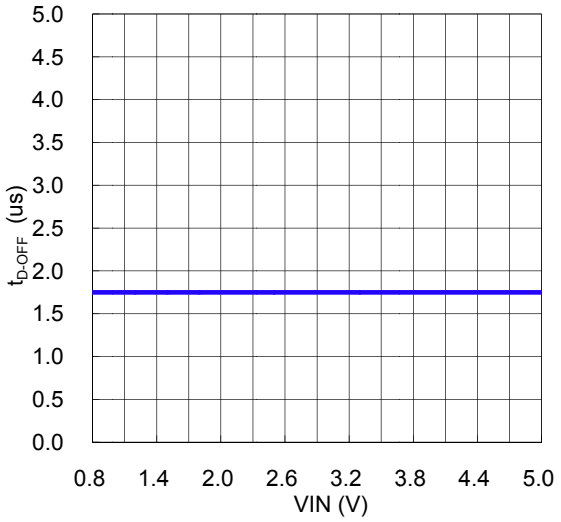



Fig.9 Turn-off Delay Time vs. VIN

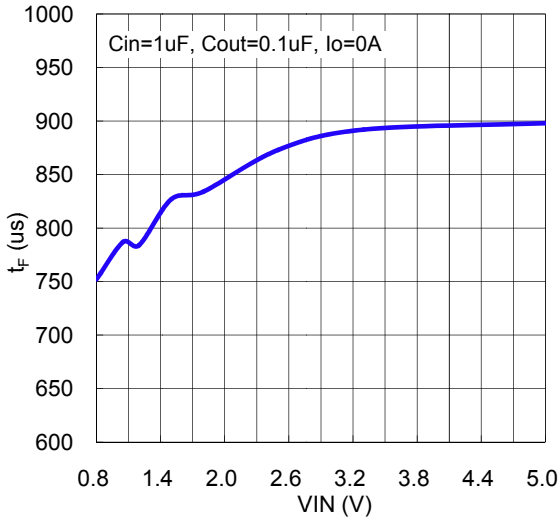



Fig.10 VOUT Fall Time vs. VIN

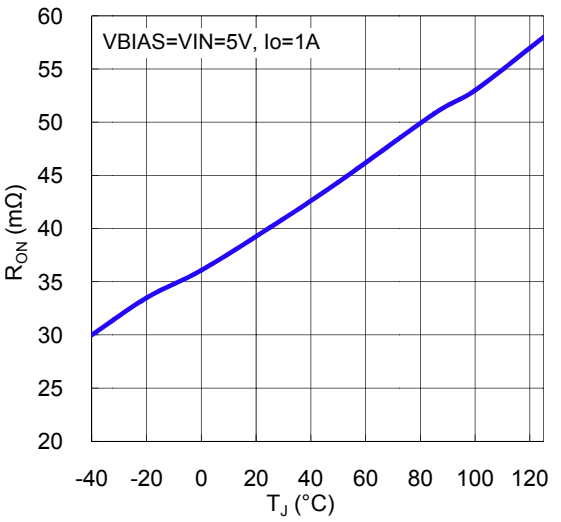



Fig.11 $R_{ON}$ vs. Temperature

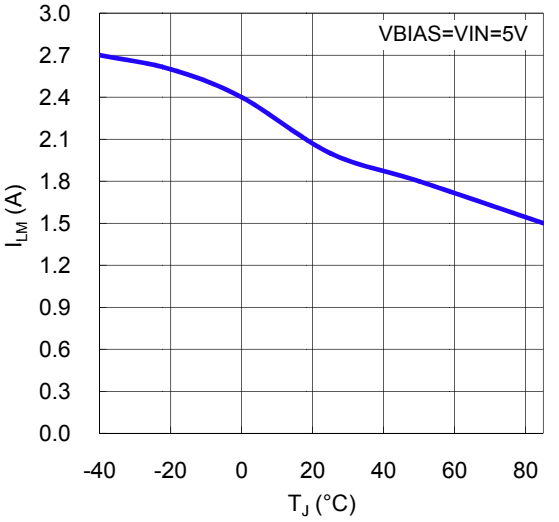



Fig.12 Current Limit vs. Temperature

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

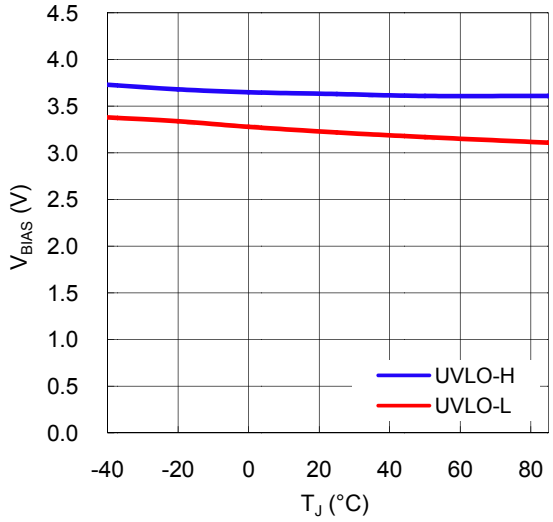



Fig.13 UVLO Threshold vs. Temperature

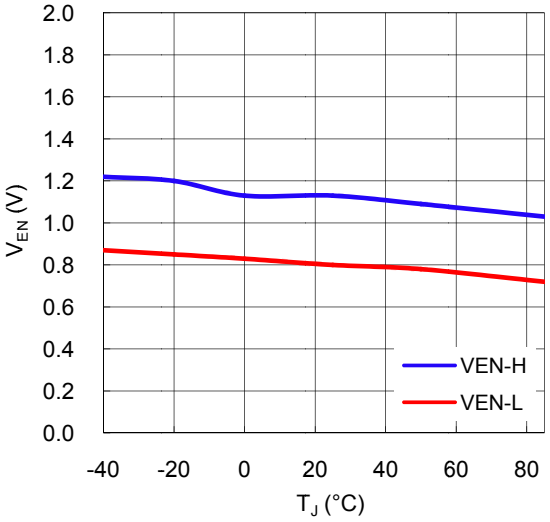



Fig.14 EN Threshold vs. Temperature

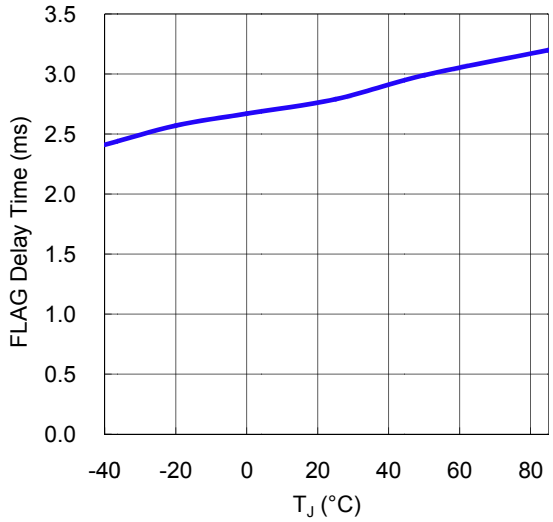



Fig.15 FLAG Delay Time vs. Temperature

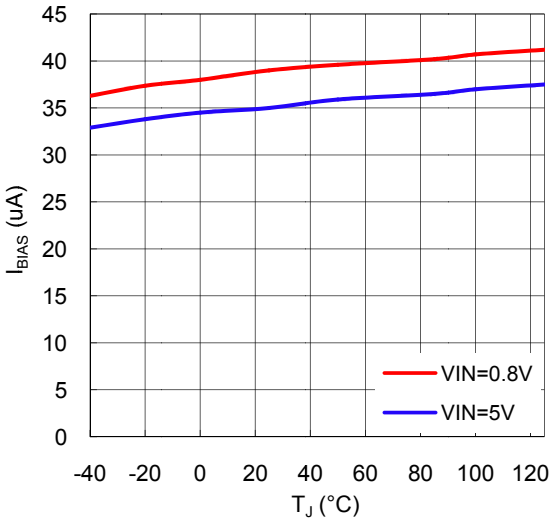



Fig.16 VBIAS Current vs. Temperature

## APPLICATION INFORMATION

### On/Off Control

The load switch is controlled by the EN pin. The EN pin is active high and has a low threshold making it capable of interfacing with low voltage signals. The EN pin can be used with standard 1.8V, 2.5V or 3.3V GPIO logic threshold. Do not leave the EN pin float.

The Figure17 shows the VOUT on/off definition.

$t_{D-ON}$: VOUT turn-on delay time

$t_R$: VOUT rise time

$t_{D-OFF}$: VOUT turn-off delay time

$t_F$: VOUT fall time

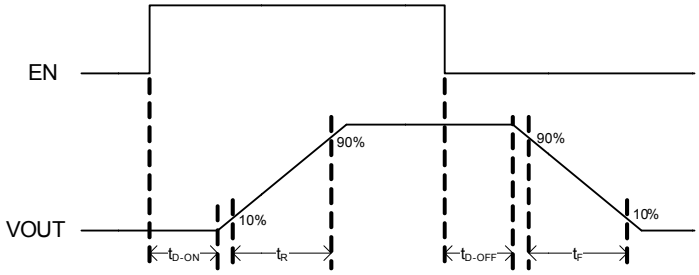



Fig.17 ON/OFF Waveform

### FLAG Indicator

The APE8988 provides an error indicator (/FLG) output, which is an open-drain output requiring a pull-up resistor. Typically connect to +5V bias supply through a 10kΩ resistor. The FLAG comparator continuously monitors the fault condition for over current, short circuit and thermal shutdown conditions. If the fault condition keeps for 3ms, /FLG becomes low immediately.

### Input Capacitor

An input capacitor is recommended to be placed between VIN and GND to limit the voltage drop on the input supply during high current application.

### Output Capacitor

Setting a $C_{IN}$ greater than the $C_{OUT}$ is highly recommended. Since the internal body diode is in the NMOS switch, this prevents the current flows through the body diode from VOUT to VIN when the system supply is removed.

## APPLICATION INFORMATION (Continued)

**Layout Considerations**

Follow the below guidelines for PCB layout to achieve stable operation. Take below figure for reference.

1. Keep the high current paths (VIN, VOUT and GND) wide and short to obtain the best effect.
2. The input and output capacitors should be close to the device as possible to minimize the parasitic trace inductances.

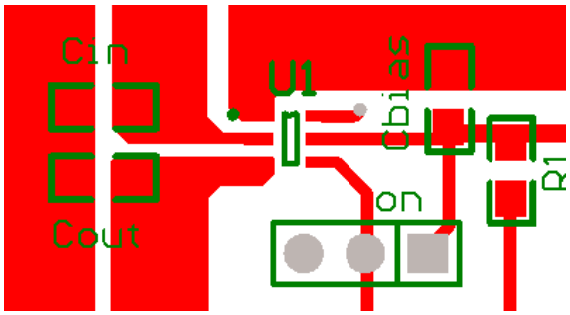



Fig.18 Reference layout

## MARKING INFORMATION

**SOT-26**

