High Voltage Synchronous Rectified Buck MOSFET Drivers

ISL6208, ISL6208B

The ISL6208 and ISL6208B are high frequency, dual MOSFET drivers, optimized to drive two N-Channel power MOSFETs in a synchronous-rectified buck converter topology. They are especially suited for mobile computing applications that require high efficiency and excellent thermal performance. These drivers, combined with an Intersil multiphase Buck PWM controller, form a complete single-stage core-voltage regulator solution for advanced mobile microprocessors.

ISL6208 and ISL6208B have the same function but different packages. The descriptions in this datasheet are based on ISL6208 and also apply to ISL6208B.

The ISL6208 features 4A typical sinking current for the lower gate driver. This current is capable of holding the lower MOSFET gate off during the rising edge of the Phase node. This prevents shoot-through power loss caused by the high dv/dt of phase voltages. The operating voltage matches the 30V breakdown voltage of the MOSFETs commonly used in mobile computer power supplies.

The ISL6208 also features a three-state PWM input that, working together with Intersil's multiphase PWM controllers, will prevent negative voltage output during CPU shutdown. This feature eliminates a protective Schottky diode usually seen in a microprocessor power systems.

MOSFET gates can be efficiently switched up to 2MHz using the ISL6208. Each driver is capable of driving a 3000pF load with propagation delays of 8ns and transition times under 10ns. Bootstrapping is implemented with an internal Schottky diode. This reduces system cost and complexity, while allowing the use of higher performance MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

A diode emulation feature is integrated in the ISL6208 to enhance converter efficiency at light load conditions. This feature also allows for monotonic start-up into pre-biased outputs. When diode emulation is enabled, the driver will allow discontinuous conduction mode by detecting when the inductor current reaches zero and subsequently turning off the low side MOSFET gate.

Features

- Dual MOSFET drives for synchronous rectified bridge
- Adaptive shoot-through protection
- 0.5Ω On-resistance and 4A sink current capability
- Supports high switching frequency up to 2MHz
  - Fast output rise and fall time
  - Low propagation delay
- Three-state PWM input for power stage shutdown
- Internal bootstrap schottky diode
- Low bias supply current (5V, 80µA)
- Diode emulation for enhanced light load efficiency and pre-biased start-up applications
- VCC POR (power-on-reset) feature integrated
- Low three-state shutdown holdoff time (typical 160ns)
- Pin-to-pin compatible with ISL6207
- QFN and DFN package:
  - Compliant to JEDEC PUB95 MO-220
    QFN - Quad flat no leads - package outline
    DFN - Dual flat no leads - package outline
  - Near chip scale package footprint, which improves PCB efficiency and has a thinner profile
- Pb-free (RoHS compliant)

Applications

- Core voltage supplies for Intel® and AMD® mobile microprocessors
- High frequency low profile DC/DC converters
- High current low output voltage DC/DC converters
- High input voltage DC/DC converters

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Technical Brief TB389 "PCB Land Pattern Design and Surface Mount Guidelines for MLFP Packages"
- Technical Brief TB447 "Guidelines for Preventing Boot-to-Phase Stress on Half-Bridge MOSFET Driver ICs"

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

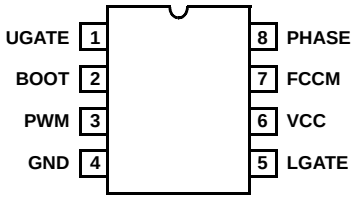
PART NUMBER (Notes 3, 4)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6208CBZ (Note 1)	ISL62 08CBZ	-10 to +100	8 Ld SOIC	M8.15
ISL6208CRZ (Note 1)	208Z	-10 to +100	8 Ld 3x3 QFN	L8.3x3
ISL6208BCRZ-T (Note 2)	8BC	-10 to +100	8 Ld 2x2 DFN	L8.2x2D
ISL6208IBZ (Note 1)	ISL62 08IBZ	-40 to +100	8 Ld SOIC	M8.15
ISL6208IRZ (Note 1)	8IRZ	-40 to +100	8 Ld 3x3 QFN	L8.3x3
ISL6208BIRZ-T (Note 2)	8BI	-40 to +100	8 Ld 2x2 DFN	L8.2x2D

NOTES:

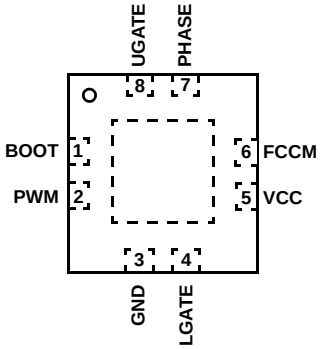
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL6208, ISL6208B. For more information on MSL please see techbrief TB363.

Pin Configurations

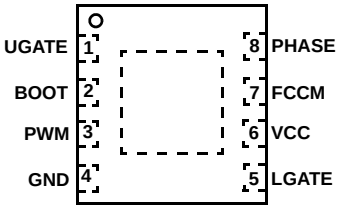
ISL6208CBZ, ISL6208IBZ
(8 LD SOIC)
TOP VIEW



ISL6208CRZ, ISL6208IRZ
(8 LD 3x3 QFN)
TOP VIEW



ISL6208BCRZ, ISL6208BIRZ
(8 LD 2x2 DFN)
TOP VIEW



Block Diagram

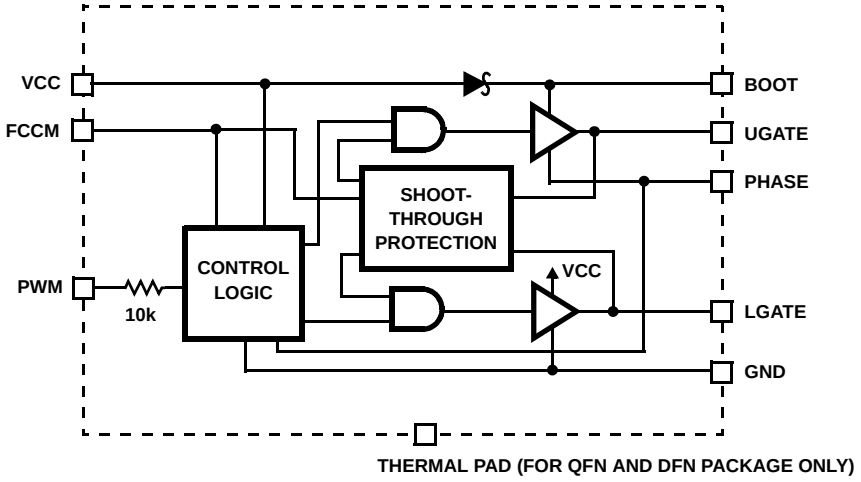


FIGURE 1. BLOCK DIAGRAM

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to 7V
Input Voltage (V_{FCCM}, V_{PWM}) . . . . . -0.3V to VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . . . -0.3V to 33V
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V (DC)
-0.3V to 9V (<10ns)
PHASE Voltage (Note 5) . . . . . GND - 0.3V to 30V
GND - 10V (<20ns Pulse Width, 10µJ)
UGATE Voltage . . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
V_{PHASE} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . . GND - 0.3V (DC) to VCC + 0.3V
GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V
Ambient Temperature Range . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 6, 9)	110	67
8 Ld 3x3 QFN Package (Notes 7, 8)	80	15
8 Ld 2x2 DFN Package (Notes 7, 8)	89	24

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . . . -10°C to +100°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, VCC . . . . . 5V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. The Phase Voltage is capable of withstanding -7V when the BOOT pin is at GND.
6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
8. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
9. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply across the operating temperature range.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
V_{CC} SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	PWM pin floating, V_{FCCM} = 5V	-	80	-	µA
POR						
V_{CC} Rising			-	3.40	**3.90**	V
V_{CC} Falling			**2.40**	2.90	-	V
Hysteresis			-	500	-	mV
BOOTSTRAP DIODE						
Forward Voltage	V_F	V_{VCC} = 5V, forward bias current = 2mA	**0.50**	0.55	**0.65**	V
PWM INPUT						
Input Current	I_{PWM}	V_{PWM} = 5V	-	250	-	µA
		V_{PWM} = 0V	-	-250	-	µA
PWM Three-State Rising Threshold		V_{VCC} = 5V	**0.70**	1.00	**1.30**	V
PWM Three-State Falling Threshold		V_{VCC} = 5V	**3.5**	3.8	**4.1**	V
Three-State Shutdown Hold-off Time	t_{TSSHD}	V_{VCC} = 5V, temperature = +25°C	100	175	250	ns
FCCM INPUT						
FCCM LOW Threshold			**0.50**	-	-	V
FCCM HIGH Threshold			-	-	**2.0**	V
SWITCHING TIME						
UGATE Rise Time (Note 10)	t_{RU}	V_{VCC} = 5V, 3nF load	-	8.0	-	ns
LGATE Rise Time (Note 10)	t_{RL}	V_{VCC} = 5V, 3nF load	-	8.0	-	ns
UGATE Fall Time (Note 10)	t_{FU}	V_{VCC} = 5V, 3nF load	-	8.0	-	ns

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply across the operating temperature range.**

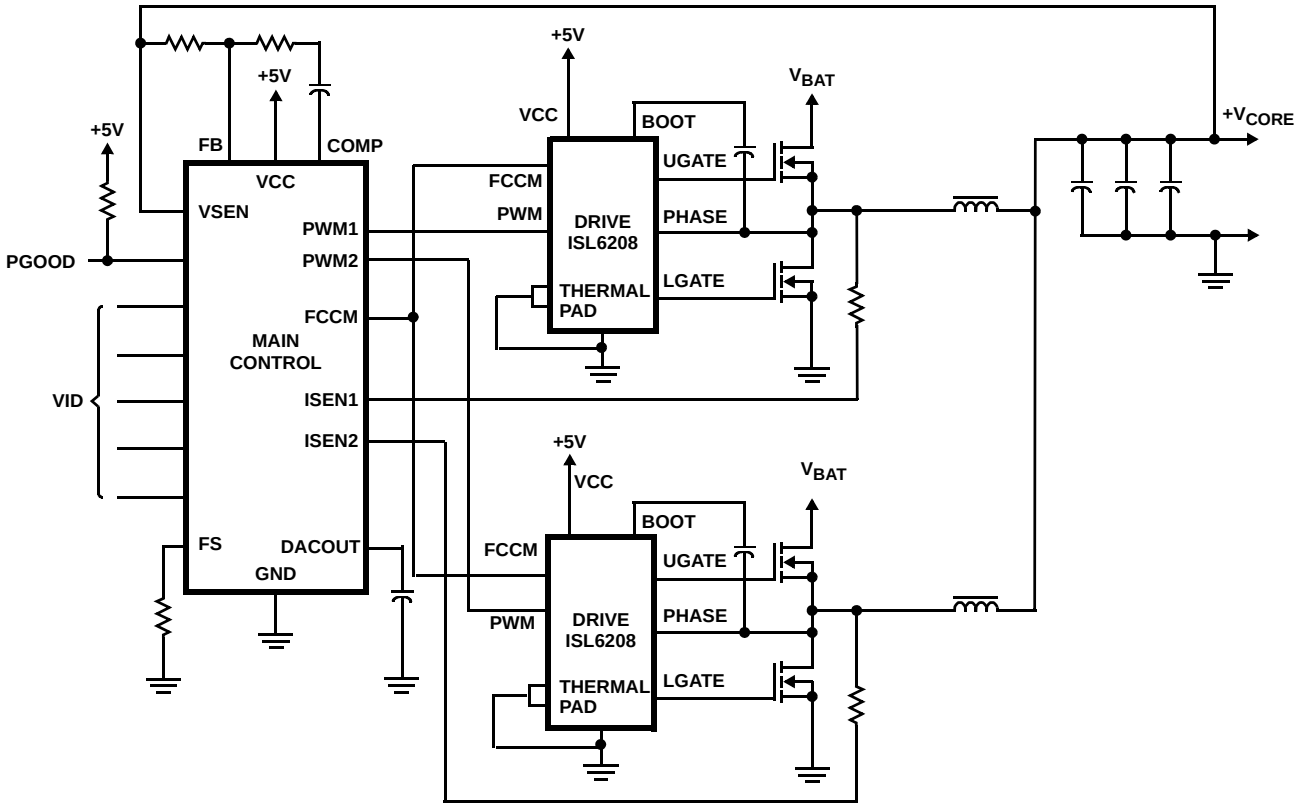
PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
LGATE Fall Time (Note 10)	t_{FL}	V_{VCC} = 5V, 3nF load	-	4.0	-	ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	V_{VCC} = 5V, outputs unloaded	-	18	-	ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	V_{VCC} = 5V, outputs unloaded	-	25	-	ns
UGATE Turn-On Propagation Delay	t_{PDHU}	V_{VCC} = 5V, outputs unloaded	**10**	20	**30**	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	V_{VCC} = 5V, outputs unloaded	**10**	20	**30**	ns
UG/LG Three-State Propagation Delay	t_{PTS}	V_{VCC} = 5V, outputs unloaded	-	35	-	ns
Minimum LG ON-TIME in DCM (Note 10)	t_{LGMIN}		-	400	-	ns
OUTPUT						
Upper Drive Source Resistance	R_U	500mA source current	-	1	**2.5**	Ω
Upper Driver Source Current (Note 10)	I_U	$V_{UGATE-PHASE}$ = 2.5V	-	2.00	-	A
Upper Drive Sink Resistance	R_U	500mA sink current	-	1	**2.5**	Ω
Upper Driver Sink Current (Note 10)	I_U	$V_{UGATE-PHASE}$ = 2.5V	-	2.00	-	A
Lower Drive Source Resistance	R_L	500mA source current	-	1	**2.5**	Ω
Lower Driver Source Current (Note 10)	I_L	V_{LGATE} = 2.5V	-	2.00	-	A
Lower Drive Sink Resistance	R_L	500mA sink current	-	0.5	**1.0**	Ω
Lower Driver Sink Current (Note 10)	I_L	V_{LGATE} = 2.5V	-	4.00	-	A

NOTES:

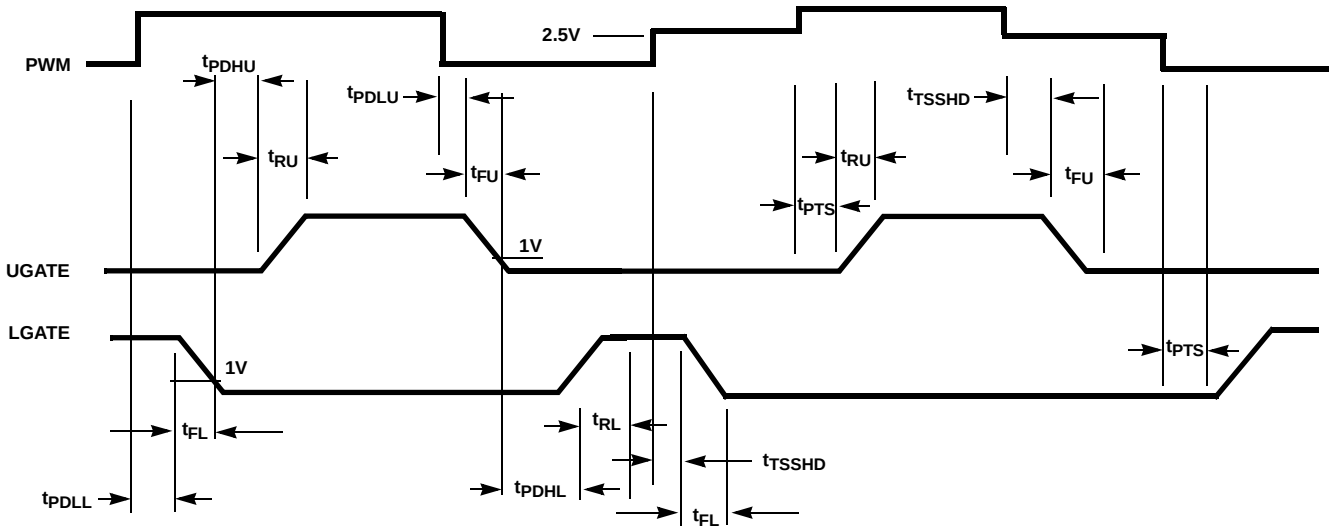
10. Limits established by characterization and are not production tested.

11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Application with 2-Phase Converter



Timing Diagram



Functional Pin Description

UGATE

The UGATE pin is the upper gate drive output. Connect to the gate of high-side power N-Channel MOSFET.

BOOT

BOOT is the floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See "Internal Bootstrap Diode" on page 8 for guidance in choosing the appropriate capacitor value.

PWM

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation. See "Three-State PWM Input" on page 8 for further details. Connect this pin to the PWM output of the controller.

GND

GND is the ground pin for the IC.

LGATE

LGATE is the lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.

VCC

Connect the VCC pin to a +5V bias supply. Place a high quality bypass capacitor from this pin to GND.

FCCM

The FCCM pin enables or disables Diode Emulation. When FCCM is LOW, diode emulation is allowed. Otherwise, continuous conduction mode is forced. See "Diode Emulation" on page 8 for more detail.

PHASE

Connect the PHASE pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.

Description

Theory of Operation

Designed for speed, the ISL6208 dual MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising edge on PWM initiates the turn-off of the lower MOSFET (see "Timing Diagram"). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the "Electrical Specifications" on page 3. Adaptive shoot-through circuitry monitors the LGATE voltage. When LGATE has fallen below 1V, UGATE is allowed to turn ON. This prevents both the lower and upper MOSFETs from conducting simultaneously, or shoot-through.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The upper MOSFET gate-to-source voltage is monitored, and the lower gate is allowed to rise after the upper MOSFET gate-to-source voltage drops below 1V. The lower gate then rises [t_{RL}], turning on the lower MOSFET.

This driver is optimized for converters with large step-down compared to the upper MOSFET because the lower MOSFET conducts for a much longer time in a switching period. The lower gate driver is therefore sized much larger to meet this application requirement.

The 0.5Ω ON-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected to the lower gate through the drain-to-gate capacitor of the lower MOSFET and prevent a shoot-through caused by the high dv/dt of the phase node.

Typical Performance Waveforms

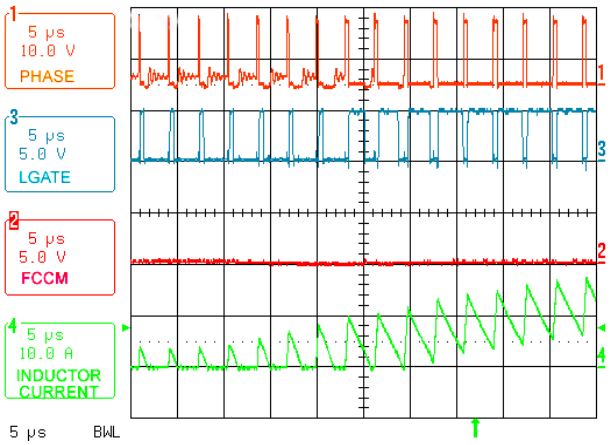


FIGURE 2. LOAD TRANSIENT (0 - 30A, 3-PHASE)

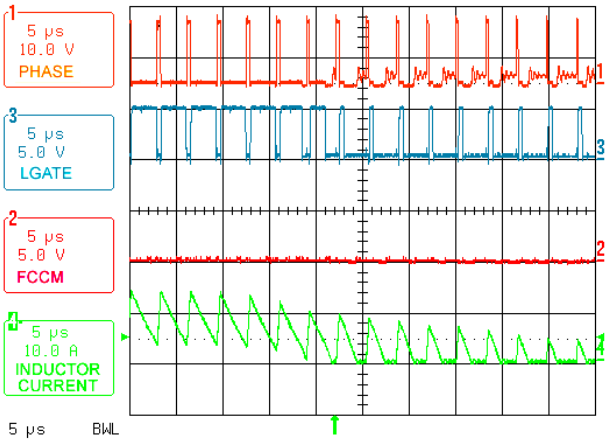


FIGURE 3. LOAD TRANSIENT (30 - 0A, 3-PHASE)

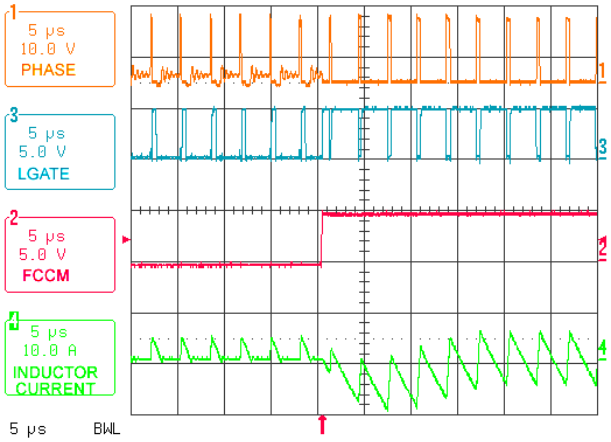


FIGURE 4. DCM TO CCM TRANSITION AT NO LOAD

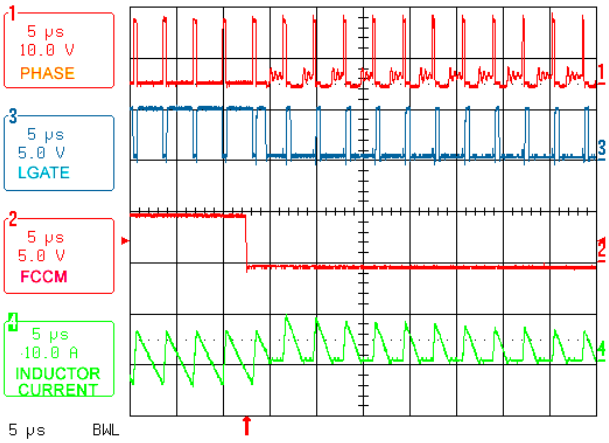


FIGURE 5. CCM TO DCM TRANSITION AT NO LOAD

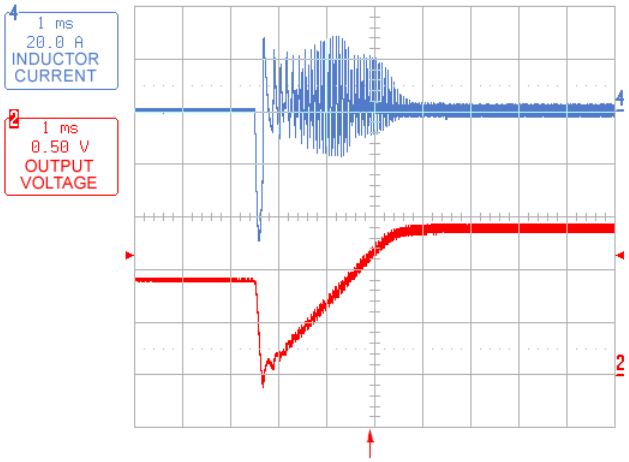


FIGURE 6. PRE-BIASED START-UP IN CCM MODE

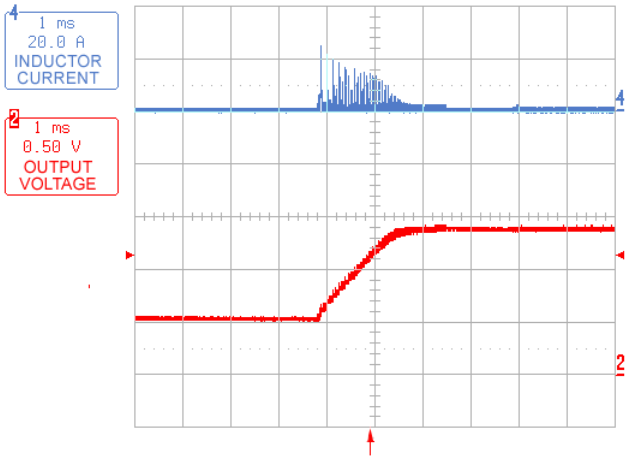


FIGURE 7. PRE-BIASED START-UP IN DCM MODE

Diode Emulation

Diode emulation allows for higher converter efficiency under light load situations. With diode emulation active, the ISL6208 will detect the zero current crossing of the output inductor and turn off LGATE. This ensures that discontinuous conduction mode (DCM) is achieved. Diode emulation is asynchronous to the PWM signal. Therefore, the ISL6208 will respond to the FCCM input immediately after it changes state. Refer to"Typical Performance Waveforms" on page 7.

Note: Intersil does not recommend Diode Emulation use with $r_{DS(ON)}$ current sensing topologies. The turn-OFF of the low side MOSFET can cause gross current measurement inaccuracies.

Three-State PWM Input

A unique feature of the ISL6208 and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the "Electrical Specifications" table on page 3 determine when the lower and upper gates are enabled.

Adaptive Shoot-Through Protection

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to turn on.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 1V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the upper MOSFET gate-to-source voltage during UGATE turn-off. Once the upper MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise.

Internal Bootstrap Diode

This driver features an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

The bootstrap capacitor must have a maximum voltage rating above the maximum battery voltage plus 5V. The bootstrap capacitor can be chosen from Equation 1:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \quad \text{(EQ. 1)}$$

where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose an upper MOSFET has a gate charge, Q_{GATE}, of 25nC at 5V and also assume the droop in the drive voltage over a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance is 0.15µF. A good quality ceramic capacitor is recommended.

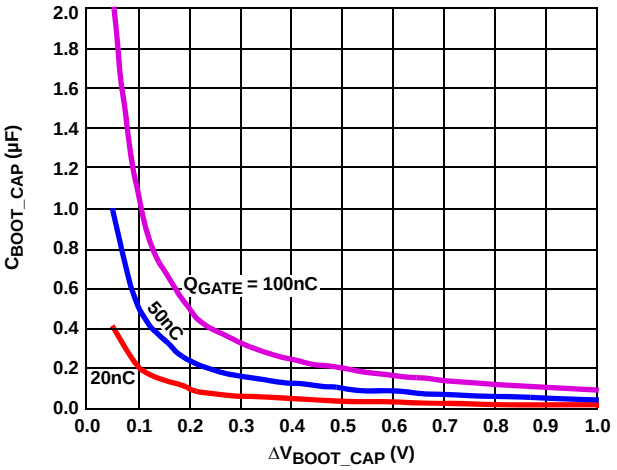


FIGURE 8. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Power Dissipation

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the SO-8 package is approximately 800mW. When designing the driver into an application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the driver is approximated as shown in Equation 2:

$$P = f_{sw}(1.5V_U Q_U + V_L Q_L) + I_{VCC} V_{CC} \quad \text{(EQ. 2)}$$

where f_{sw} is the switching frequency of the PWM signal. V_U and V_L represent the upper and lower gate rail voltage. Q_U and Q_L is the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The I_{VCC} V_{CC} product is the quiescent power of the driver and

is typically negligible.

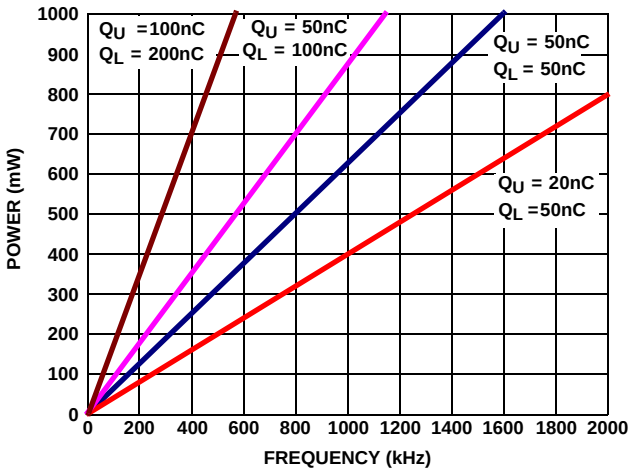


FIGURE 9. POWER DISSIPATION vs FREQUENCY

Layout Considerations

Reducing Phase Ring

The parasitic inductances of the PCB and power devices (both upper and lower FETs) could cause increased PHASE ringing, which may lead to voltages that exceed the absolute maximum rating of the devices. When PHASE rings below ground, the negative voltage could add charge to the bootstrap capacitor through the internal bootstrap diode. Under worst-case conditions, the added charge could overstress the BOOT and/or PHASE pins. To prevent this from happening, the user should perform a careful layout inspection to reduce trace inductances, and select low lead inductance MOSFETs and drivers. D^2PAK and DPAK packaged MOSFETs have high parasitic lead inductances, as opposed to SO-8. If higher inductance MOSFETs must be used, a Schottky diode is recommended across the lower MOSFET to clamp negative PHASE ring.

A good layout would help reduce the ringing on the phase and gate nodes significantly:

- Avoid using vias for decoupling components where possible, especially in the BOOT-to-PHASE path. Little or no use of vias for VCC and GND is also recommended. Decoupling loops should be short.
- All power traces (UGATE, PHASE, LGATE, GND, VCC) should be short and wide, and avoid using vias. If vias must be used, two or more vias per layer transition is recommended.
- Keep the SOURCE of the upper FET as close as thermally possible to the DRAIN of the lower FET.
- Keep the connection in between the SOURCE of lower FET and power ground wide and short.
- Input capacitors should be placed as close to the DRAIN of the upper FET and the SOURCE of the lower FET as thermally possible.

Note: Refer to Intersil Tech Brief TB447 for more information.

Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal pad of the QFN and DFN parts to the power ground with multiple vias, or placing a low noise copper plane underneath the SOIC part is recommended. This heat spreading allows the part to achieve its full thermal potential.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
July 14, 2014	FN9115.7	Updated Phase voltage under "Absolute Maximum Ratings" on page 3 from "GND - 8V (<20ns Pulse Width, 10µJ)" to "GND - 10V (<20ns Pulse Width, 10µJ)" Updated "Package Outline Drawing" on page 13 (M8.15) to the latest revision. Updated Products verbiage to About Intersil verbiage on page 10.
January 17, 2012	FN9115.6	Added limits for "UGATE Turn-On Propagation Delay" and "LGATE Turn-On Propagation Delay" on page 4.
October 26, 2011	FN9115.5	Removed limits for "UGATE Turn-On Propagation Delay" and "LGATE Turn-On Propagation Delay" on page 4.
July 12, 2011	FN9115.4	Added "Revision History" on page 10 and "Products" on page 10. Added ISL6208BCRZ and ISL6208BIRZ parts to "Ordering Information" on page 2. Removed leaded, obsolete devices (ISL6208CB, ISL6208CR, ISL6208IB, ISL6208IR). Updated Tape & Reel note in "Ordering Information" on page 2 from "Add "-T" suffix for tape and reel." to new standard "Add "-T*" suffix for tape and reel." The "*" covers all possible tape and reel options Added MSL note to "Ordering Information" on page 2 Added Pinout for ISL6208BIRZ and ISL6208BCRZ on *page 2* Added "Thermal Information" on page 3 for new ISL6802B package, 8 Ld 2x2 DFN. Added Theta JC for SOIC package and Note 9. Removed "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." from common conditions of spec table. Added as Note in MIN MAX columns of "Electrical Specifications" table. Added standard text "Boldface limits apply over the operating temp range" to common conditions of spec table. Bolded applicable specs. Updated "Package Outline Drawing" on page 13 (M8.15) as follows: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern

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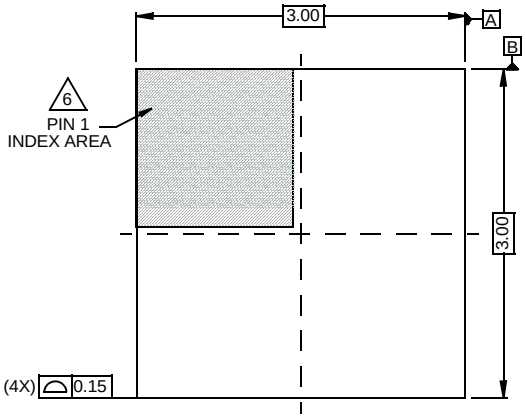
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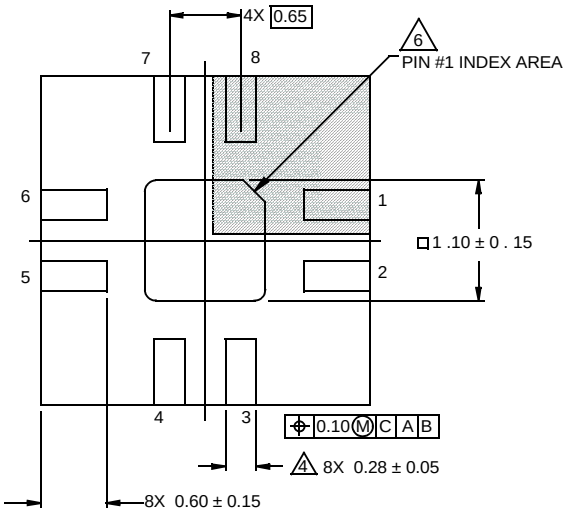
Package Outline Drawing

L8.3x3

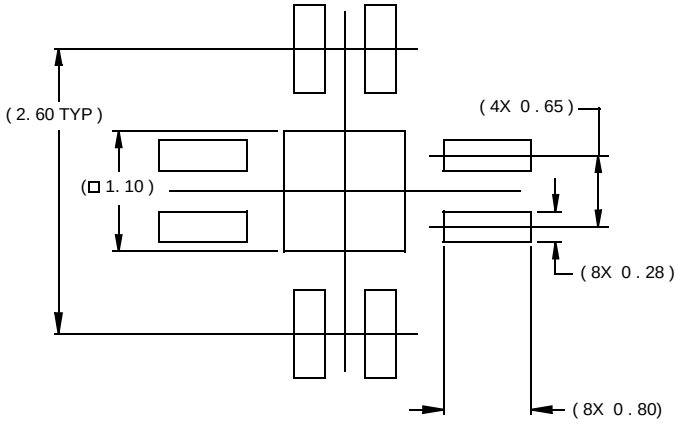
8 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 3/07



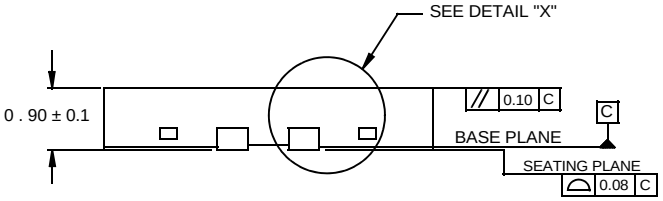
TOP VIEW



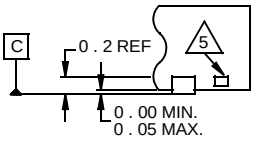
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

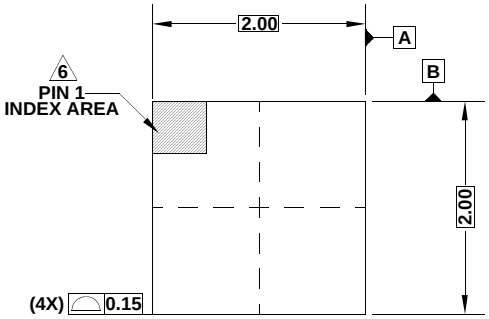
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Package Outline Drawing

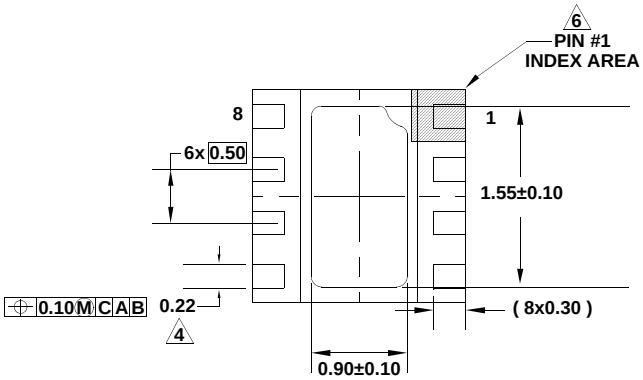
L8.2x2D

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (DFN) WITH EXPOSED PAD

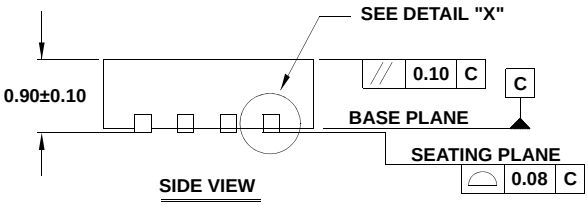
Rev 0, 3/11



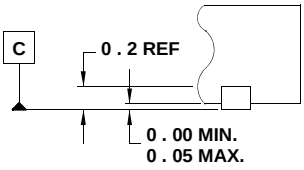
TOP VIEW



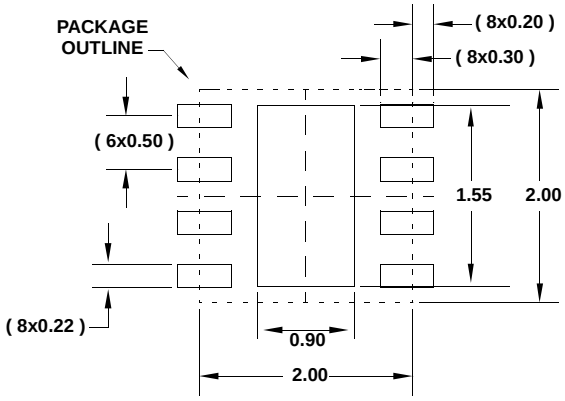
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

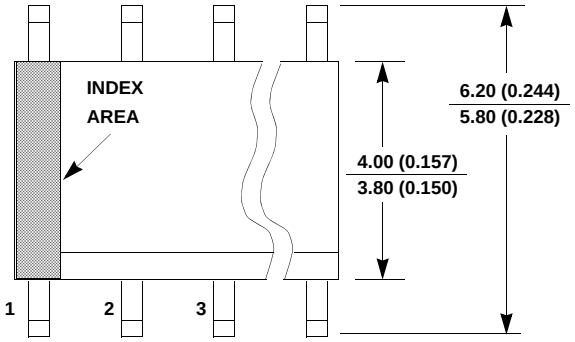
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

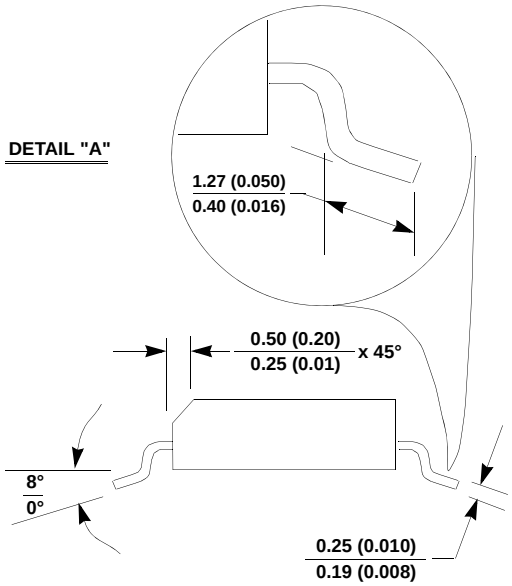
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

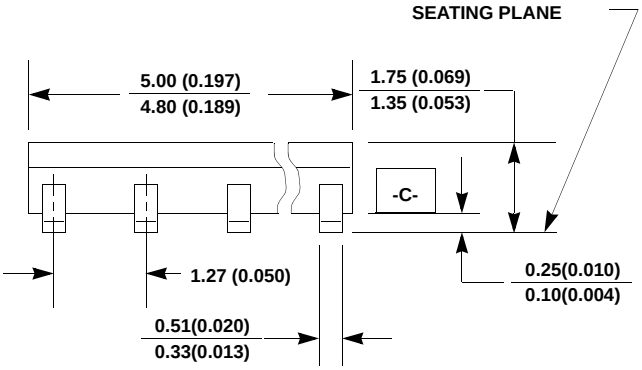
Rev 4, 1/12



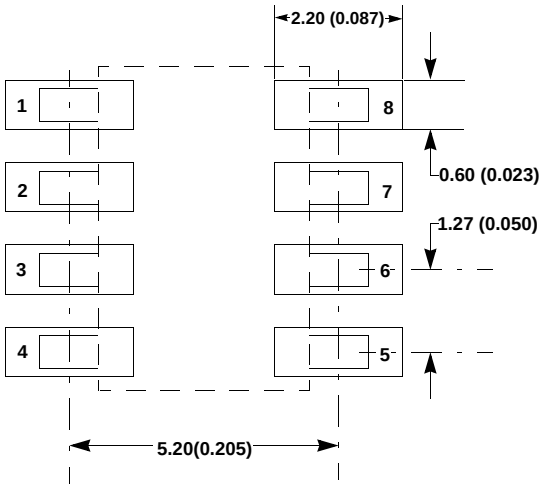
TOP VIEW



SIDE VIEW “B”



SIDE VIEW “A



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.