

1.5V Drive Pch+Pch MOSFET

QS8J1

●Structure

Silicon P-channel MOSFET

●Features

- 1) Low On-resistance.
- 2) Low voltage drive. (1.5 V)
- 3) High power package.

●Applications

Switching

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS8J1		○

●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit
Drain-source voltage	V_{DS}	-12	V
Gate-source voltage	V_{GS}	±10	V
Drain current	Continuous	I_D	±4.5
	Pulsed	I_{DP} *1	±18
Source current (Body diode)	Continuous	I_S	-1
	Pulsed	I_{SP} *1	-18
Total power dissipation	P_D *2	1.5	W / TOTAL
		1.25	W / ELEMENT
Channel temperature	T_{ch}	150	°C
Range of Storage temperature	T_{stg}	-55 to +150	°C

*1 $P_W \leq 10 \mu s$, Duty cycle $\leq 1\%$

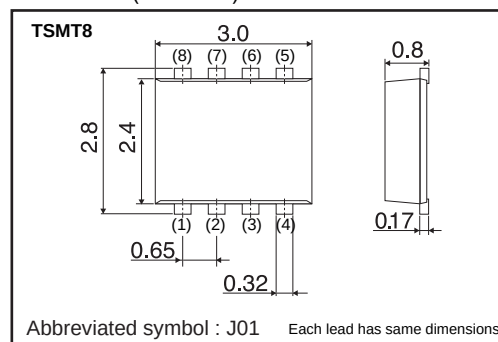
*2 Mounted on a ceramic board

●Thermal resistance

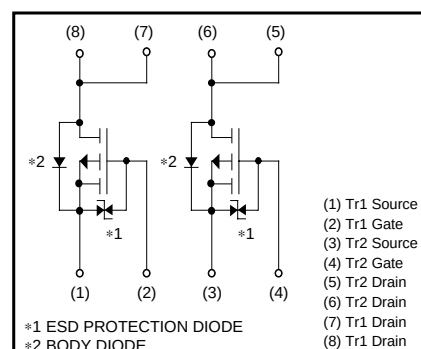
Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}$ *	83.3	°C/W / TOTAL
		100	°C/W / ELEMENT

* Mounted on a ceramic board.

●Dimensions (Unit : mm)



●Inner circuit



Transistors

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	±10	μA	$V_{GS}=±10V$, $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	−12	—	—	V	$I_D = -1mA$, $V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	−1	μA	$V_{DS} = -12V$, $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	−0.3	—	−1.0	V	$V_{DS} = -6V$, $I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	21	29	mΩ	$I_D = -4.5A$, $V_{GS} = -4.5V$
		—	27	38	mΩ	$I_D = -2.2A$, $V_{GS} = -2.5V$
		—	36	54	mΩ	$I_D = -2.2A$, $V_{GS} = -1.8V$
		—	49	98	mΩ	$I_D = -0.9A$, $V_{GS} = -1.5V$
Forward transfer admittance	$ Y_{fs} $ *	6.5	—	—	S	$V_{DS} = -6V$, $I_D = -4.5A$
Input capacitance	C_{iss}	—	2450	—	pF	$V_{DS} = -6V$
Output capacitance	C_{oss}	—	320	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	290	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	12	—	ns	$V_{DD} \rightleftharpoons -6V$
Rise time	t_r *	—	75	—	ns	$V_{GS} = -4.5V$ $I_D = -2.2A$
Turn-off delay time	$t_{d(off)}$ *	—	390	—	ns	$R_L \rightleftharpoons 2.7\Omega$
Fall time	t_f *	—	215	—	ns	$R_G=10\Omega$
Total gate charge	Q_g *	—	31	—	nC	$V_{DD} \rightleftharpoons -6V$ $V_{GS} = -4.5V$
Gate-source charge	Q_{gs} *	—	4.5	—	nC	$I_D = -4.5A$
Gate-drain charge	Q_{gd} *	—	4.0	—	nC	$R_L \rightleftharpoons 1.3\Omega$ / $R_G=10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	—	—	−1.2	V	$I_S = -4.5A$, $V_{GS}=0V$

* Pulsed

Transistors

●Electrical characteristic curves

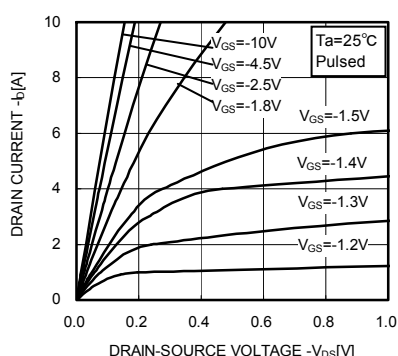


Fig.1 Typical Output Characteristics (I)

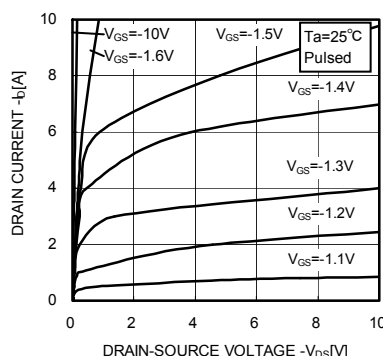


Fig.2 Typical Output Characteristics (II)

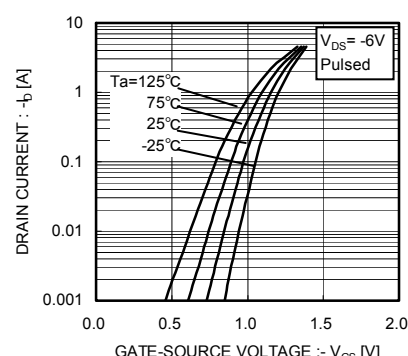


Fig.3 Typical Transfer Characteristics

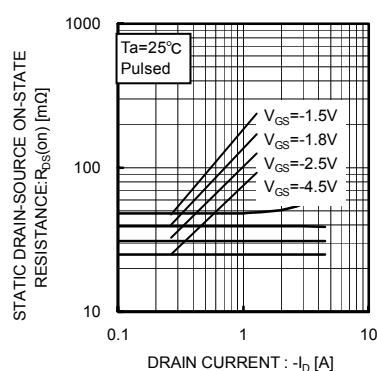


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

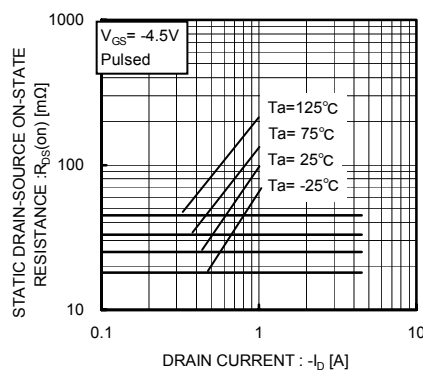


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

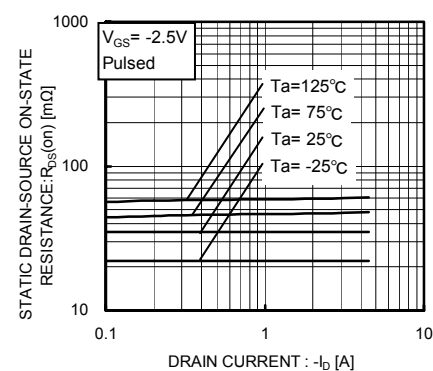


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)

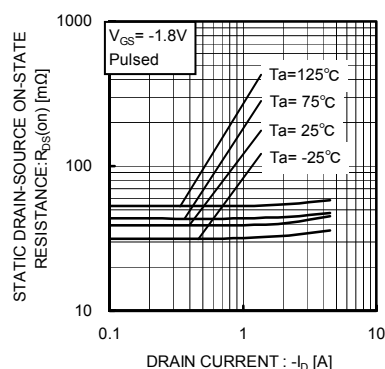


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)

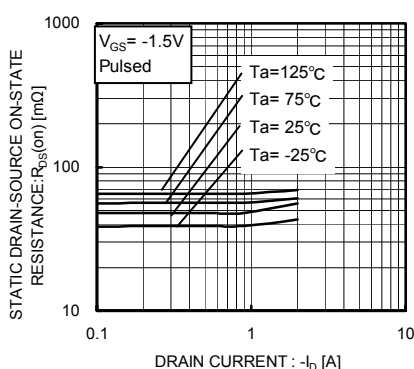


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (V)

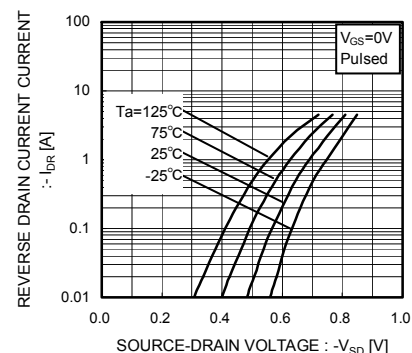


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

Transistors

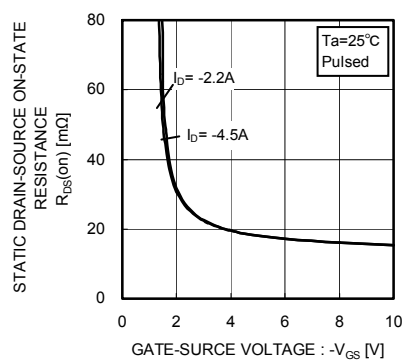


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

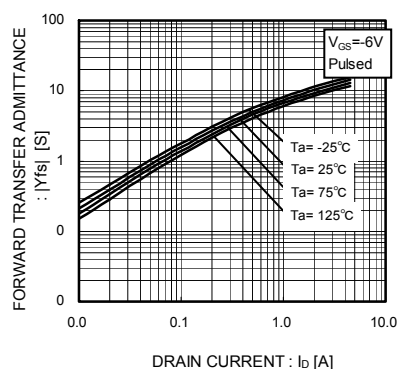


Fig.11 Forward Transfer Admittance vs. Drain Current

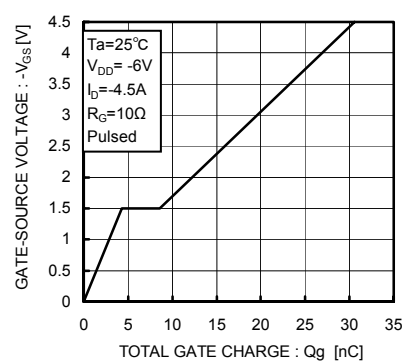


Fig.12 Dynamic Input Characteristics

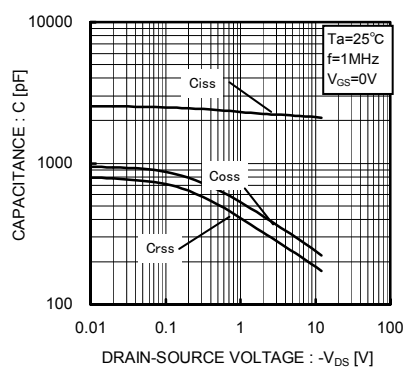


Fig.13 Typical Capacitance vs. Drain-Source Voltage

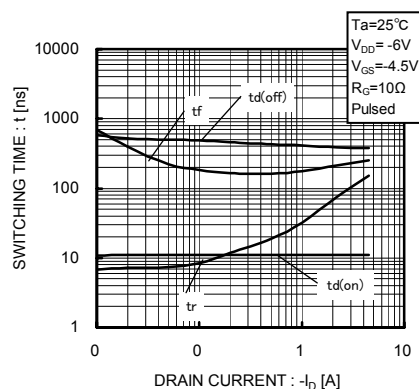


Fig.14 Switching Characteristics

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●Measurement circuits

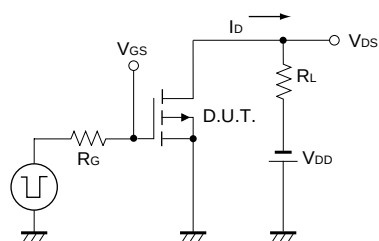


Fig.1-1 Switching Time Measurement Circuit

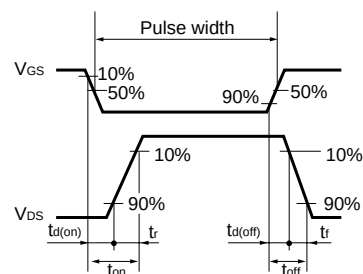


Fig.1-2 Switching Time Waveforms

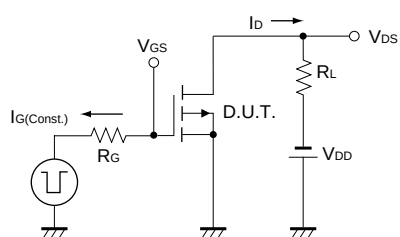


Fig.2-1 Gate Charge Measurement Circuit

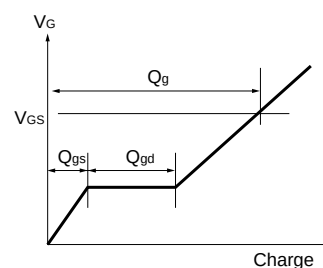


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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