3A, 2MHz, Synchronous Step-Down Converter

General Description

The RT8055 is a high efficiency synchronous, step-down DC/DC converter. Its input voltage range is from 2.6V to 5.5V and provides an adjustable regulated output voltage from 0.8V to 5V while delivering up to 3A of output current.

The internal synchronous low on-resistance power switches increase efficiency and eliminate the need for an external Schottky diode. The switching frequency is set by an external resistor. The 100% duty cycle provides low dropout operation extending battery life in portable systems. Current mode operation with external compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The RT8055 is operated in forced continuous PWM Mode which minimizes ripple voltage and reduces the noise and RF interference.

The RT8055 is available in the WDFN-10L 3x3 and SOP-8 (Exposed Pad) packages.

Ordering Information

RT8055□□

- Package Type
  - QW : WDFN-10L 3x3 (W-Type)
  - SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
  - Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

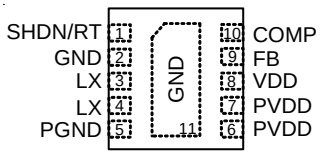
- **High Efficiency : Up to 95%**
- **Low $R_{DS(ON)}$ Internal Switches : 100mΩ**
- **Programmable Frequency : 300kHz to 2MHz**
- **No Schottky Diode Required**
- **0.8V Reference Voltage Allows for Low Output Voltage**
- **Forced Continuous Mode Operation**
- **100% Duty Cycle Operation**
- **Input Over Voltage Protection**
- **RoHS Compliant and Halogen Free**

Applications

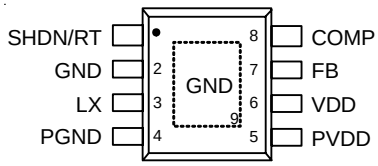
- Portable Instruments
- Battery-Powered Equipment
- Notebook Computers
- Distributed Power Systems
- IP Phones
- Digital Cameras
- 3G/3.5G Data Card

Pin Configurations

(TOP VIEW)



WDFN-10L 3x3

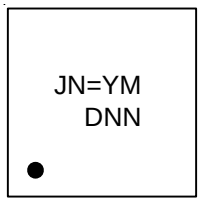


SOP-8 (Exposed Pad)

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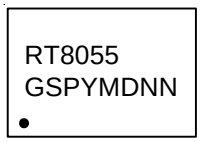
Marking Information

RT8055GQW



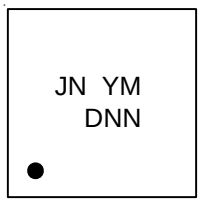
JN= : Product Code
YMDNN : Date Code

RT8055GSP



RT8055GSP : Product Number
YMDNN : Date Code

RT8055ZQW



JN : Product Code
YMDNN : Date Code

Typical Application Circuit

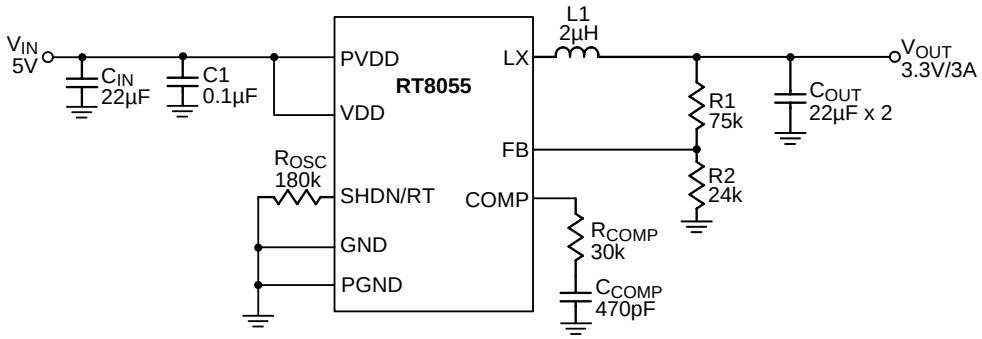


Table 1. Recommended Component Selection

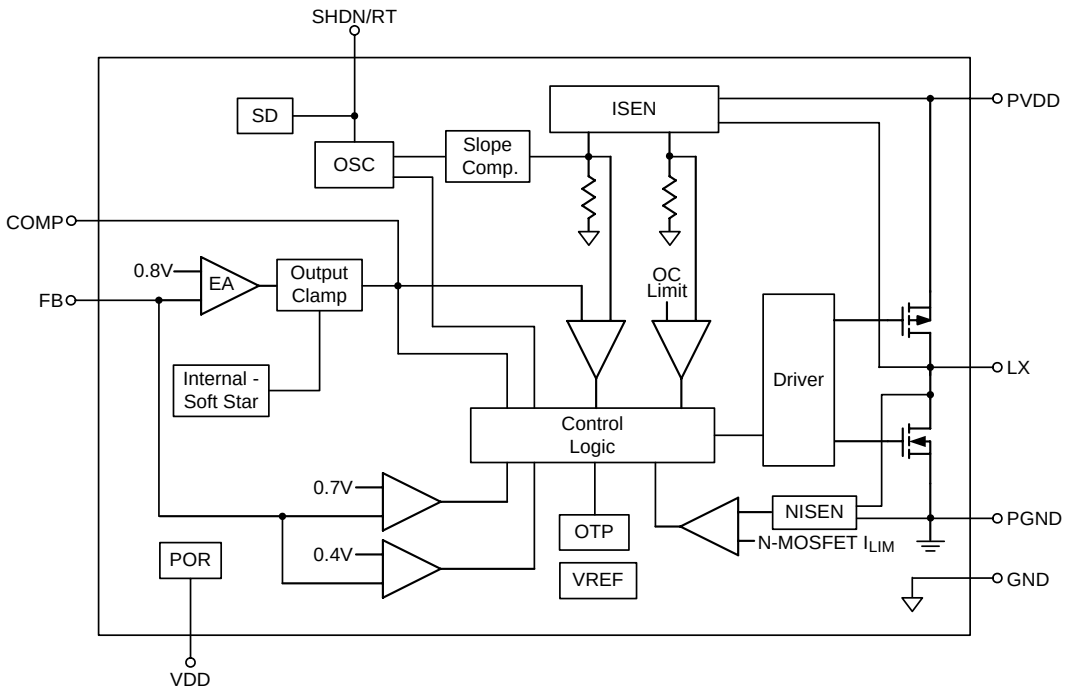
V_{OUT}	R1 (kΩ)	R2 (kΩ)	R_{COMP} (kΩ)	C_{COMP} (nF)	L1 (µH)	C_{OUT} (µF)
3.3	75	24	30	0.47	2.2	22 x 2
2.5	51	24	27	0.47	2.2	22 x 2
1.8	30	24	22	0.47	2.2	22 x 2
1.5	21	24	18	0.47	2.2	22 x 2
1.2	12	24	15	0.47	1.0	22 x 2
1.0	6	24	13	0.47	1.0	22 x 2

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Functional Pin Description

Pin No.		Pin Name	Pin Function
WDFN-10L 3x3	SOP-8		
1	1	SHDN/RT	Shutdown Control or Frequency Setting Input. Connect a resistor to ground from this pin sets the switching frequency. Force this pin to V_{DD} or GND causes the device to be shut down.
2, 11 (Exposed Pad)	2, 9 (Exposed Pad)	GND	Signal Ground. All small-signal components and compensation components should be connected to this ground, which in turn connects to PGND at one point. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3, 4	3	LX	Internal Power MOSFET Switches Output. Connect this pin to the inductor.
5	4	PGND	Power Ground. Connect this pin close to the negative terminal of C_{IN} and C_{OUT}.
6, 7	5	PVDD	Power Supply Input. Decouple this pin to PGND with a capacitor.
8	6	VDD	Signal Supply Input. Decouple this pin to GND with a capacitor. Generally, V_{DD} is equal to PVDD.
9	7	FB	Feedback Pin. This pin receives the feedback voltage from a resistive divider connected across the output.
10	8	COMP	Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Connect external compensation elements to this pin to stabilize the control loop.

Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD, PVDD ---------- –0.3V to 6.5V
- LX Pin Switch Voltage ---------- –0.3V to (PVDD + 0.3V)
  <10ns ---------- –5V to 8.5V
- Other I/O Pin Voltages ---------- –0.3V to 6.5V
- LX Pin Switch Current ---------- 4A
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10L 3x3 ---------- 1.667W
  SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 2)
  WDFN-10L 3x3, θ_{JA} ---------- 60°C/W
  WDFN-10L 3x3, θ_{JC} ---------- 7.8°C/W
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.6V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{DD}		2.6	--	5.5	V
Feedback Reference Voltage	V_{REF}		0.784	0.8	0.816	V
Feedback Leakage Current	I_{FB}	V_{FB} = 3.3V	--	--	0.1	μA
DC Bias Current		Active , V_{FB} = 0.7V, Not Switching	--	500	--	μA
		Shutdown	--	--	1	μA
Output Voltage Line Regulation	ΔV_{LINE}	V_{IN} = 2.6V to 5.5V	--	0.1	--	%/V
Output Voltage Load Regulation	ΔV_{LOAD}	V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A	--	0.4	--	%
Error Amplifier Transconductance	gm		--	400	--	μA/V
Current Sense Transresistance	R_S		--	0.4	--	Ω
RT Leakage Current		SHDN/RT = V_{IN} = 5.5V	--	--	1	μA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency		R_{OSC} = 180kΩ	1.44	1.8	2.16	MHz
		Adjustable Switching Frequency Range	0.3	--	2	
Switch On Resistance, High	$R_{DS(ON)_P}$	I_{SW} = 0.3A	--	100	160	mΩ
Switch On Resistance, Low	$R_{DS(ON)_N}$	I_{SW} = 0.3A	--	100	170	mΩ
Peak Current Limit	I_{LIM}		3.5	--	--	A
Under Voltage Lockout Threshold (Note 5)		V_{DD} Rising @Full Temperature	2.33	2.4	2.57	V
		V_{DD} Falling @Full Temperature	1.98	2.2	2.37	
Shutdown Threshold	V_{SHDN}	V_{SHDN} Rising	--	V_{IN} – 0.85	V_{IN} – 0.4	V

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

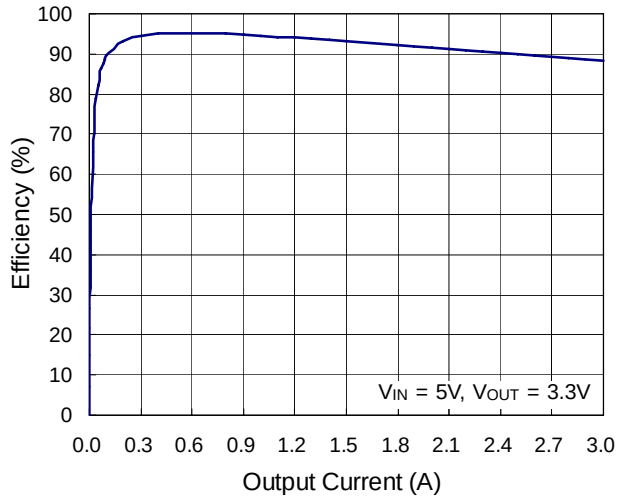
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

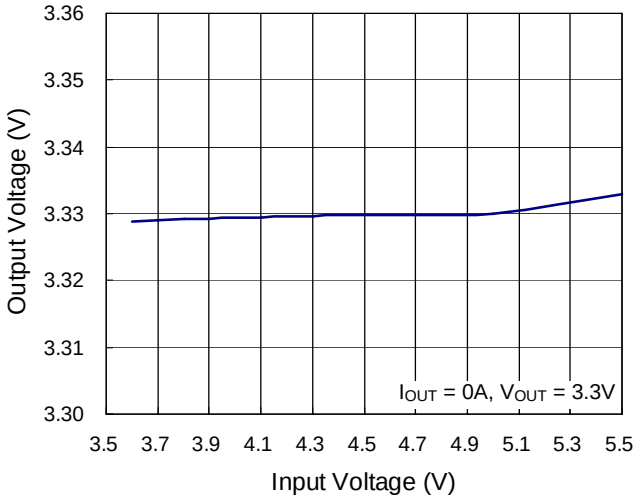
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Typical Operating Characteristics

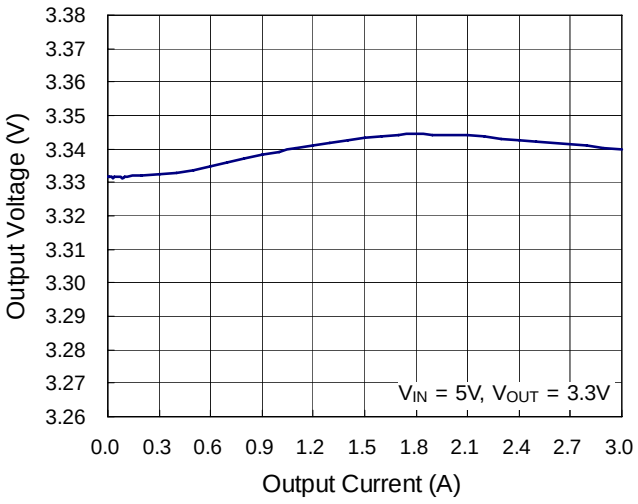
Efficiency vs. Output Current



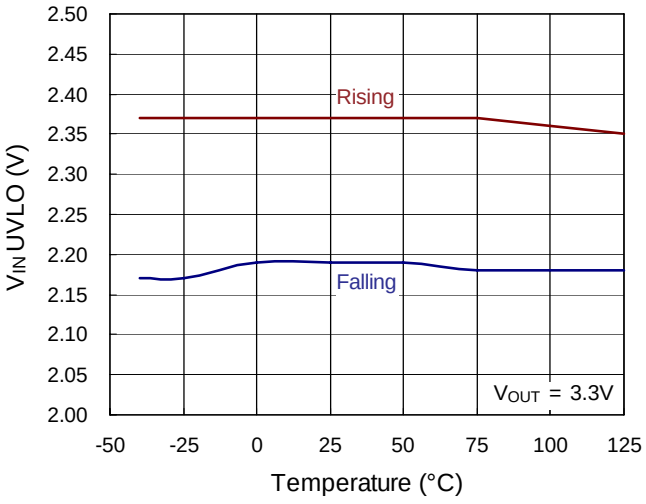
Output Voltage vs. Input Voltage



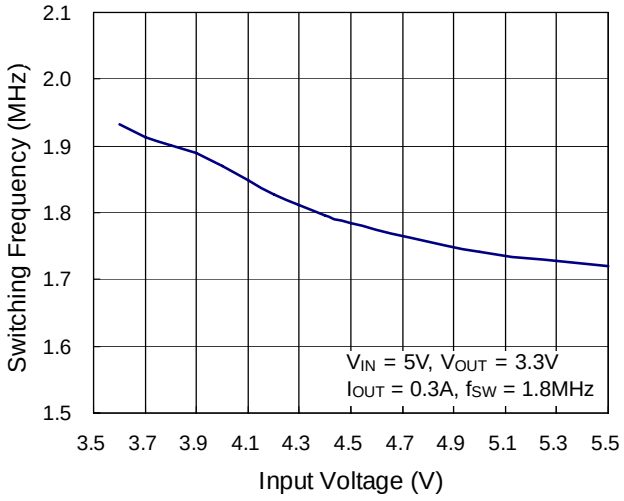
Output Voltage vs. Output Current



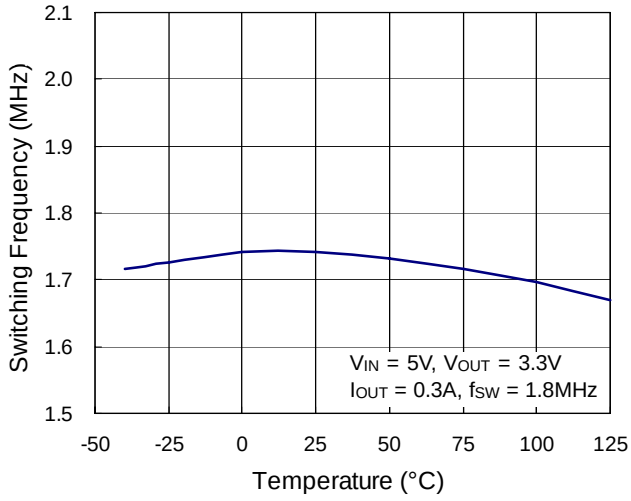
V_{IN} UVLO vs. Temperature



Switching Frequency vs. Input Voltage

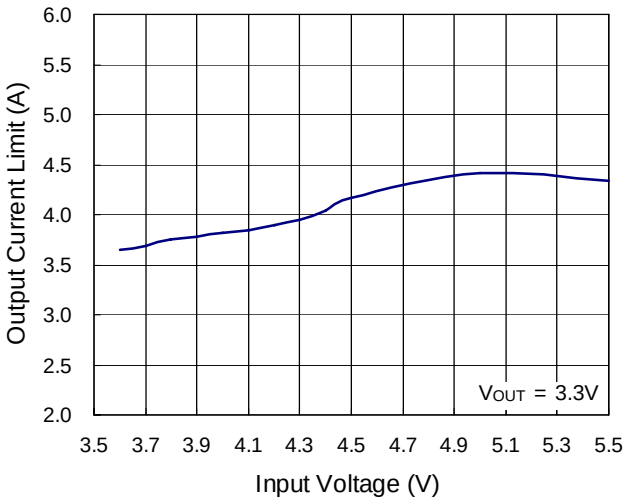


Switching Frequency vs. Temperature

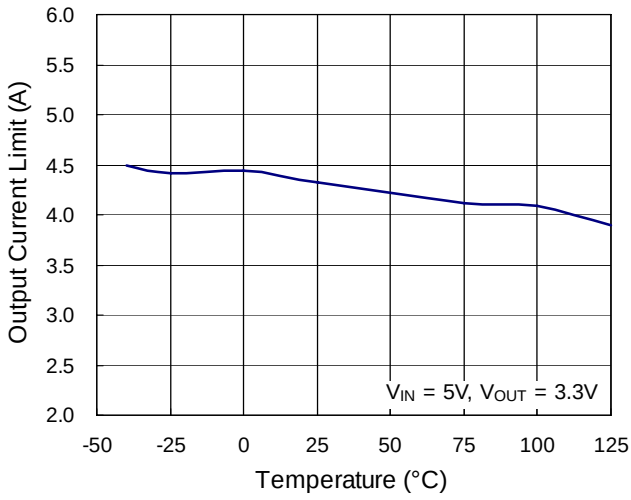


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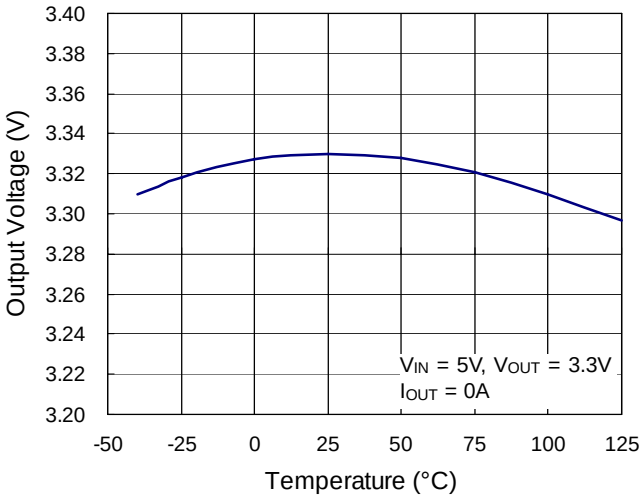
Output Current Limit vs. Input Voltage



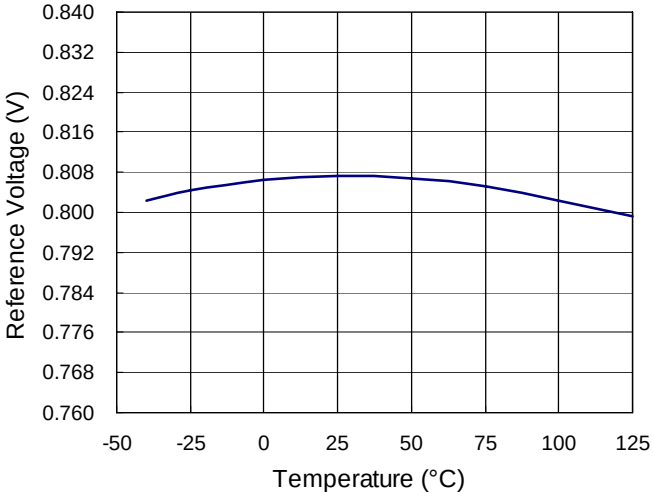
Output Current Limit vs. Temperature



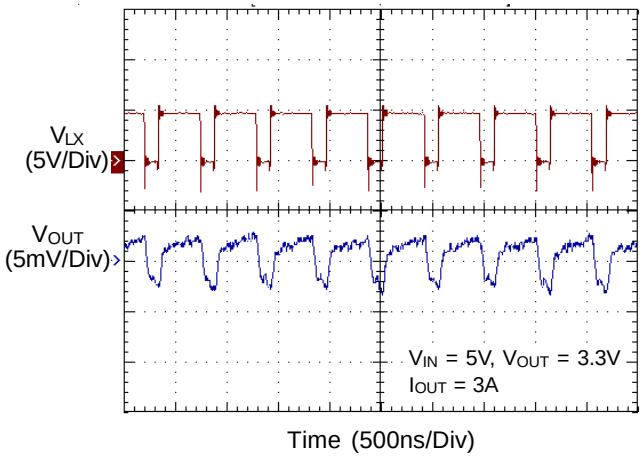
Output Voltage vs. Temperature



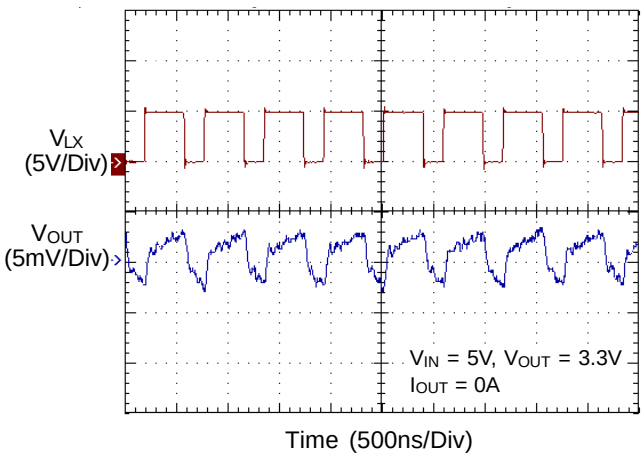
Reference Voltage vs. Temperature



Output Ripple

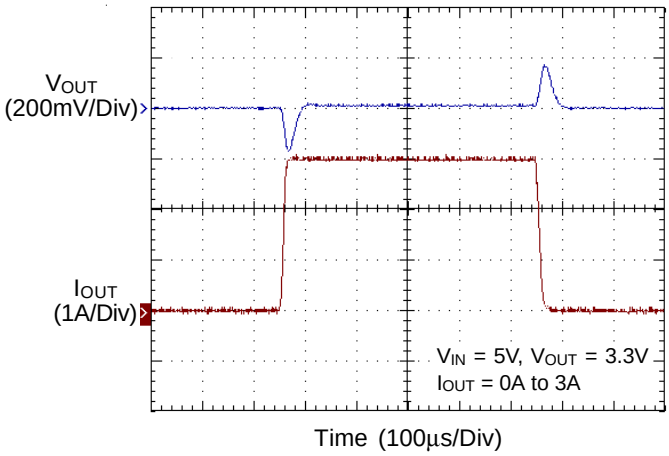


Output Ripple

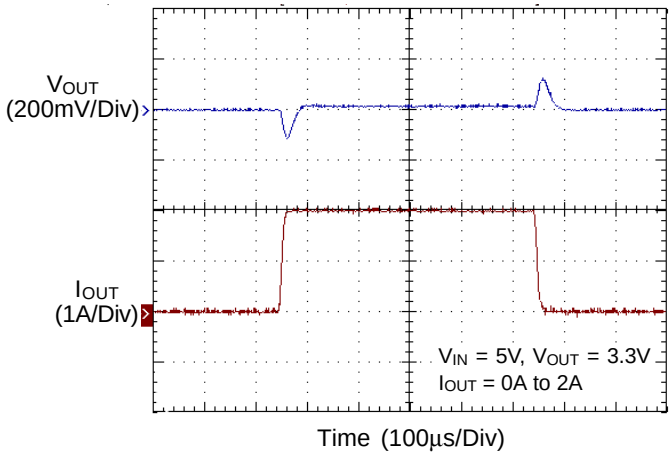


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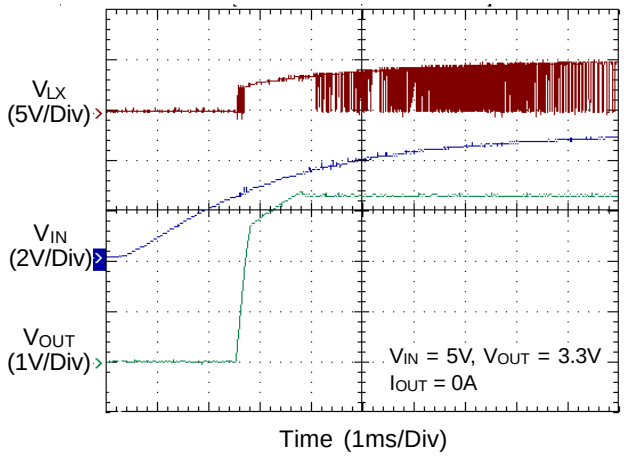
Load Transient Response



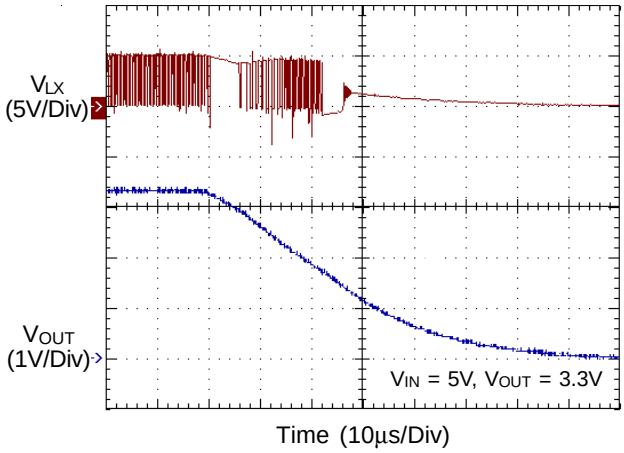
Load Transient Response



Power On from V_{IN}



UVP Shutdown



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Application Information

The basic RT8055 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} equals to 0.8V typical.

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

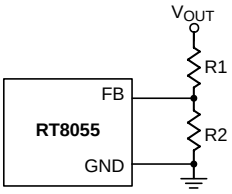


Figure 1. Setting the Output Voltage

Soft-Start

The RT8055 contains an internal soft-start clamp that gradually raises the clamp on the COMP pin.

Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The operating frequency of the RT8055 is determined by an external resistor that is connected between the SHDN/RT pin and GND. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator. The RT resistor value can be determined by examining the frequency vs. R_{RT} curve. Although frequencies as high as 2MHz are possible, the minimum on-time of the RT8055 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 110ns. Therefore, the minimum duty cycle is equal to 100 x 110ns x f (Hz).

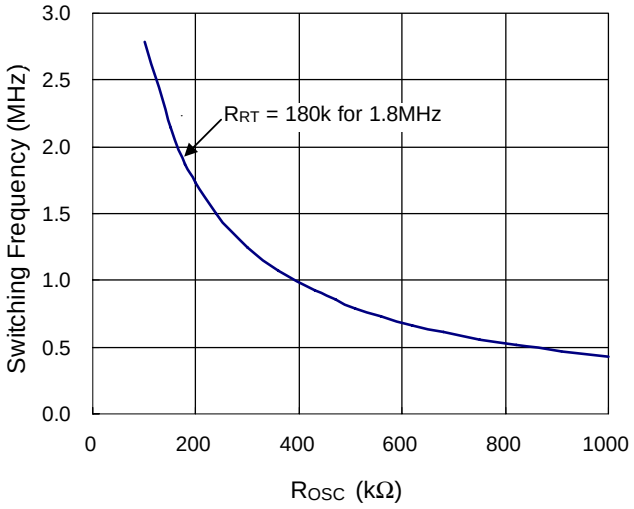


Figure 2

100% Duty Cycle Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle eventually reaching 100% duty cycle.

The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-MOSFET and the inductor.

Low Supply Operation

The RT8055 is designed to operate down to an input supply voltage of 2.6V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-Channel and N-Channel power switches increases. The user should calculate the power dissipation when the RT8055 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the RT8055, however, separated inductor current signals are used to monitor over current condition.

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This keeps the maximum output current relatively constant regardless of duty cycle.

Short Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. A current runaway detector is used to monitor inductor current. As current increasing beyond the control of current loop, switching cycles will be skipped to prevent current runaway from occurring.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.4(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input

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and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{DD}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) packages, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-10L 3x3 packages, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for SOP-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 3 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

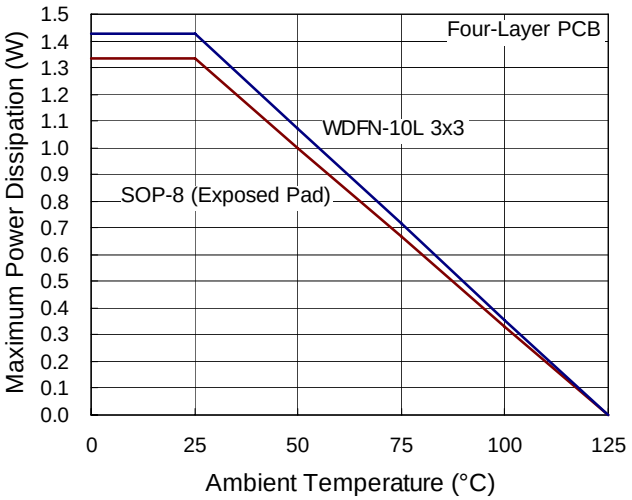


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8055.

- A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the GND pin at one point that is then connected to the PGND pin close to the IC. The exposed pad should be connected to GND.
- Connect the terminal of the input capacitor(s), C_{IN}, as close as possible to the PVDD pin. This capacitor provides the AC current into the internal power MOSFETs.
- LX node is with high frequency voltage swing and should be kept within small area. Keep all sensitive small-signal nodes away from the LX node to prevent stray capacitive noise pick-up.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of powercomponents.

  You can connect the copper areas to any DC net (PVDD, VDD, VOUT, PGND, GND, or any other DC rail in your system).
- Connect the FB pin directly to the feedback resistors. The resistor divider must be connected between V_{OUT} and GND.

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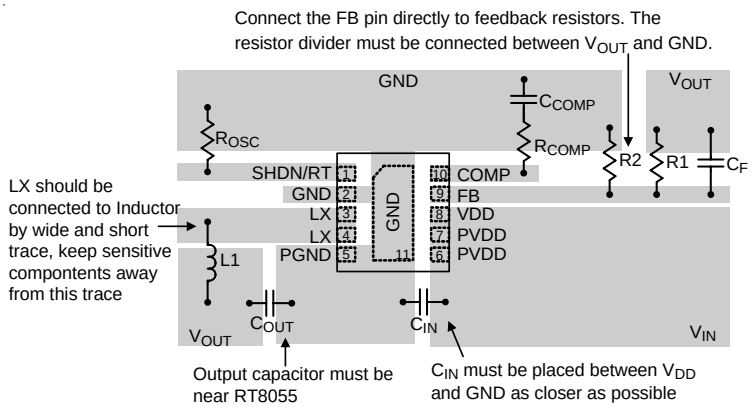


Figure 4. PCB Layout Guide

Recommended component selection for Typical Application

Table 2. Inductors

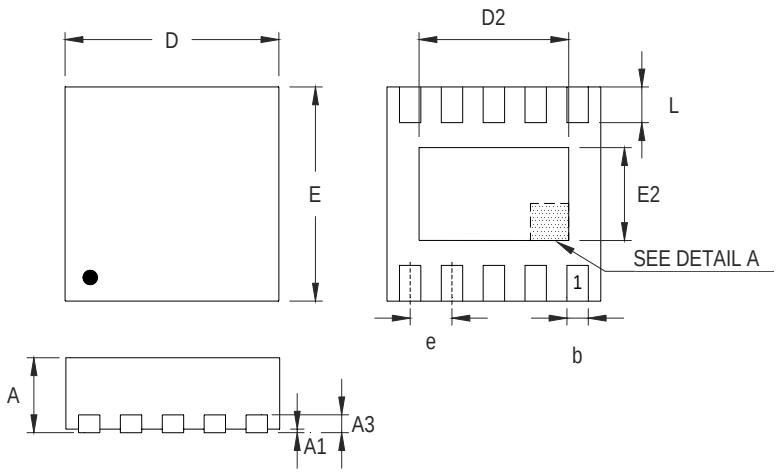
Component Supplier	Series	Inductance (μH)	DCR (mΩ)	Current Rating (mA)	Dimensions (mm)
TAIYO YUDEN	NR 8040	2	9	7800	8x8x4

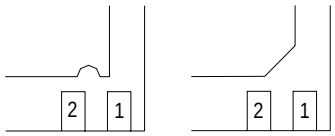
Table 3. Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (μF)	Case Size
TDK	C3225X5R0J226M	22	1210
TDK	C2012X5R0J106M	10	0805
Panasonic	ECJ4YB0J226M	22	1210
Panasonic	ECJ4YB1A106M	10	1210
TAIYO YUDEN	LMK325BJ226ML	22	1210
TAIYO YUDEN	JMK316BJ226ML	22	1206
TAIYO YUDEN	JMK212BJ106ML	10	0805

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Outline Dimension





DETAIL A

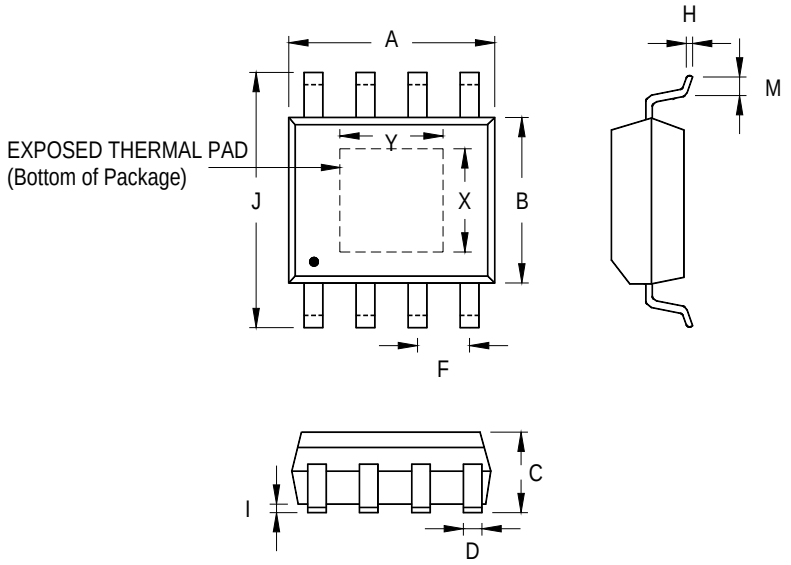
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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