RJK0389DPA

Silicon N Channel Power MOS FET with Schottky Barrier Diode
High Speed Power Switching

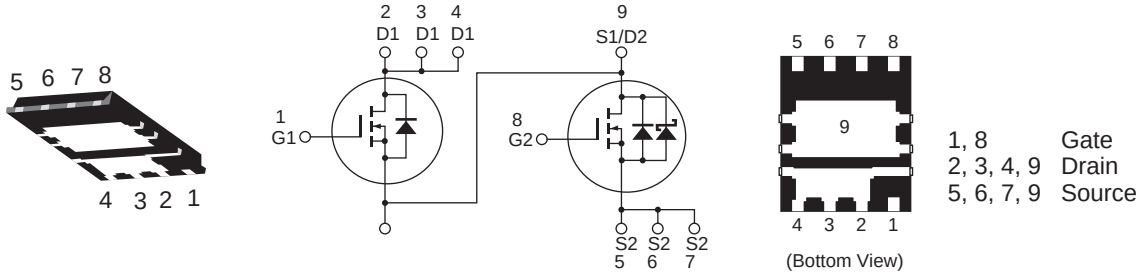
REJ03G1722-0410
Rev.4.10
May 13, 2010

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PWSN0008DD-A
(Package name: WPAK-D2)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		MOS1	MOS2	
Drain to source voltage	V_{DSS}	30	30	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	15	20	A
Drain peak current	$I_{D(pulse)}$ Note1	60	80	A
Reverse drain current	I_{DR}	15	20	A
Avalanche current	I_{AP} Note 2	8	11	A
Avalanche energy	E_{AR} Note 2	6.4	12.1	mJ
Channel dissipation	Pch Note3	10	10	W
Channel temperature	Tch	150	150	°C
Storage temperature	Tstg	–55 to +150	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C

Electrical Characteristics

• MOS1

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	8.2	10.7	mΩ	I_D = 7.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	11.8	16.5	mΩ	I_D = 7.5 A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	—	32	—	S	I_D = 7.5 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	860	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	165	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	53	—	pF	f = 1 MHz
Gate Resistance	Rg	—	4.2	—	Ω	
Total gate charge	Qg	—	6.3	—	nC	V_{DD} = 10 V
Gate to source charge	Qgs	—	2.3	—	nC	V_{GS} = 4.5 V
Gate to drain charge	Qgd	—	1.4	—	nC	I_D = 15 A
Turn-on delay time	$t_{d(on)}$	—	6.9	—	ns	V_{GS} = 10 V, I_D = 7.5 A
Rise time	t_r	—	4.1	—	ns	V_{DD} ≅ 10 V
Turn-off delay time	$t_{d(off)}$	—	40.8	—	ns	R_L = 1.33 Ω
Fall time	t_f	—	5.6	—	ns	R_g = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.84	1.10	V	I_F = 15 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	20	—	ns	I_F =15 A, V_{GS} = 0 di_F/ dt = 100 A/μs

Notes: 4. Pulse test

• MOS2

(Ta = 25°C)

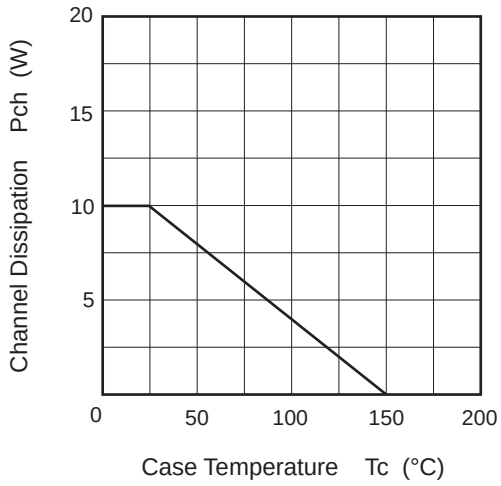
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	mA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	V_{DS} = 10 V, I_D =1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	6.8	8.9	mΩ	I_D = 10 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	10.5	14.7	mΩ	I_D = 10 A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	—	38	—	S	I_D = 10 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	1000	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	240	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	100	—	pF	f = 1 MHz
Gate Resistance	Rg	—	4.5	—	Ω	
Total gate charge	Qg	—	7.2	—	nC	V_{DD} = 10 V
Gate to source charge	Qgs	—	2.9	—	nC	V_{GS} = 4.5 V
Gate to drain charge	Qgd	—	2.2	—	nC	I_D = 20 A
Turn-on delay time	$t_{d(on)}$	—	8.5	—	ns	V_{GS} = 10 V, I_D = 10 A
Rise time	t_r	—	4.0	—	ns	V_{DD} ≅ 10 V
Turn-off delay time	$t_{d(off)}$	—	39	—	ns	R_L = 1.0 Ω
Fall time	t_f	—	6.6	—	ns	R_g = 4.7 Ω
Schottky Barrier diode forward voltage	V_F	—	0.44	—	V	I_F = 2 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	12	—	ns	I_F = 20 A, V_{GS} = 0 di_F/ dt = 100 A/μs

Notes: 4. Pulse test

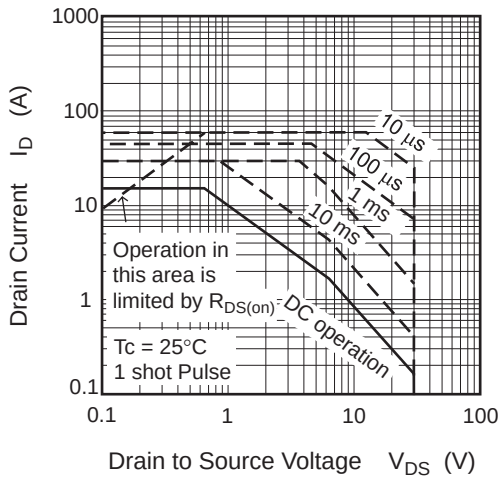
Main Characteristics

• MOS1

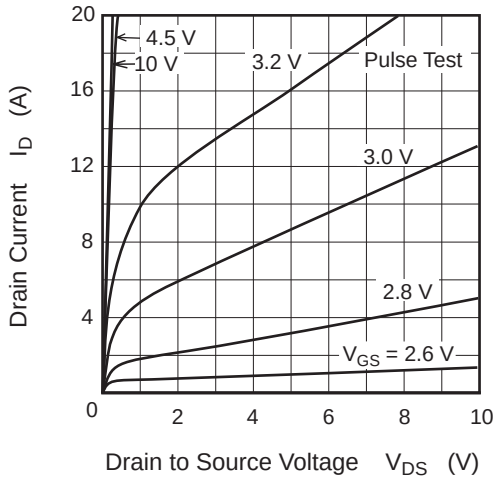
Power vs. Temperature Derating



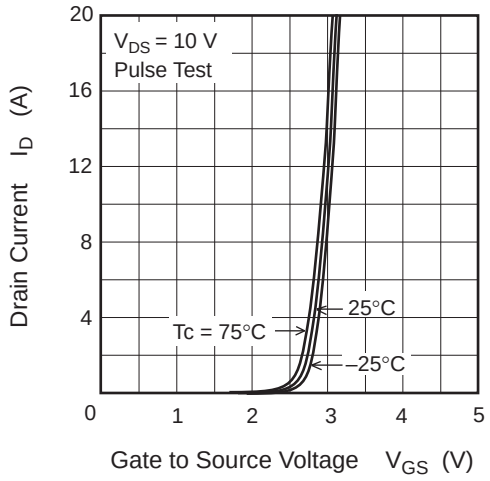
Maximum Safe Operation Area



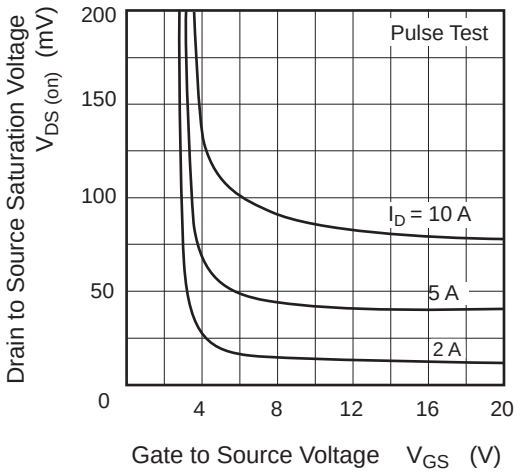
Typical Output Characteristics



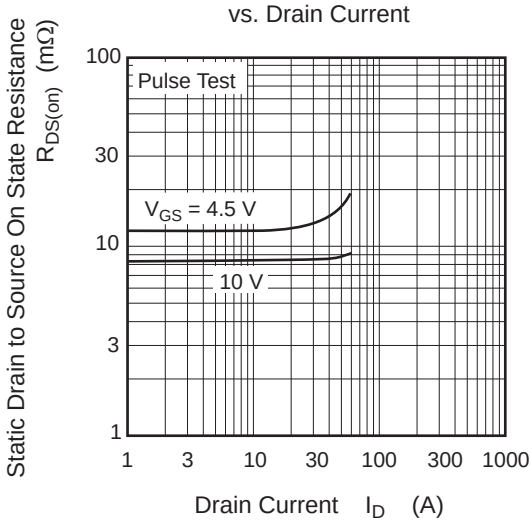
Typical Transfer Characteristics



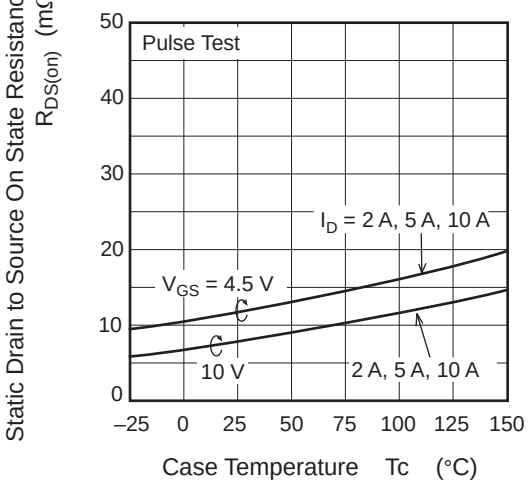
Drain to Source Saturation Voltage vs. Gate to Source Voltage



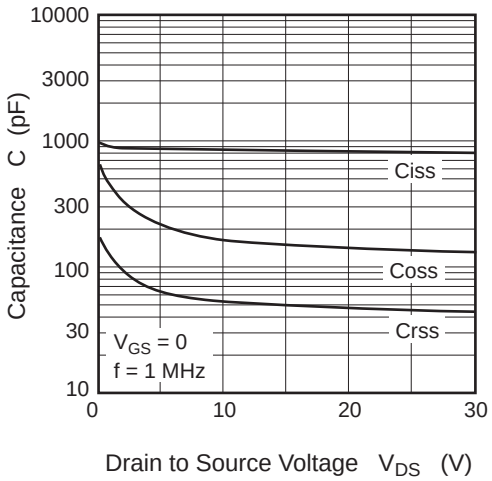
Static Drain to Source On State Resistance vs. Drain Current



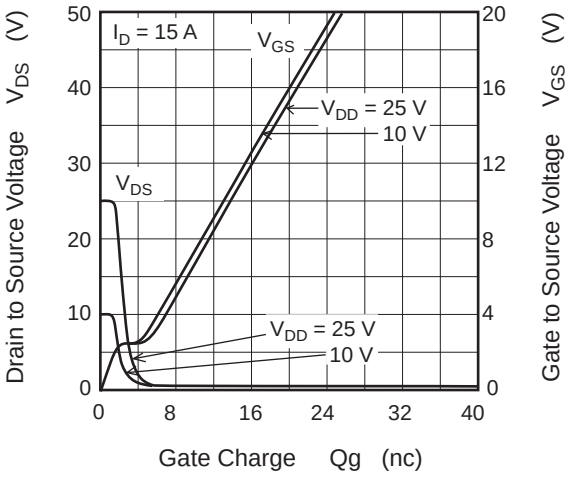
Static Drain to Source On State Resistance vs. Temperature



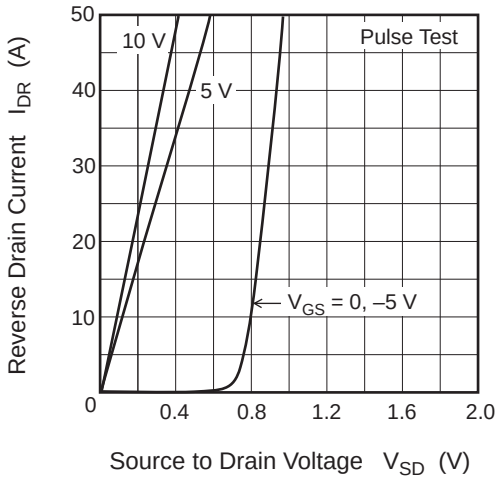
Typical Capacitance vs. Drain to Source Voltage



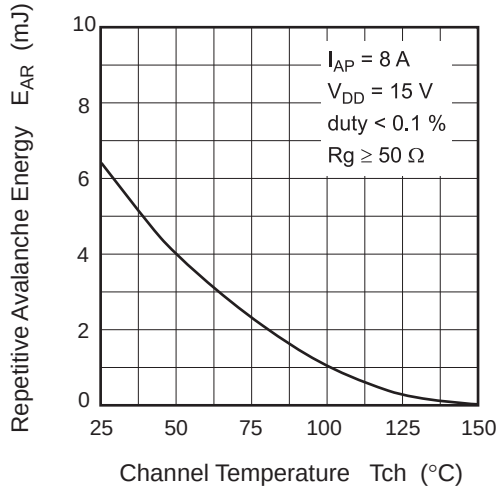
Dynamic Input Characteristics



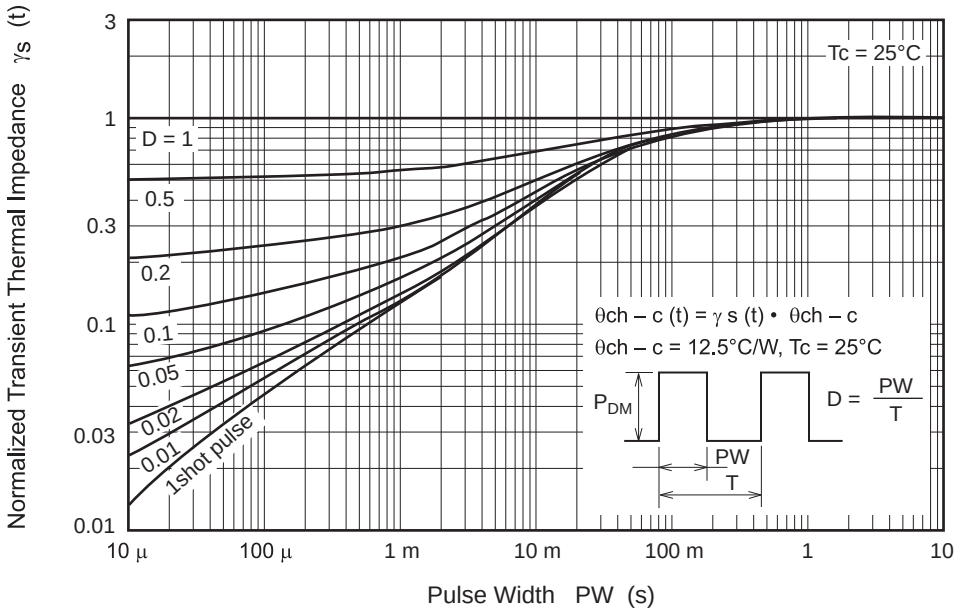
Reverse Drain Current vs. Source to Drain Voltage



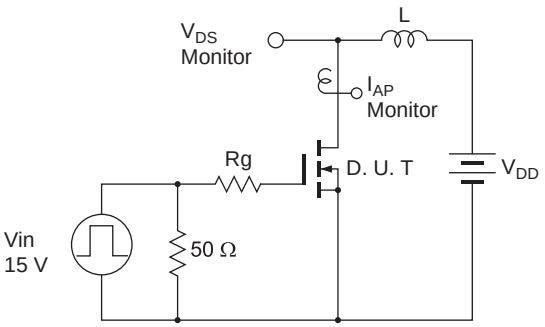
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

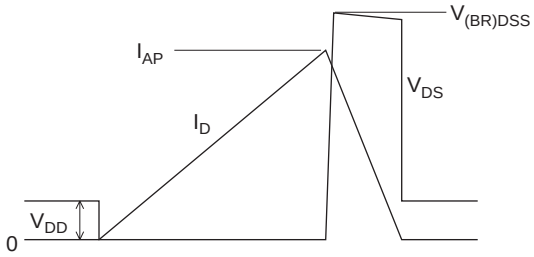


Avalanche Test Circuit

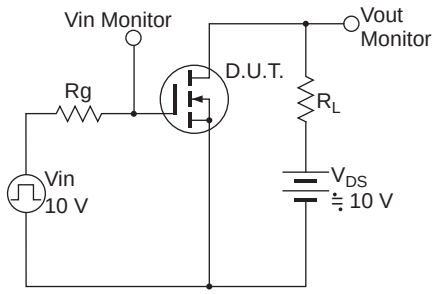


Avalanche Waveform

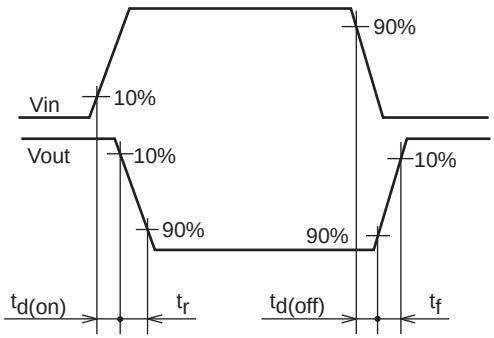
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

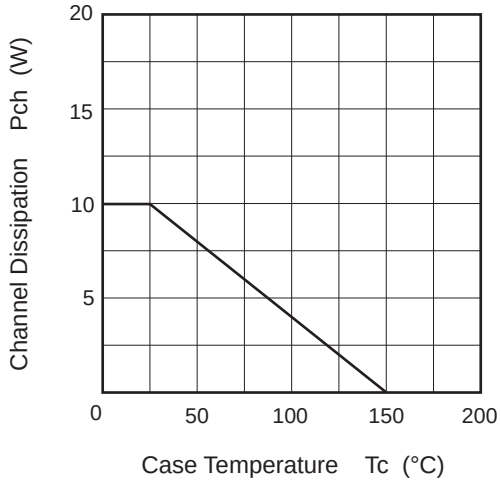


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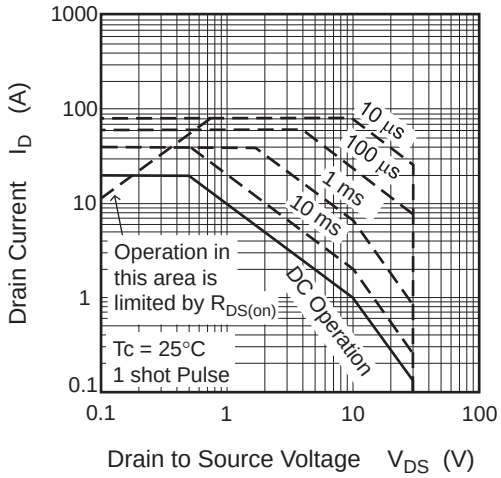


• MOS2 and Schottky Barrier Diode

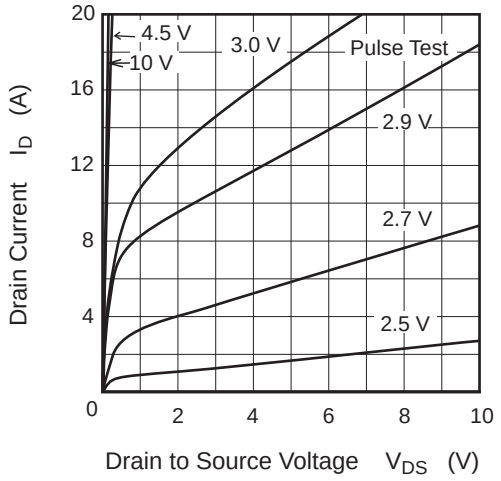
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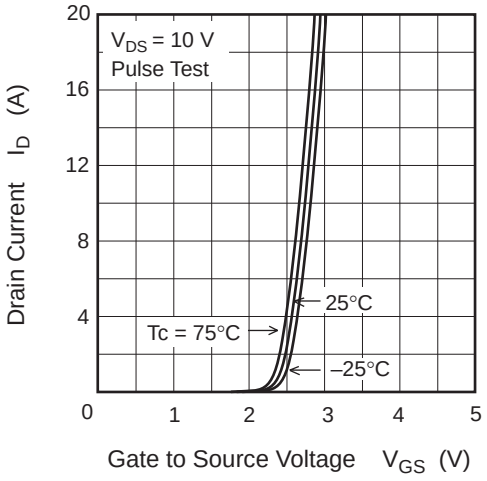
Maximum Safe Operation Area



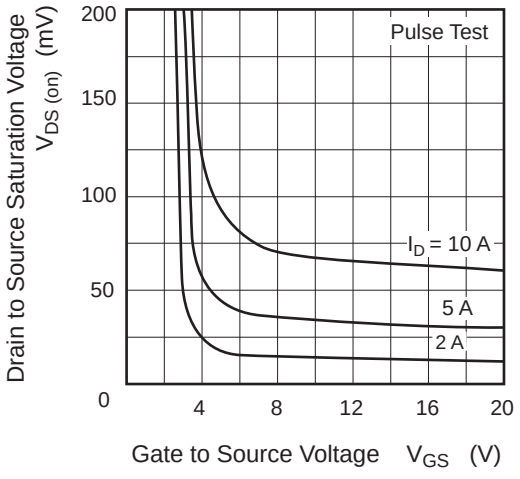
Typical Output Characteristics



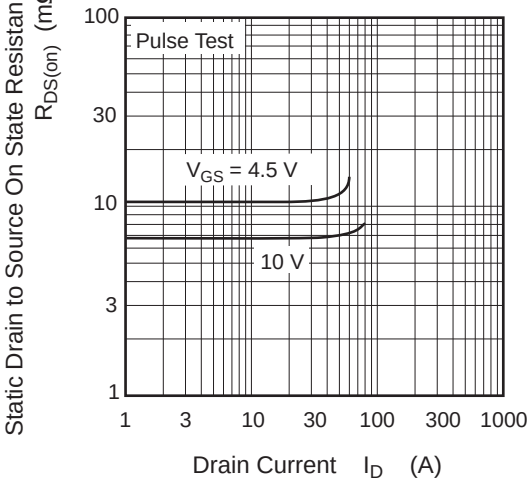
Typical Transfer Characteristics



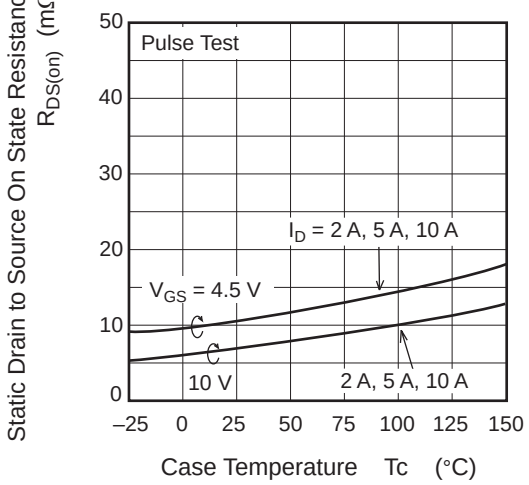
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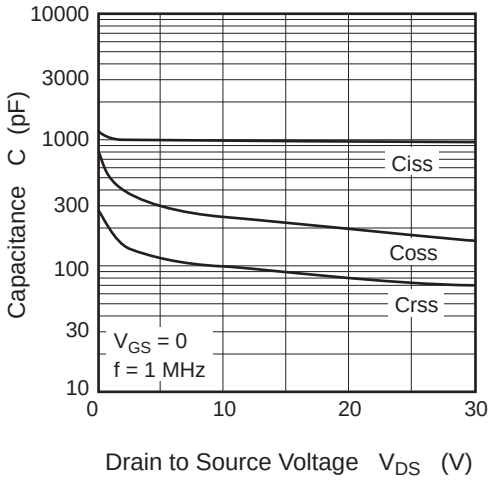
Static Drain to Source On State Resistance vs. Drain Current



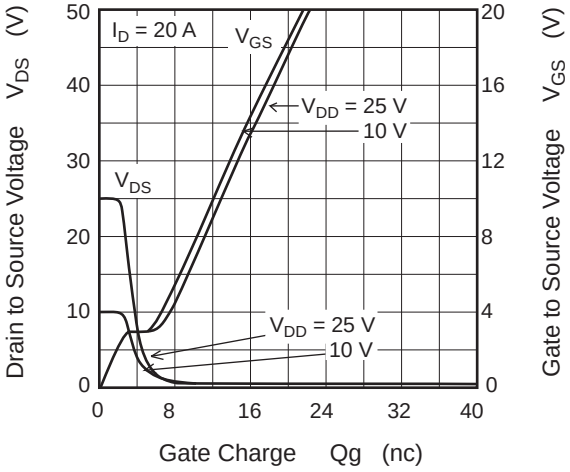
Static Drain to Source On State Resistance vs. Temperature



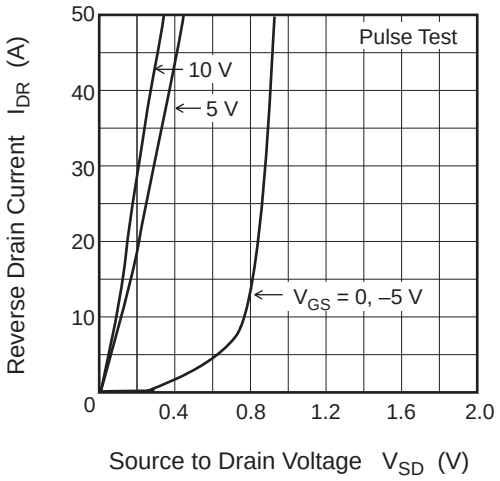
Typical Capacitance vs. Drain to Source Voltage



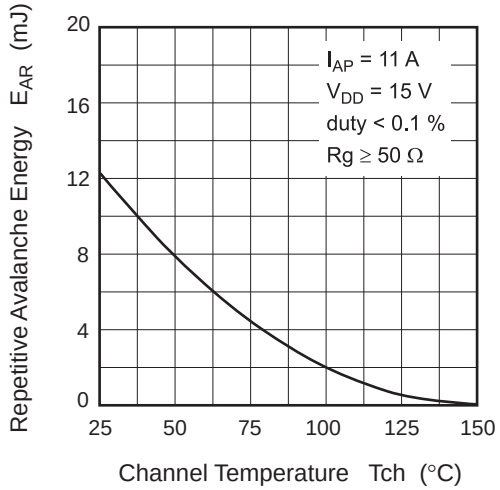
Dynamic Input Characteristics



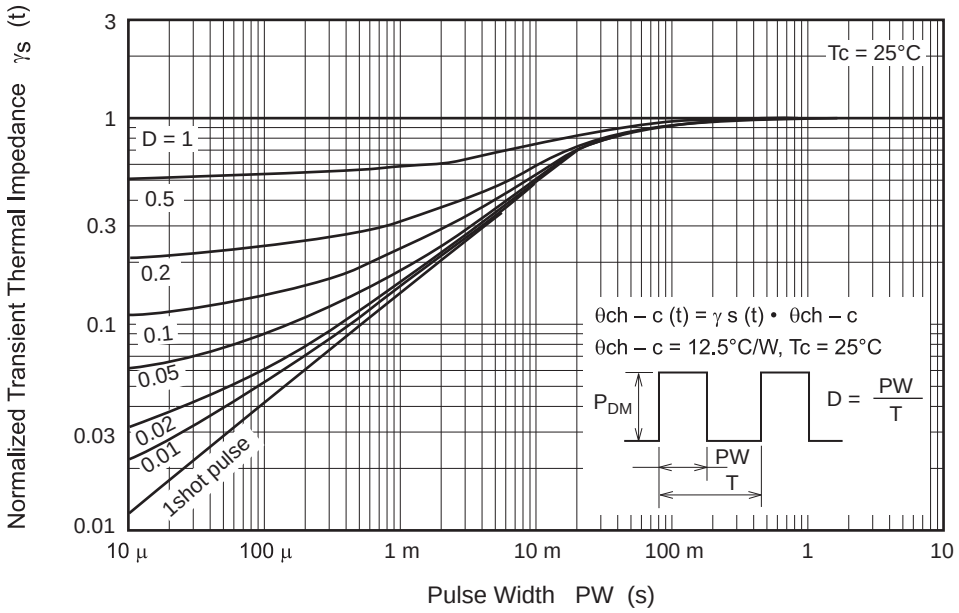
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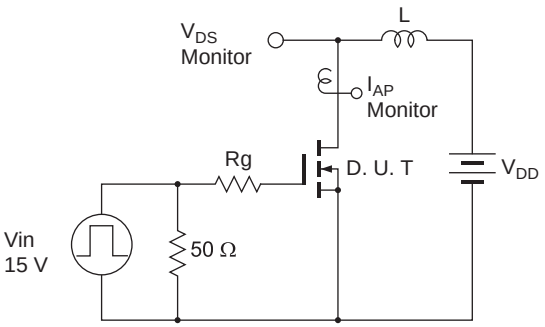
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

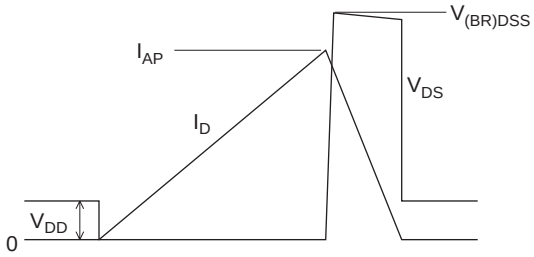


Avalanche Test Circuit

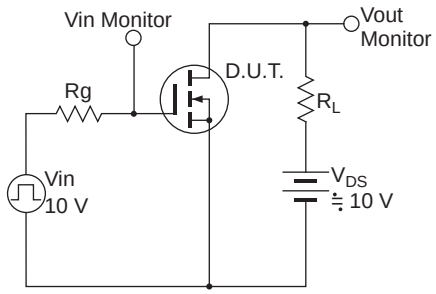


Avalanche Waveform

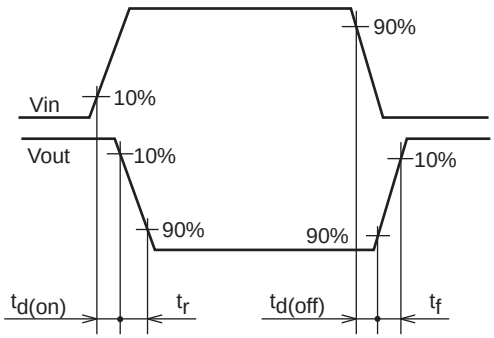
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



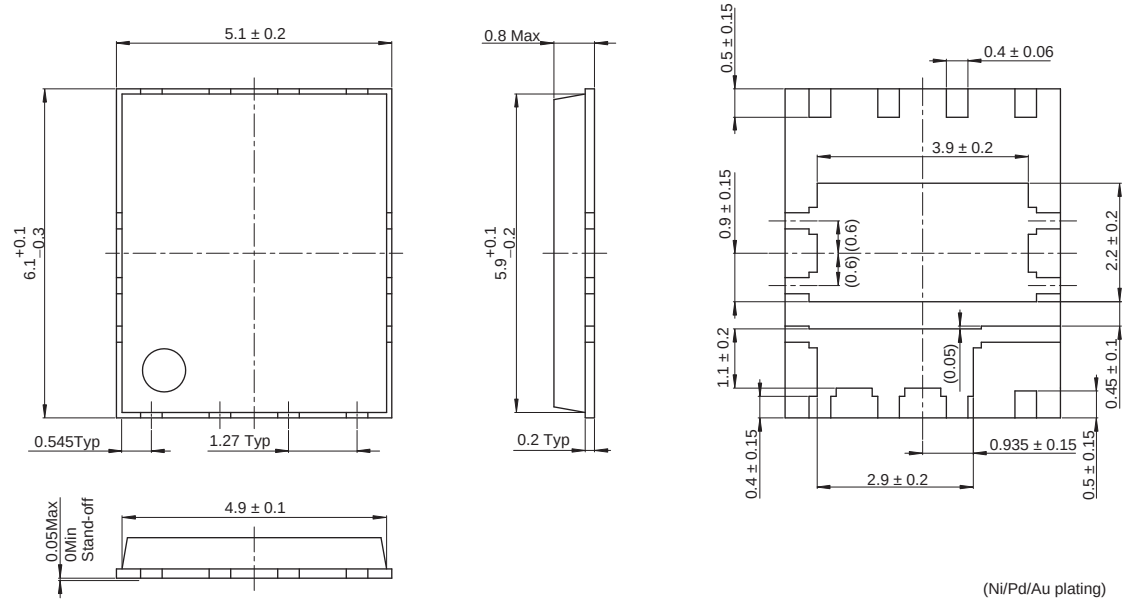
Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
WPAK-D(2)	—	PWSN0008DD-A	WPAK-D(2)V	0.07g

Unit : mm



Ordering Information

Part No.	Quantity	Shipping Container
RJK0389DPA-00-J53	3000 pcs	Taping

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