DATA SHEET

BST80
N-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of April 1995
File under Discrete Semiconductors, SC13b

1997 Jun 20

Philips Semiconductors

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N-channel enhancement mode vertical D-MOS transistor

BST80

FEATURES

- Low drain-source on-state resistance
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

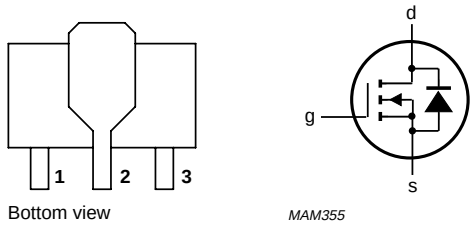
- Thin and thick film circuits
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT89 package.

PINNING - SOT89

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate



Marking code: KM

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	80	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1	W
R_{DSon}	drain-source on-state resistance	I_D = 500 mA; V_{GS} = 10 V	2	3	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	I_D = 500 mA; V_{DS} = 15 V	300	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	80	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	500	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a ceramic substrate; area 2.5 cm^2; thickness 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	80	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0	–	–	1	μA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 500 mA	–	2	3	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	I_D = 500 mA; V_{DS} = 15 V	–	300	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	45	60	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	30	45	pF
C_{rss}	reverse transfer capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	8	12	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 500 mA	–	–	10	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 50 V; I_D = 500 mA	–	–	15	ns

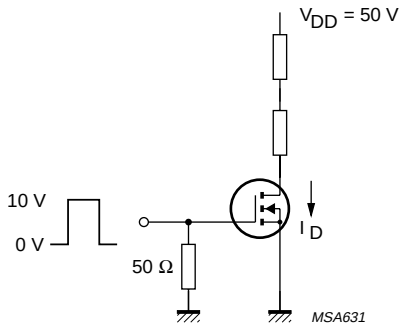


Fig.2 Switching times test circuit.

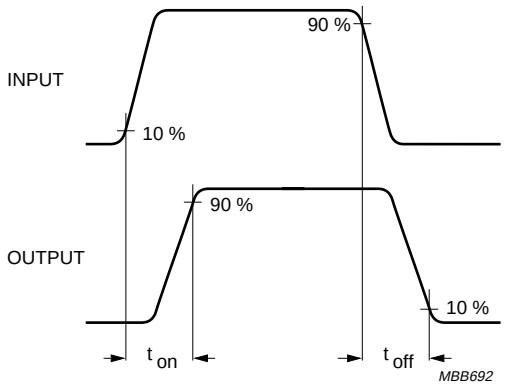


Fig.3 Input and output waveforms.

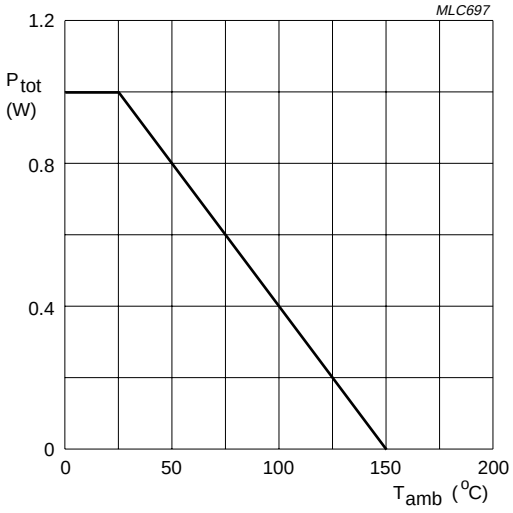
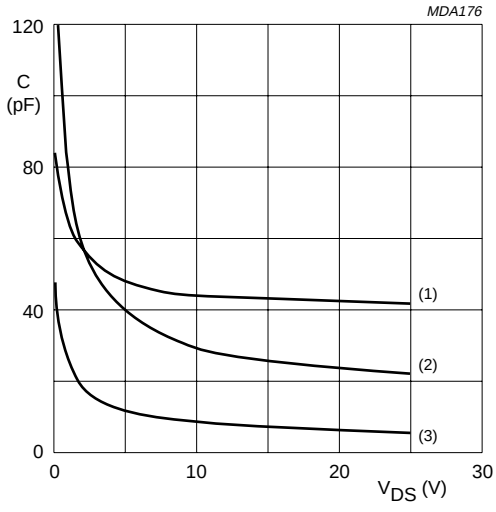


Fig.4 Power derating curve.



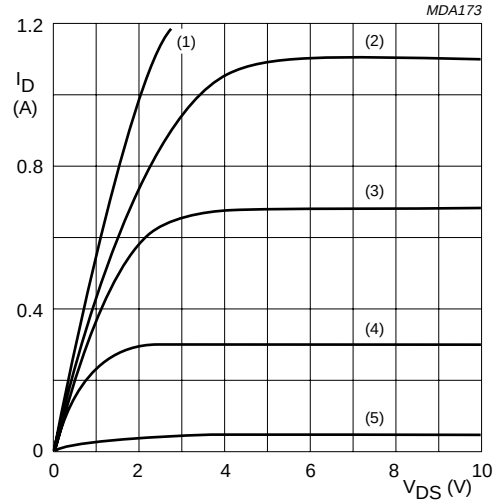
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

(1) C_{iss}.

(2) C_{oss}.

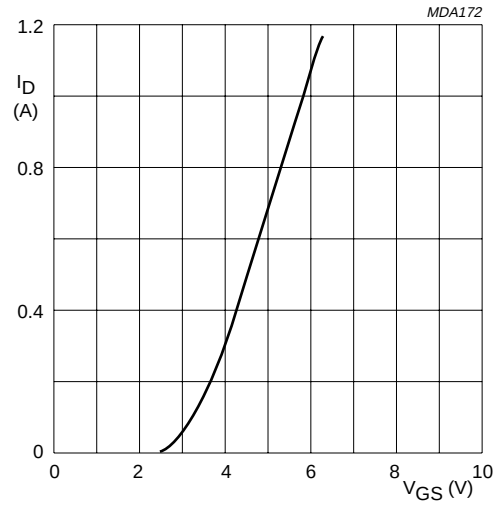
(3) C_{rss}.

Fig.5 Capacitance as a function of drain-source voltage; typical values.



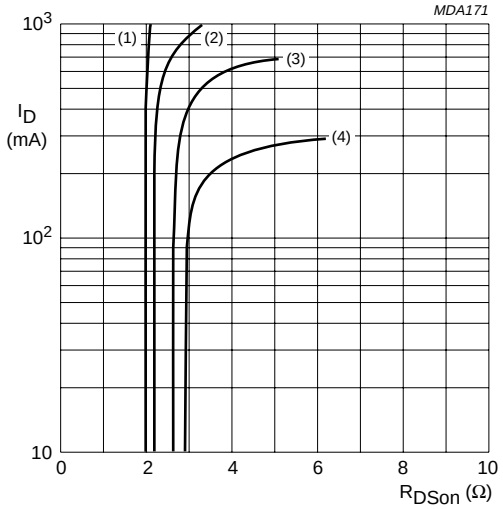
T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 6 V.
(3) V_{GS} = 5 V.
(4) V_{GS} = 4 V.
(5) V_{GS} = 3 V.

Fig.6 Output characteristics; typical values.



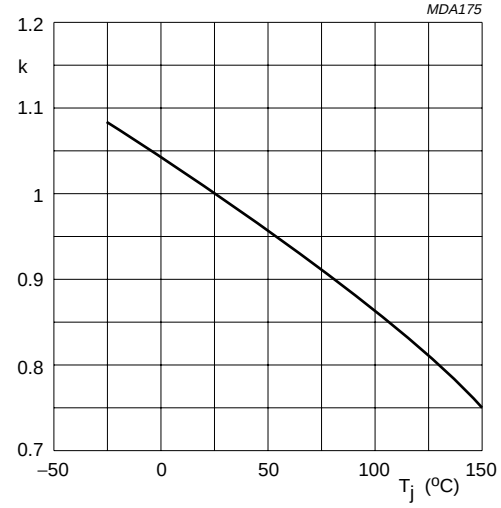
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Transfer characteristic; typical values.



T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 6 V.
(3) V_{GS} = 5 V.
(4) V_{GS} = 4 V.

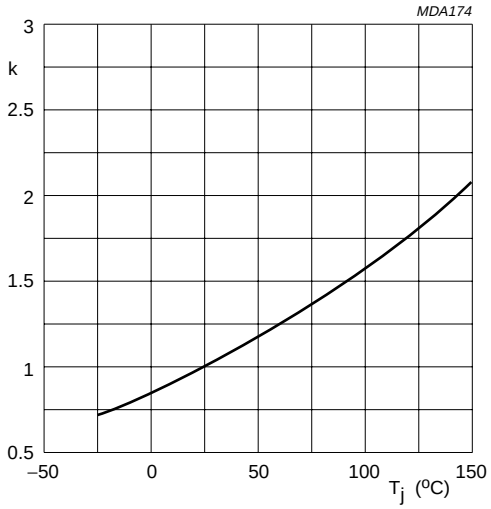
Fig.8 Drain current as a function of drain-source on-state resistance; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at 1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage; typical values.



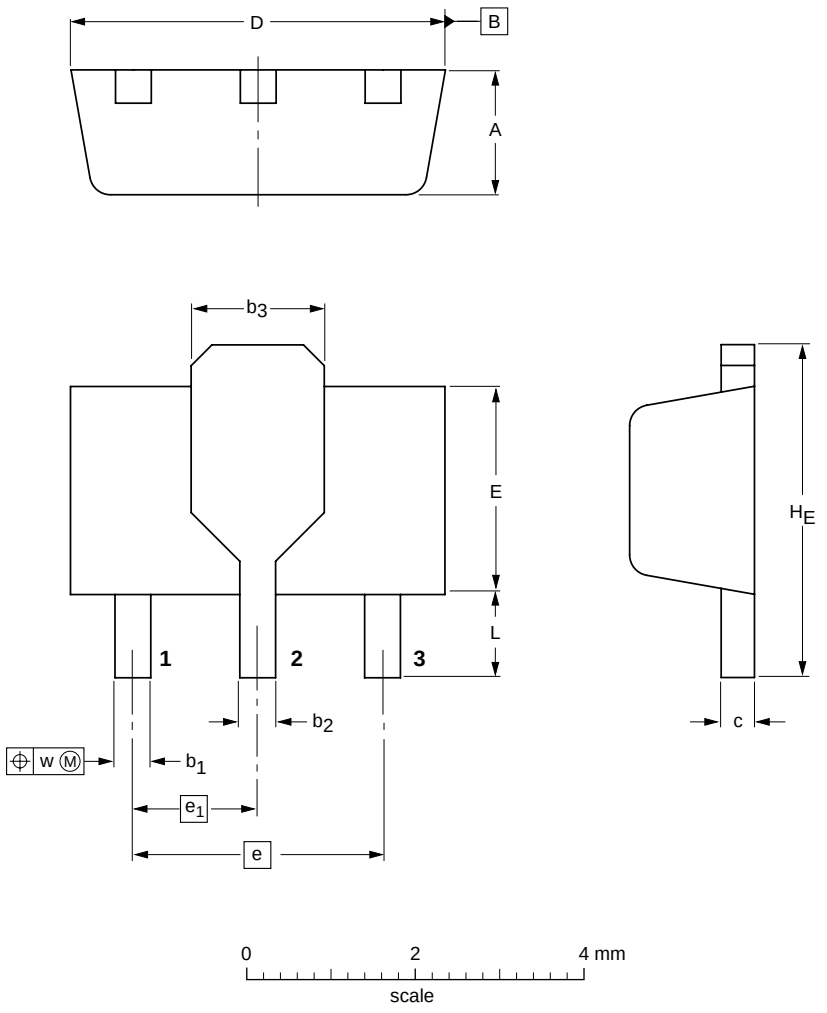
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

I_D = 500 mA; V_{GS} = 10 V.

Fig.10 Temperature coefficient of drain-source on-state resistance; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; drain pad for good heat transfer; 3 leads **SOT89**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_1	b_2	b_3	c	D	E	e	e_1	H_E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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