LP2950-N/LP2951-N Series of Adjustable Micropower Voltage Regulators

Check for Samples: LP2950-N, LP2951-N

FEATURES

- **5V, 3V, and 3.3V Versions Available**
- **High Accuracy Output Voltage**
- **Ensured 100 mA Output Current**
- **Extremely Low Quiescent Current**
- **Low Dropout Voltage**
- **Extremely Tight Load and Line Regulation**
- **Very Low Temperature Coefficient**
- **Use as Regulator or Reference**
- **Needs Minimum Capacitance for Stability**
- **Current and Thermal Limiting**
- **Stable With Low-ESR Output Capacitors (10 mΩ to 6Ω)**

LP2951-N VERSIONS ONLY

- **Error Flag Warns of Output Dropout**
- **Logic-Controlled Electronic Shutdown**
- **Output Programmable From 1.24 to 29V**

DESCRIPTION

The LP2950-N and LP2951-N are micropower voltage regulators with very low quiescent current (75 µA typ.) and very low dropout voltage (typ. 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950-N/LP2951-N increases only slightly in dropout, prolonging battery life.

The LP2950-N-5.0 is available in the surface-mount PFM package, and in the popular 3-pin TO-92 package for pin-compatibility with older 5V regulators. The 8-lead LP2951-N is available in plastic, ceramic dual-in-line, WSON, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V, 3V, or 3.3V output (depending on the version), or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950-N/LP2951-N has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

Block Diagram and Typical Applications

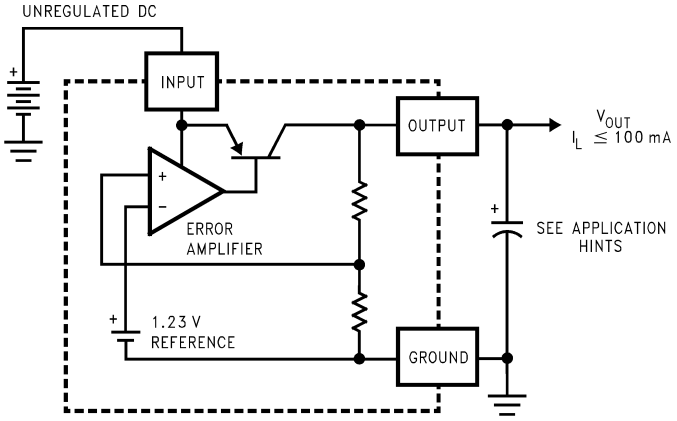


Figure 1. LP2950-N

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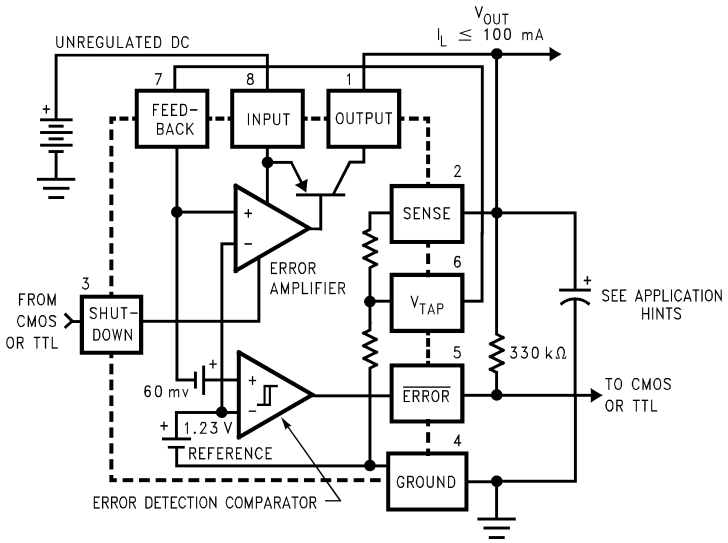


Figure 2. LP2951-N

Connection Diagrams

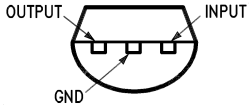


Figure 3. TO-92 Plastic Package (LP) Bottom View

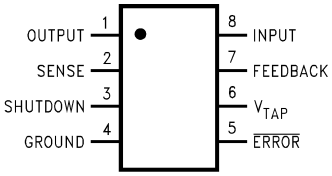


Figure 4. Dual-In-Line Packages (P, NAB) Surface-Mount Package (D, DGK) Top View

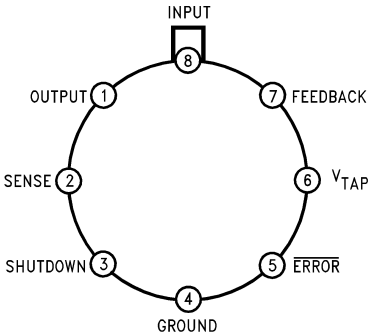


Figure 5. Metal Can Package (LMC) Top View

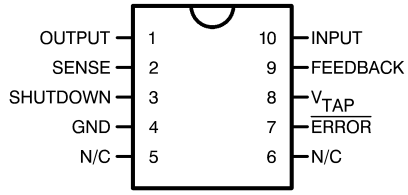


Figure 6. 10-Lead Ceramic Surface-Mount Package (NAC) Top View

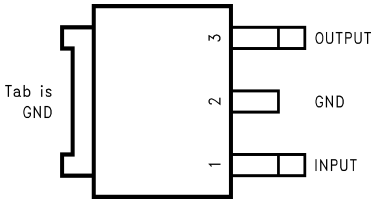
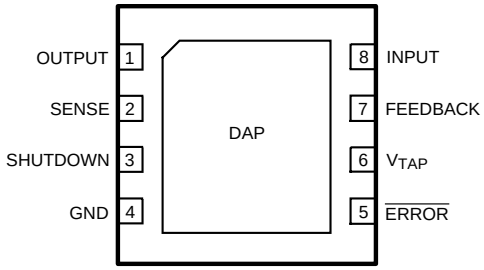


Figure 7. PFM (NDP) Front View



Connect DAP to GND at device pin 4.

Figure 8. 8-Lead WSON (NGT) Top View

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Input Supply Voltage - SHUTDOWN Input Voltage Error Comparator Output Voltage(3)		−0.3 to +30V
FEEDBACK Input Voltage(3)(4)		−1.5 to +30V
Power Dissipation		Internally Limited
Junction Temperature (T_J)		+150°C
Ambient Storage Temperature		−65° to +150°C
Soldering Dwell Time, Temperature	Wave	4 seconds, 260°C
	Infrared	10 seconds, 240°C
	Vapor Phase	75 seconds, 219°C
ESD Rating	Human Body Model(5)	2500V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) May exceed input supply voltage.
(4) When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.
(5) Human Body Model (HBM) is 1.5 kΩ in series with 100 pF; LP2950-N passes 2.5 kV (HBM) ESD; LP2951-N passes 2.5 kV (HBM) except: Feedback pin passes 1kV (HBM) and Shutdown pin passes 2kV (HBM).

OPERATING RATINGS(1)

Maximum Input Supply Voltage		30V
Junction Temperature Range (T_J)(2)	LP2950AC-XX, LP2950C-XX	−40° to +125°C
	LP2951	−55° to +150°C
	LP2951AC-XX, LP2951C-XX	−40° to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) The junction-to-ambient thermal resistances are as follows: 180°C/W and 160°C/W for the TO-92 package with 0.40 inch and 0.25 inch leads to the printed circuit board (PCB) respectively, 105°C/W for the molded PDIP (P), 130°C/W for the ceramic DIP (NAB), 160°C/W for the molded plastic SOIC (D), 200°C/W for the molded plastic VSSOP (DGK), and 160°C/W for the metal can package (LMC). The above thermal resistances for the P, NAB, D, and DGK packages apply when the package is soldered directly to the PCB. Junction-to-case thermal resistance for the LMC package is 20°C/W. Junction-to-case thermal resistance for the PFM package is 5.4°C/W. The value of θ_{JA} for the WSON package is typically 51°C/W but is dependent on the PCB trace area, trace material, and the number of layers and thermal vias. For details of thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (literature number SNOA401).

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ELECTRICAL CHARACTERISTICS[1]

Parameter	Conditions[1]	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit[2][3]	Typ	Tested Limit[2]	Design Limit[4]	Typ	Tested Limit[2]	Design Limit[4]	
3V Versions[5]										
Output Voltage	T_J = 25°C	3.0	3.015	3.0	3.015		3.0	3.030		V max
			2.985		2.985			2.970		V min
	−25°C ≤ T_J ≤ 85°C	3.0		3.0		3.030	3.0		3.045	V max
						2.970			2.955	V min
	Full Operating Temperature Range	3.0	**3.036**	3.0		**3.036**	3.0		**3.060**	V max
			2.964			**2.964**			**2.940**	V min
Output Voltage	100 µA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}	3.0	**3.045**	3.0		**3.042**	3.0		**3.072**	V max
			2.955			**2.958**			**2.928**	V min
3.3V Versions[5]										
Output Voltage	T_J = 25°C	3.3	3.317	3.3	3.317		3.3	3.333		V max
			3.284		3.284			3.267		V min
	−25°C ≤ T_J ≤ 85°C	3.3		3.3		3.333	3.3		3.350	V max
						3.267			3.251	V min
	Full Operating Temperature Range	3.3	**3.340**	3.3		**3.340**	3.3		**3.366**	V max
			3.260			**3.260**			**3.234**	V min
Output Voltage	100 µA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}	3.3	**3.350**	3.3		**3.346**	3.3		**3.379**	V max
			3.251			**3.254**			**3.221**	V min
5V Versions[5]										
Output Voltage	T_J = 25°C	5.0	5.025	5.0	5.025		5.0	5.05		V max
			4.975		4.975			4.95		V min
	−25°C ≤ T_J ≤ 85°C	5.0		5.0		5.05	5.0		5.075	V max
						4.95			4.925	V min
	Full Operating Temperature Range	5.0	**5.06**	5.0		**5.06**	5.0		**5.1**	V max
			4.94			**4.94**			**4.9**	V min
Output Voltage	100 µA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}	5.0	**5.075**	5.0		**5.075**	5.0		**5.12**	V max
			4.925			**4.925**			**4.88**	V min
All Voltage Options										
Output Voltage Temperature Coefficient	See[6]	**20**	**120**	**20**		**100**	**50**		**150**	ppm/°C
Line Regulation[7]	(V_ONOM + 1)V ≤ V_{in} ≤ 30V[8]	0.03	0.1	0.03	0.1		0.04	0.2		% max
			0.5			**0.2**			**0.4**	% max

(1) Unless otherwise noted, all limits specified for V_{IN} = (V_{ONOM} + 1)V, I_L = 100 µA and C_L = 1µF for 5V versions and 2.2 µF for 3V and 3.3V versions. Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for T_A = T_J = 25°C. Additional conditions for the 8-pin versions are FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE, and $V_{SHUTDOWN}$ ≤ 0.8V.
(2) Ensured and 100% production tested.
(3) A Military RETS specification is available on request. At time of printing, the LP2951-N RETS specification complied with the boldface limits in this column. The LP2951-N LMC, NAC, or NAB may also be procured as Standard Military Drawing Spec #5962-3870501MGA, MXA, or MPA.
(4) Ensured but not 100% production tested. These limits are not used to calculate outgoing AQL levels.
(5) All LP2950 devices have the nominal output voltage coded as the last two digits of the part number. In the LP2951 products, the 3.0V and 3.3V versions are designated by the last two digits, but the 5V version is denoted with no code at this location of the part number (refer to ordering information table).
(6) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
(7) Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
(8) Line regulation for the LP2951-N is tested at 150°C for I_L = 1mA. For I_L = 100 µA and T_J = 125°C, line regulation is specified by design to 0.2%. See TYPICAL PERFORMANCE CHARACTERISTICS for line regulation versus temperature and load current.

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ELECTRICAL CHARACTERISTICS[1] (continued)

Parameter	Conditions[1]	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit[2][3]	Typ	Tested Limit[2]	Design Limit[4]	Typ	Tested Limit[2]	Design Limit[4]	
Load Regulation[7]	100 µA ≤ I_L ≤ 100 mA	0.04	0.1	0.04	0.1		0.1	0.2		% max
			0.3			**0.2**			**0.3**	% max
Dropout Voltage[9]	I_L = 100 µA		80		80			80		mV max
		50	**150**	50		**150**	50		**150**	mV max
	I_L = 100 mA		450		450			450		mV max
		380	**600**	380		**600**	380		**600**	mV max
Ground Current	I_L = 100 µA	75	120	75	120		75	120		µA max
			140			**140**			**140**	µA max
	I_L = 100 mA	8	12	8	12		8	12		mA max
			14			**14**			**14**	mA max
Dropout Ground Current	V_{in} = (V_ONOM − 0.5)V I_L = 100 µA	110	170	110	170		110	170		µA max
			200			**200**			**200**	µA max
Current Limit	V_{out} = 0	160	200	160	200		160	200		mA max
			220			**220**			**220**	mA max
Thermal Regulation	See[10]	0.05	0.2	0.05	0.2		0.05	0.2		%/W max
Output Noise, 10 Hz to 100 kHz	C_L = 1µF (5V Only)	430		430			430			µV rms
	C_L = 200 µF	160		160			160			µV rms
	C_L = 3.3 µF (Bypass = 0.01 µF Pins 7 to 1 (LP2951-N)	100		100			100			µV rms
8-pin Versions Only		**LP2951**		**LP2951AC-XX**			**LP2951C-XX**			
Reference Voltage		1.235	1.25	1.235	1.25		1.235	1.26		V max
			1.26			**1.26**			**1.27**	V max
			1.22		1.22			1.21		V min
			1.2			**1.2**			**1.2**	V min
Reference Voltage	See[11]		**1.27**			**1.27**			**1.285**	V max
			1.19			**1.19**			**1.185**	V min
Feedback Pin Bias Current		20	40	20	40		20	40		nA max
			60			**60**			**60**	nA max
Reference Voltage Temperature Coefficient	See[12]	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C

(9) Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.
(10) Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10ms.
(11) $V_{REF} \le V_{OUT} \le (V_{IN} - 1V)$, 2.3V ≤ V_{IN} ≤ 30V, 100 µA ≤ I_L ≤ 100 mA, $T_J \le T_{JMAX}$.
(12) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

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ELECTRICAL CHARACTERISTICS[1] (continued)

Parameter	Conditions[1]	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit[2][3]	Typ	Tested Limit[2]	Design Limit[4]	Typ	Tested Limit[2]	Design Limit[4]	
Error Comparator										
Output Leakage Current	V_{OH} = 30V	0.01	1	0.01	1		0.01	1		µA max
			2			**2**			**2**	µA max
Output Low Voltage	V_{in} = (V_ONOM − 0.5)V I_{OL} = 400µA	150	250	150	250		150	250		mV max
			400			**400**			**400**	mV max
Upper Threshold Voltage	See[13]	60	40	60	40		60	40		mV min
			25			**25**			**25**	mV min
Lower Threshold Voltage	See[13]	75	95	75	95		75	95		mV max
			140			**140**			**140**	mV max
Hysteresis	See[13]	15		15			15			mV
Shutdown Input										
Input		1.3		1.3			1.3			V
Logic	Low (Regulator ON)		**0.6**			**0.7**			**0.7**	V max
Voltage	High (Regulator OFF)		**2.0**			**2.0**			**2.0**	V min
Shutdown Pin Input Current	$V_{shutdown}$ = 2.4V	30	50	30	50		30	50		µA max
			100			**100**			**100**	µA max
	$V_{shutdown}$ = 30V	450	600	450	600		450	600		µA max
			750			**750**			**750**	µA max
Regulator Output Current in Shutdown	See[14]	3	10	3	10		3	10		µA max
			20			**20**			**20**	µA max

(13) Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at V_{in} = (V_ONOM + 1)V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2.For example, at a programmed output voltage of 5V, the Error output is specified to go low when the output drops by 95 mV × 5V/1.235V = 384 mV. Thresholds remain constant as a percent of V_{out} as V_{out} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% ensured.

(14) $V_{SHUTDOWN} \geq 2V$, $V_{IN} \leq 30V$, V_{OUT} = 0, Feedback pin tied to V_{TAP}.

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TYPICAL PERFORMANCE CHARACTERISTICS

Quiescent Current

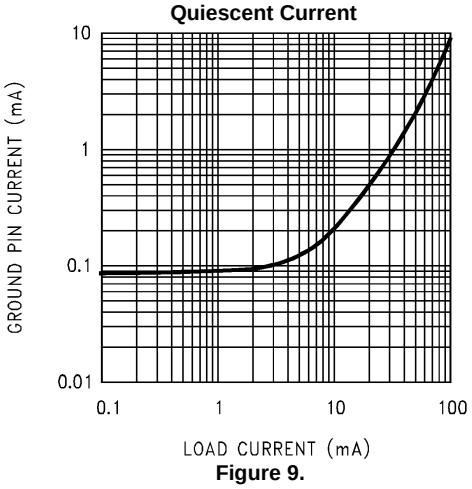


Figure 9.

Dropout Characteristics

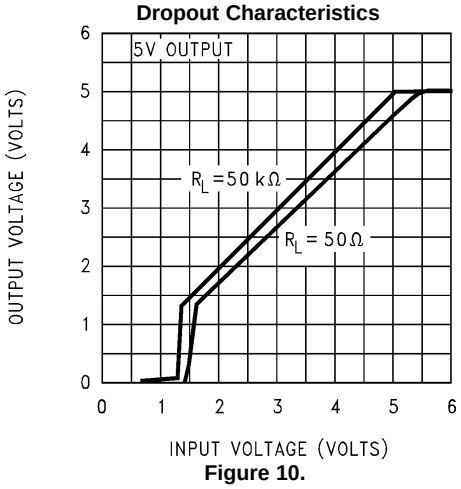


Figure 10.

Input Current

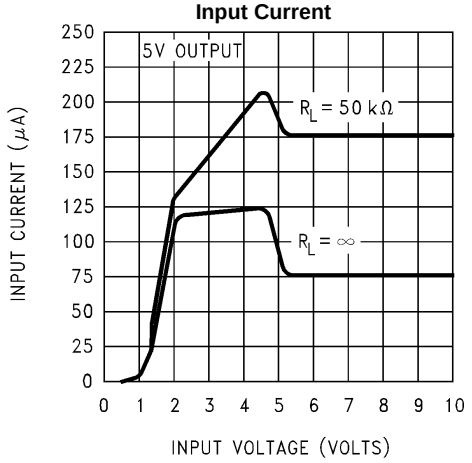


Figure 11.

Input Current

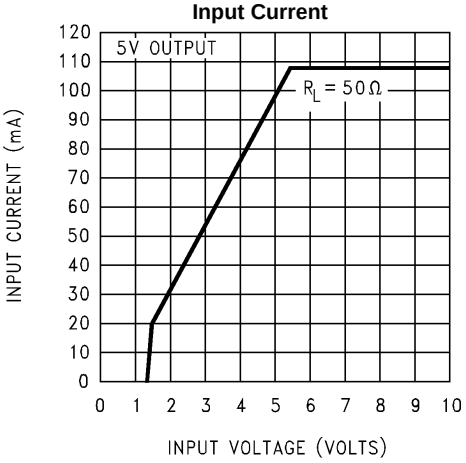


Figure 12.

Output Voltage vs. Temperature of 3 Representative Units

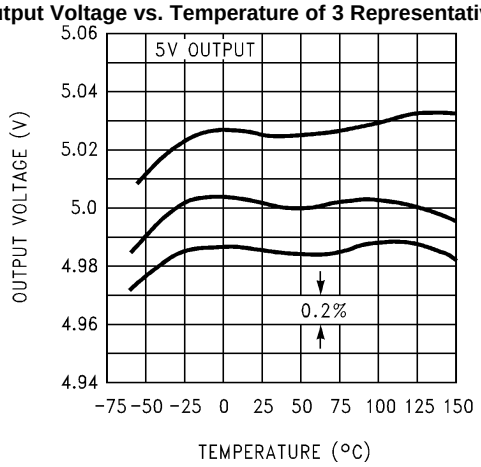


Figure 13.

Quiescent Current

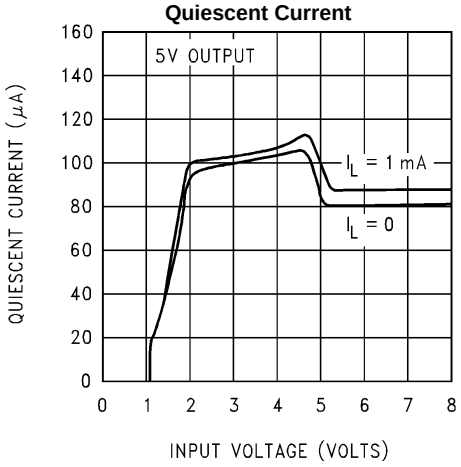


Figure 14.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Quiescent Current

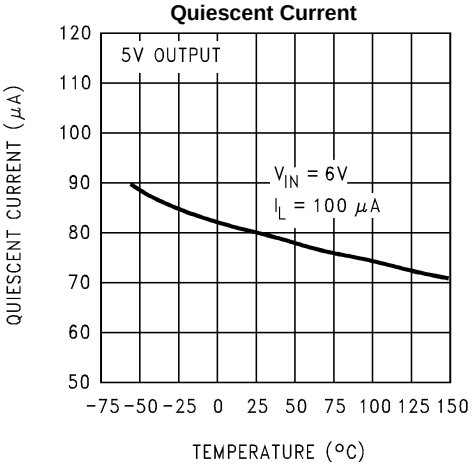


Figure 15.

Quiescent Current

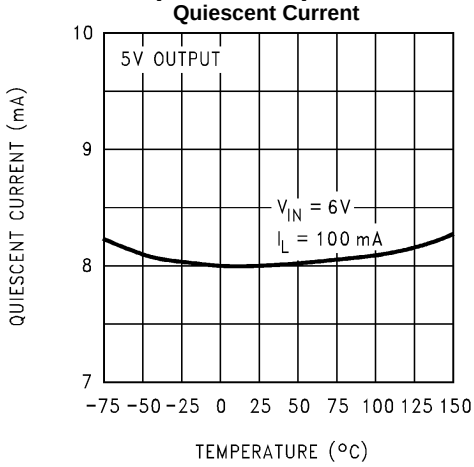


Figure 16.

Quiescent Current

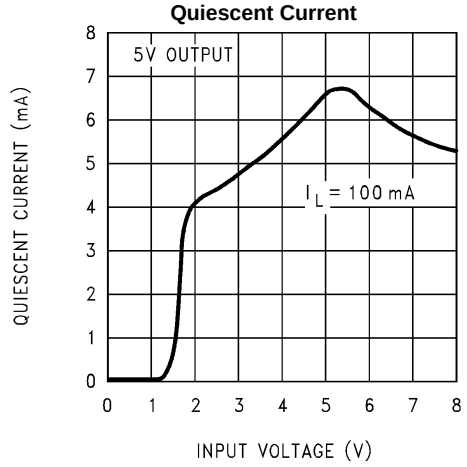


Figure 17.

Short Circuit Current

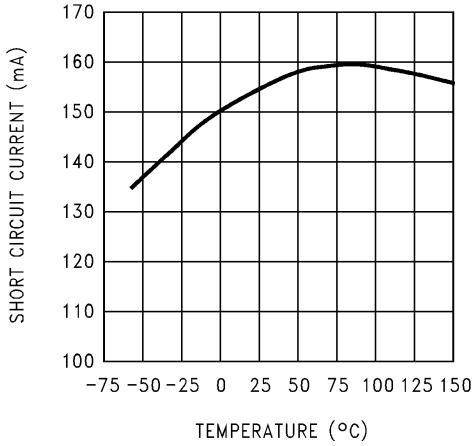


Figure 18.

Dropout Voltage

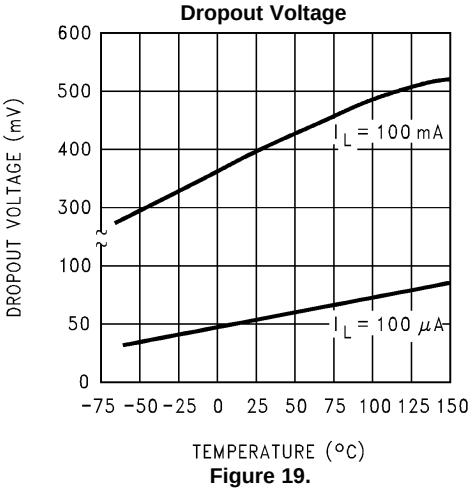


Figure 19.

Dropout Voltage

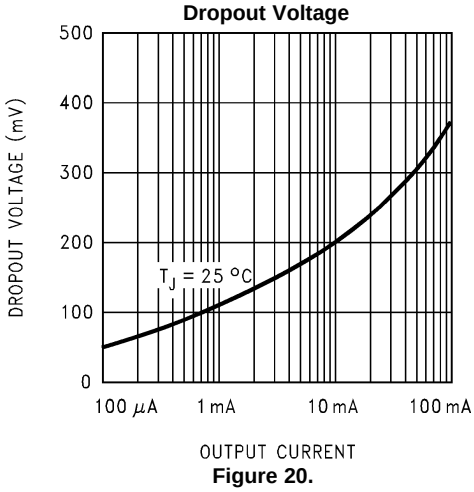


Figure 20.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LP2951-N Minimum Operating Voltage

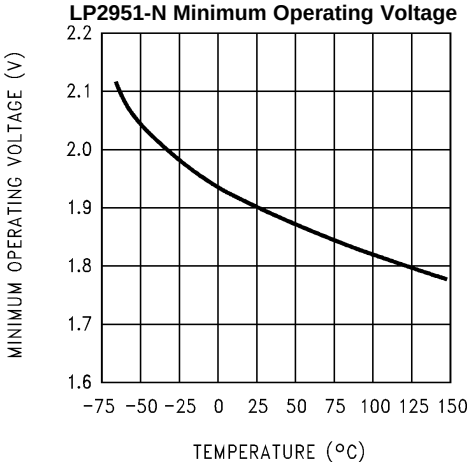


Figure 21.

LP2951-N Feedback Bias Current

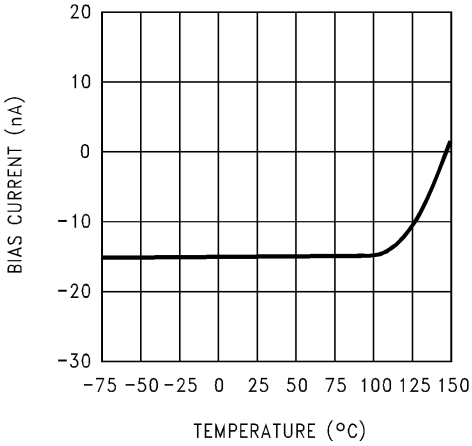


Figure 22.

LP2951-N Feedback Pin Current

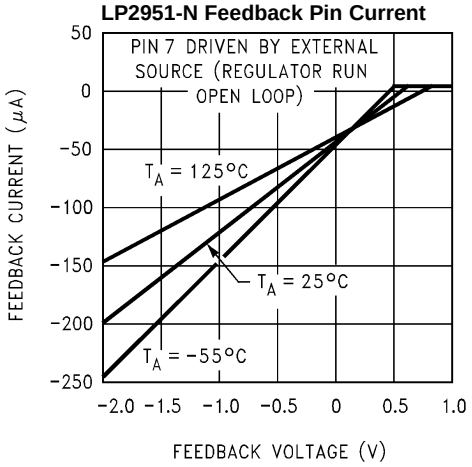


Figure 23.

LP2951-N Error Comparator Output

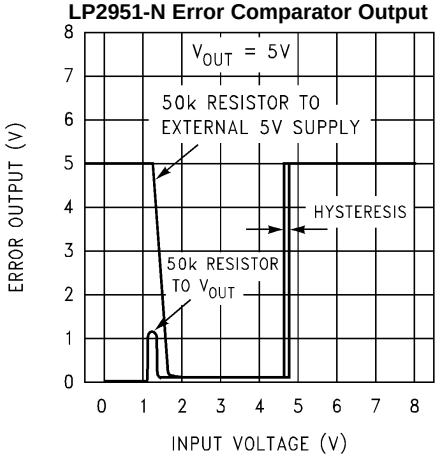


Figure 24.

LP2951-N Comparator Sink Current

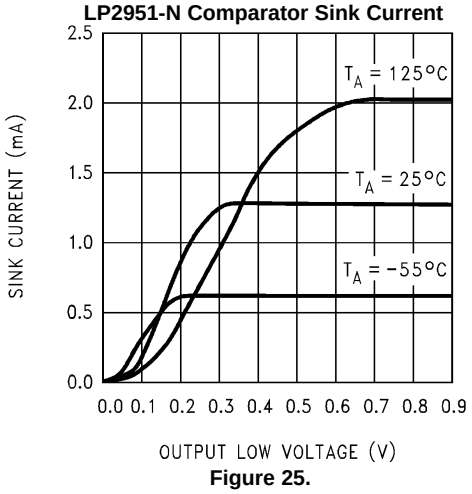


Figure 25.

Line Transient Response

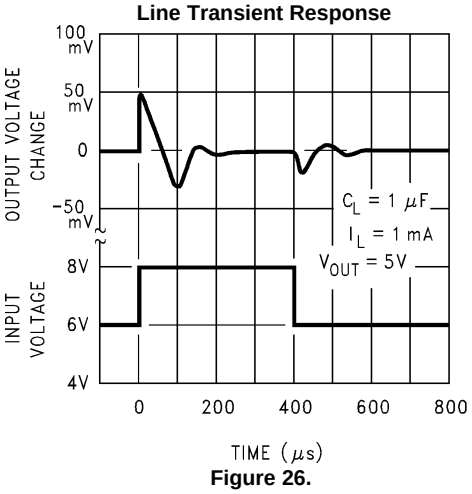


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Load Transient Response

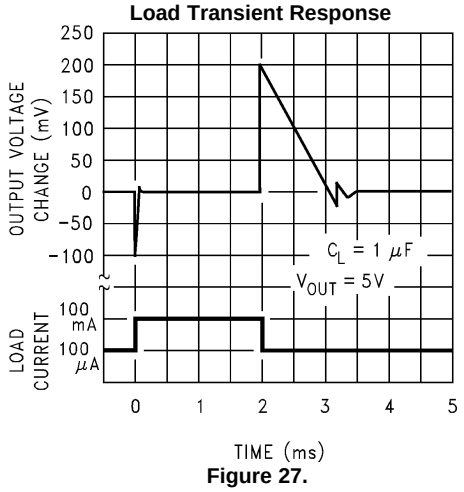


Figure 27.

Load Transient Response

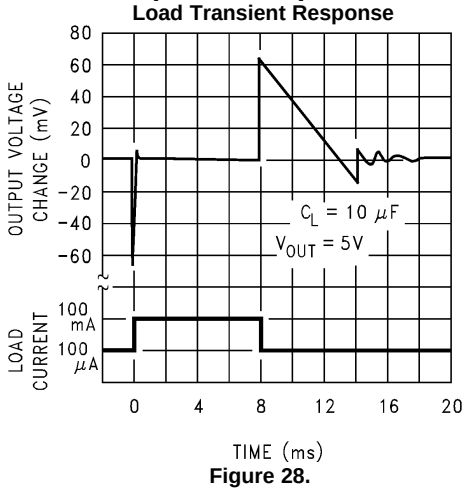


Figure 28.

LP2951-N Enable Transient

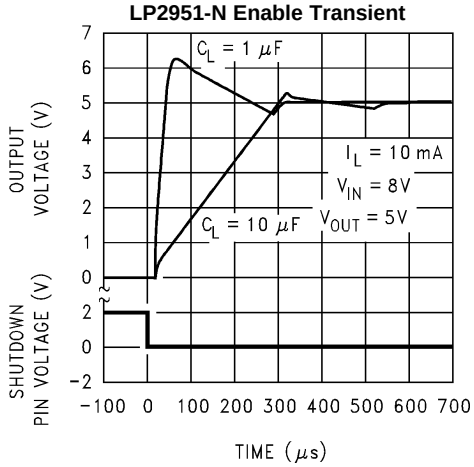


Figure 29.

Output Impedance

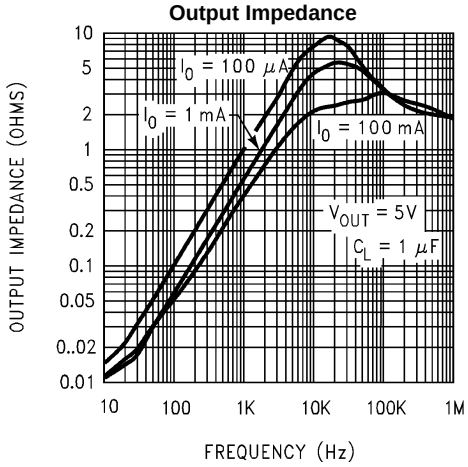


Figure 30.

Ripple Rejection

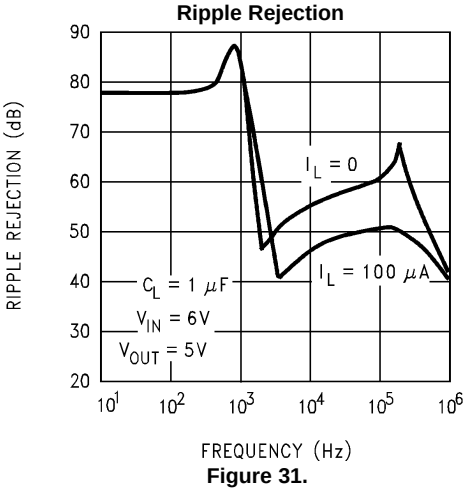


Figure 31.

Ripple Rejection

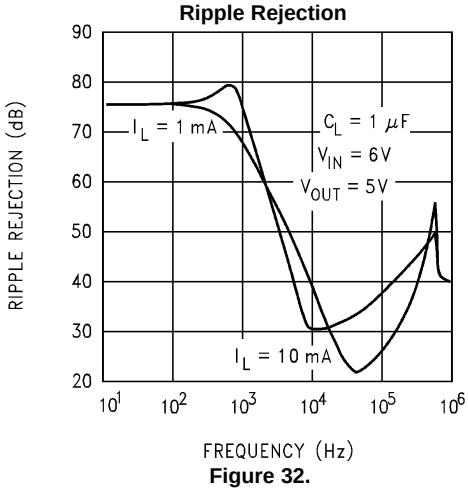


Figure 32.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Ripple Rejection

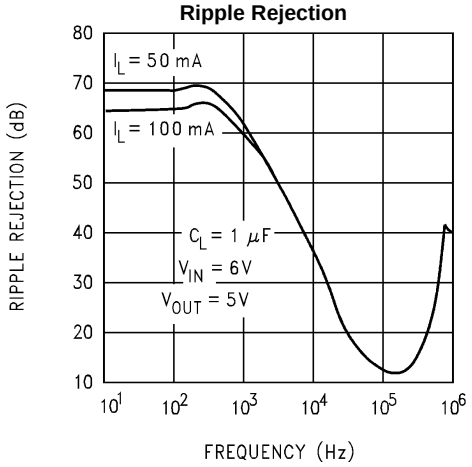


Figure 33.

LP2951-N Output Noise

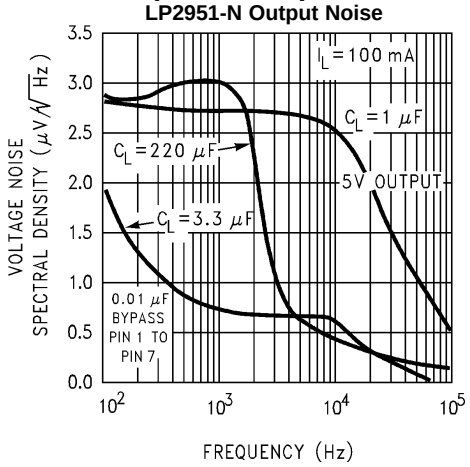


Figure 34.

LP2951-N Divider Resistance

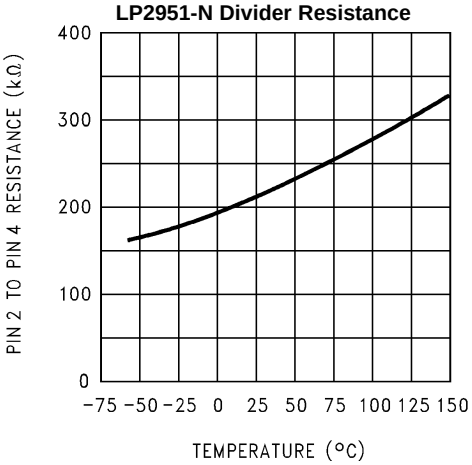


Figure 35.

Shutdown Threshold Voltage

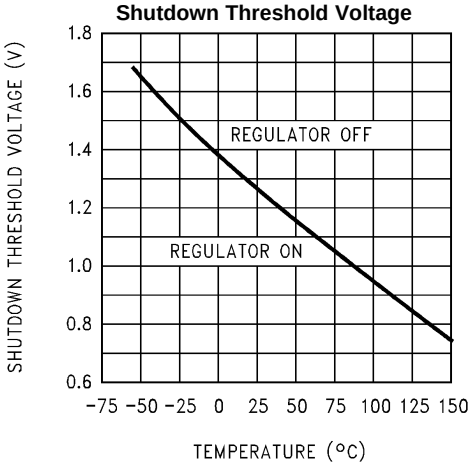


Figure 36.

Line Regulation

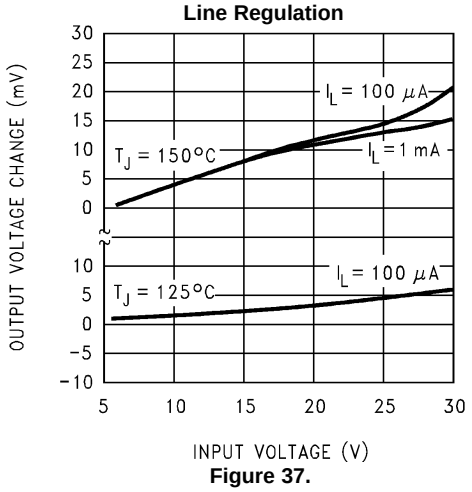


Figure 37.

LP2951-N Maximum Rated Output Current

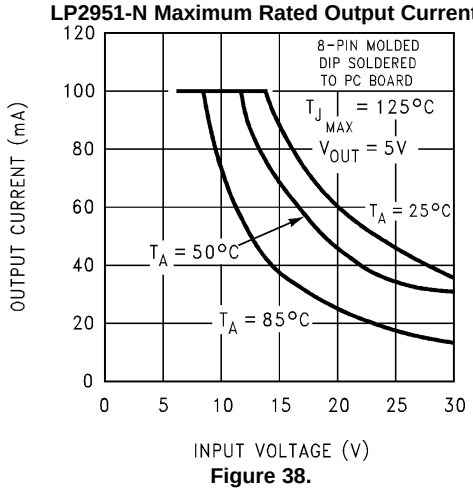


Figure 38.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LP2950-N Maximum Rated Output Current

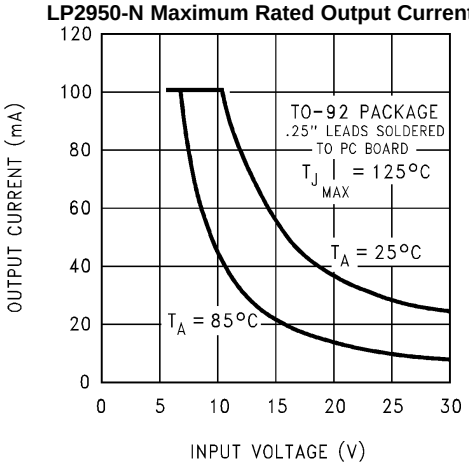


Figure 39.

Thermal Response

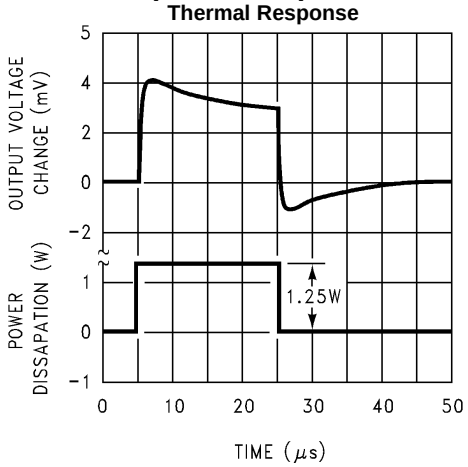


Figure 40.

Output Capacitor ESR Range

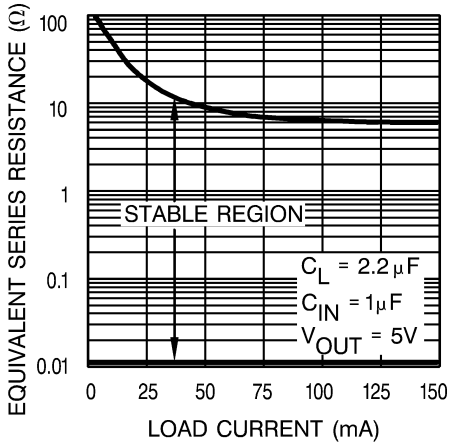


Figure 41.

LP2951-N Input Pin Current vs Input Voltage

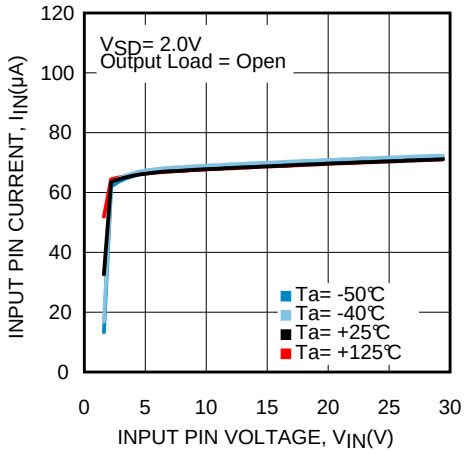


Figure 42.

LP2951-N Input Pin Current vs Input Voltage

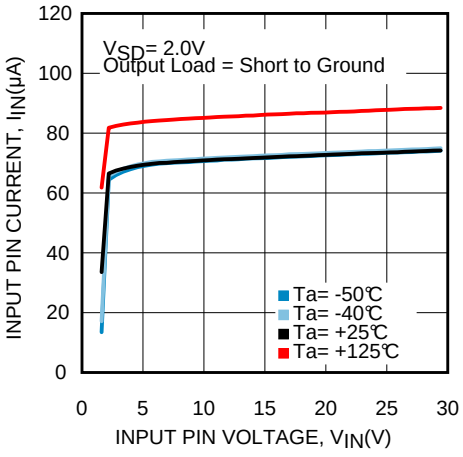


Figure 43.

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APPLICATION HINTS

Output Capacitor Requirements

A 1.0 µF (or greater) capacitor is required between the output and ground for stability at output voltages of 5V or higher. At lower output voltages, more capacitance is required (2.2 µF or more is recommended for 3.0V and 3.3V versions). Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytic work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

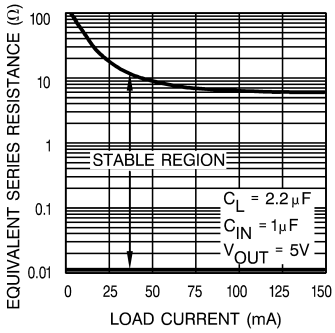


Figure 44. Output Capacitor ESR Range

The reason for the lower ESR limit is that the loop compensation of the feedback loop relies on the capacitance value and the ESR value of the output capacitor to provide the zero that gives added phase lead (See Figure 44).

$$f_Z = (1 / (2 \times \pi \times C_{OUT} \times ESR)) \quad (1)$$

Using the 2.2 µF value from the *Output Capacitor ESR Range* curve (Figure 44), a useful range for f_Z can be estimated:

$$f_{Z(MIN)} = (1 / (2 \times \pi \times 2.2\ \mu F \times 5\Omega)) = 14.5\ kHz \quad (2)$$

$$f_{Z(MAX)} = (1 / (2 \times \pi \times 2.2\ \mu F \times 0.05\Omega)) = 318\ kHz \quad (3)$$

For ceramic capacitors, the low ESR produces a zero at a frequency that is too high to be useful, so meaningful phase lead does not occur. A ceramic output capacitor can be used if a series resistance is added (recommended value of resistance about 0.1Ω to 2Ω) to simulate the needed ESR. Only X5R, X7R, or better, MLCC types should be used, and should have a DC voltage rating at least twice the $V_{OUT(NOM)}$ value.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 µF for currents below 10 mA or 0.1 µF for currents below 1 mA. Using the adjustable versions at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a 3.3 µF (or greater) capacitor should be used.

Unlike many other regulators, the LP2950-N will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951-N versions with external resistors, a minimum load of 1 µA is recommended.

Applications having conditions that may drive the LP2950-N/51 into nonlinear operation require special consideration. Nonlinear operation will occur when the output voltage is held low enough to force the output stage into output current limiting while trying to pull the output voltage up to the regulated value. The internal loop response time will control how long it takes for the device to regain linear operation when the output has returned to the normal operating range. There are three significant nonlinear conditions that need to be considered, all can force the output stage into output current limiting mode, all can cause the output voltage to over-shoot with low

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value output capacitors when the condition is removed, and the recommended generic solution is to set the output capacitor to a value not less than 10 µF. Although the 10 µF value for C_{OUT} may not eliminate the output voltage over-shoot in all cases, it should lower it to acceptable levels (<10% of $V_{OUT(NOM)}$) in the majority of cases. In all three of these conditions, applications with lighter load currents are more susceptible to output voltage over-shoot than applications with higher load currents.

1) At power-up, with the input voltage rising faster than output stage can charge the output capacitor.

$V_{IN}\ t_{RISE(MIN)} > ((C_{OUT} / 100\ mA) \times \Delta V_{IN})$

where

- $\Delta V_{IN} = V_{OUT(NOM)} + 1.0V$ (4)

2) Recovery from an output short circuit to ground condition.

$C_{OUT(MIN)} \approx (160\ mA - I_{LOAD(NOM)})/((V_{OUT(NOM)}/10)/25\ \mu s))$ (5)

3) Toggling the LP2951-N SHUTDOWN pin from high (i.e. OFF) to low (i.e. ON).

$C_{OUT(MIN)} \approx (160\ mA - I_{LOAD(NOM)})/((V_{OUT(NOM)}/10)/25\ \mu s))$ (6)

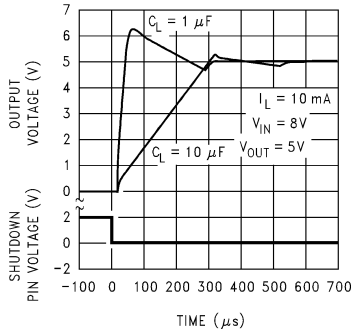


Figure 45. LP2951-N Enable Transient

Input Capacitor Requirements

A minimum 1 µF tantalum, ceramic or aluminum electrolytic capacitor should be placed from the LP2950-N/LP2951-N input pin to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

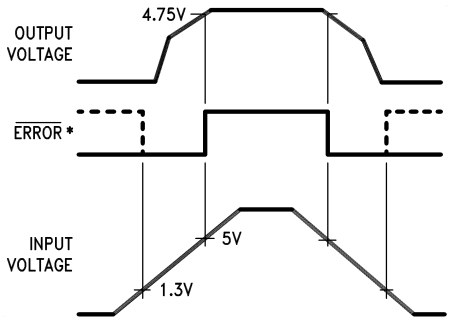
Error Detection Comparator Output

The comparator produces a logic low output whenever the LP2951-N output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60mV divided by the 1.235 reference voltage. (Refer to the block diagram in the front of the datasheet.) This trip level remains “5% below normal” regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 46 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951-N input is ramped up and down. For 5V versions, the $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75V). Since the LP2951-N's dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pull up resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 MΩ. The resistor is not required if this output is unused.

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*When $V_{IN} \leq 1.3V$, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see Figure 47), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

Figure 46. $\overline{\text{ERROR}}$ Output Timing

Programming the Output Voltage (LP2951-N)

The LP2951-N may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying the output and sense pins together, and also tying the feedback and V_{TAP} pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in Figure 47, an external pair of resistors is required.

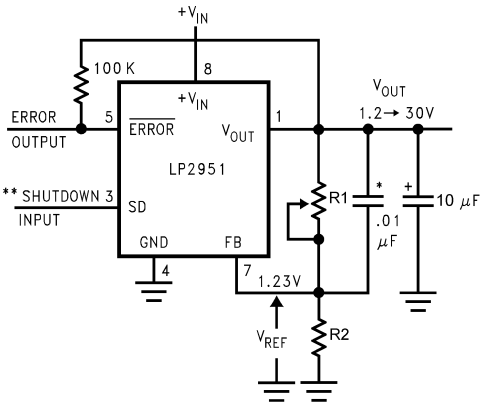
The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1 \quad (7)$$

where

- V_{REF} is the nominal 1.235V reference voltage and I_{FB} is the feedback pin bias current, nominally -20nA

The minimum recommended load current of 1 µA forces an upper limit of 1.2 MΩ on the value of R2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R2 = 100 kΩ reduces this error to 0.17% while increasing the resistor program current to 12 µA. Since the LP2951-N typically draws 60 µA at no load with Pin 2 open-circuited, this is a small price to pay.



*See Application Hints

$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

Figure 47. Adjustable Regulator

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Stray capacitance to the LP2951-N Feedback terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between the Output pin and the Feedback pin,and increasing the output capacitor to at least 3.3 µF, will fix this problem.

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP2950-N but is relatively inefficient, as increasing the capacitor from 1 µF to 220 µF only decreases the noise from 430 $\mu V_{(RMS)}$ to 160 $\mu V_{(RMS)}$ for a 100 kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz} \tag{8}$$

or about 0.01 µF. When doing this, the output capacitor must be increased to 3.3 µF to maintain stability. These changes reduce the output noise from 430 µV to 100 µV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

WSON Mounting

The NGT (No Pullback) 8-Lead WSON package requires specific mounting techniques which are detailed in Application Note 1187 (literature number SNOA401). Referring to the ***PCB Design Recommendations*** section (literature number SNOA401), it should be noted that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the eight pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device lead 4 (i.e. GND). Alternately, but not recommended, the DAP may be left floating (i.e. no electrical connection). The DAP must not be connected to any potential other than ground.

For the LP2951-N in the NGT 8-Lead WSON package, the junction-to-case thermal rating, θ_{JC}, is 14.2°C/W, where the case is the bottom of the package at the center of the DAP. The junction-to-ambient thermal performance for the LP2951-N in the NGT 8-Lead WSON package, using the JEDEC JESD51 standards is summarized in the following table:

Board Type	Thermal Vias	θ_{JC}	θ_{JA}
JEDEC 2-Layer JESD 51-3	None	14.2°C/W	185°C/W
JEDEC 4-Layer JESD 51-7	1	14.2°C/W	68°C/W
	2	14.2°C/W	60°C/W
	4	14.2°C/W	51°C/W
	6	14.2°C/W	48°C/W

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Typical Applications

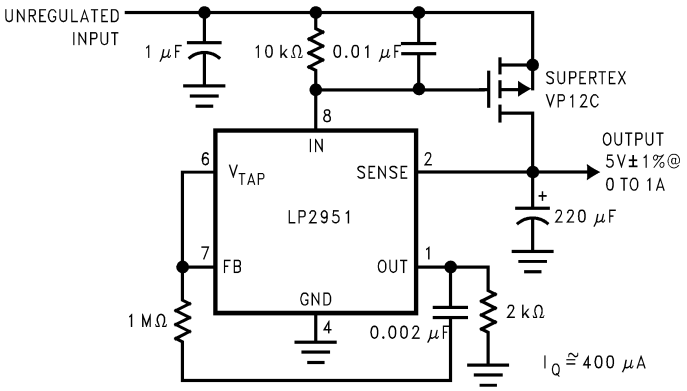


Figure 48. 1A Regulator with 1.2V Dropout

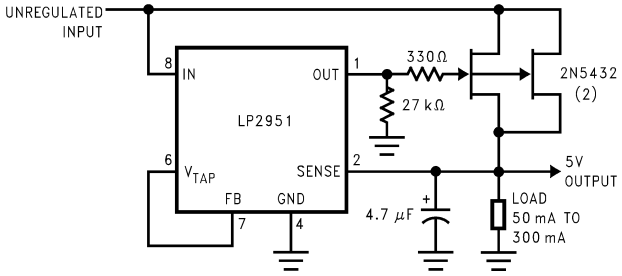
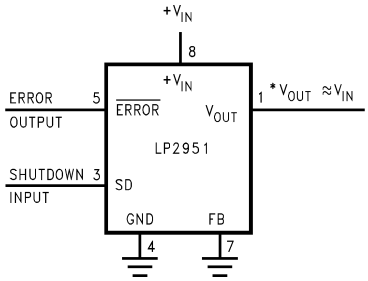


Figure 49. 300mA Regulator with 0.75V Dropout



*Minimum input-output voltage ranges from 40mV to 400mV, depending on load current. Current limit is typically 160mA.

Figure 50. Wide Input Voltage Range Current Limiter

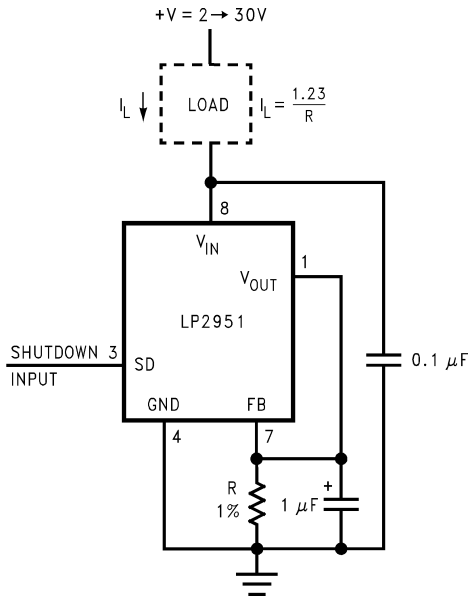
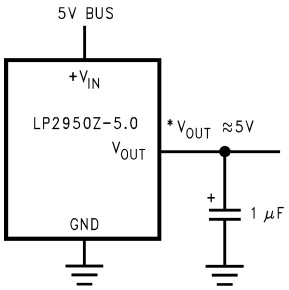


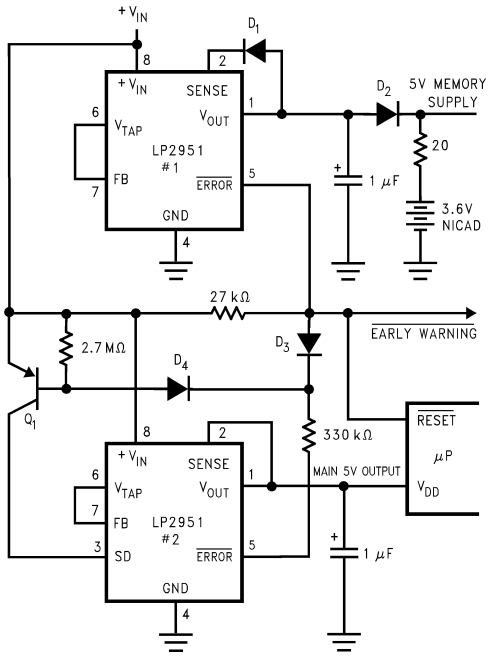
Figure 51. Low Drift Current Source



*Minimum input-output voltage ranges from 40mV to 400mV, depending on load current. Current limit is typically 160mA.

Figure 52. 5 Volt Current Limiter

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- Early warning flag on low input voltage
- Main output latches off at lower input voltages
- Battery backup on auxiliary output
- Operation: Reg. #1's V_{OUT} is programmed one diode drop above 5V. Its error flag becomes active when $V_{IN} \leq$ 5.7V. When V_{IN} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When V_{IN} again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

Figure 53. Regulator with Early Warning and Auxiliary Output

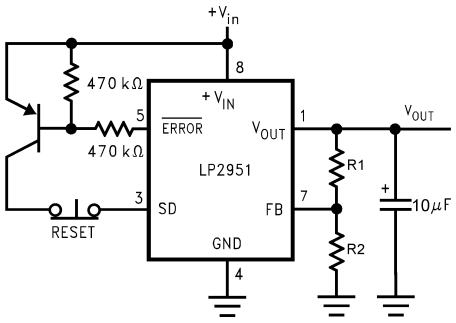
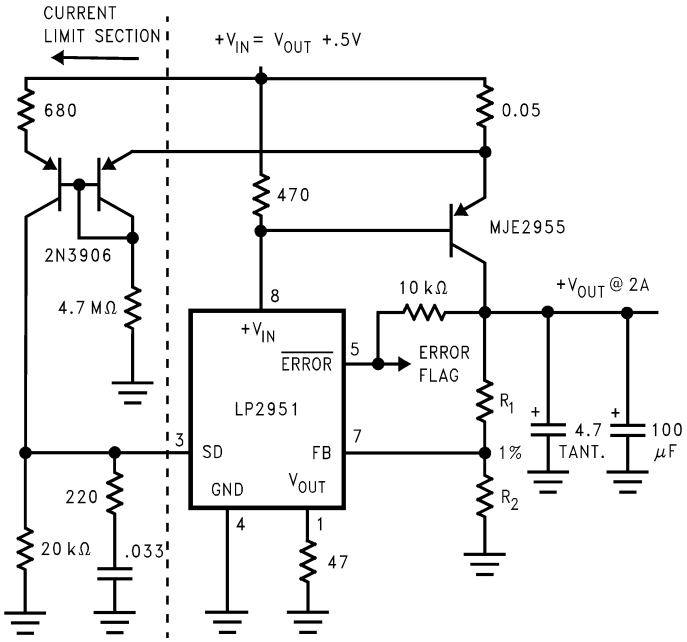


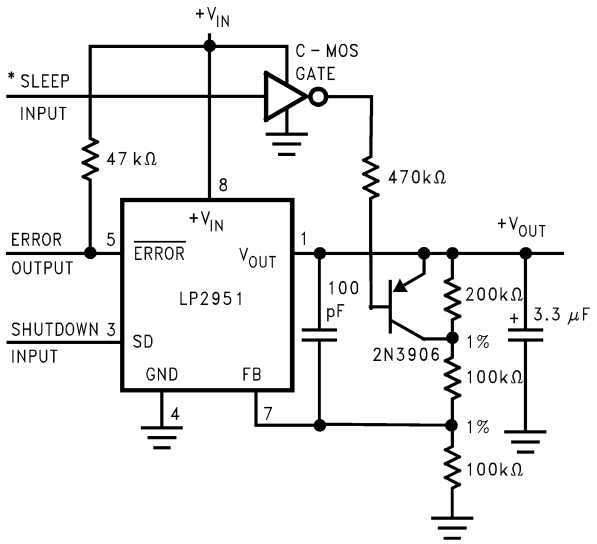
Figure 54. Latch Off When Error Flag Occurs



$V_{out} = 1.23V \left(1 + \frac{R_1}{R_2}\right)$

For $5V_{out}$, use internal resistors. Wire pin 6 to 7, & wire pin 2 to $+V_{out}$ Bus.

Figure 55. 2 Ampere Low Dropout Regulator



*High input lowers V_{out} to 2.5V

Figure 56. 5V Regulator with 2.5V Sleep Function

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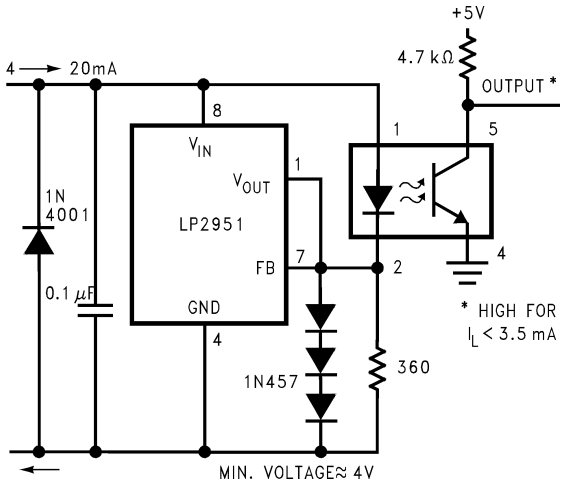
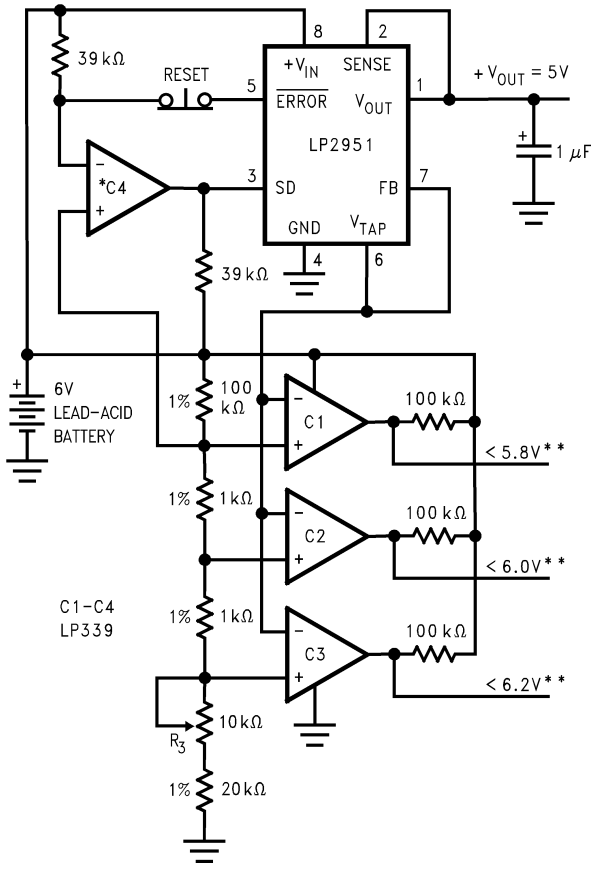
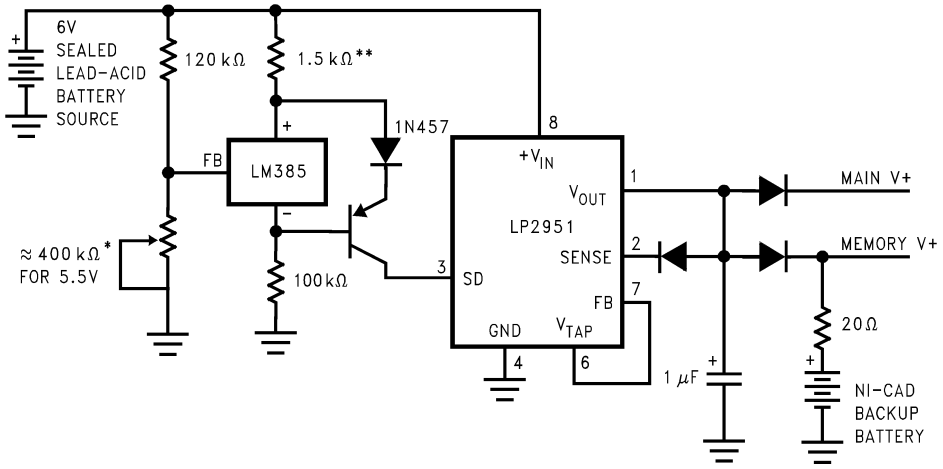


Figure 57. Open Circuit Detector for 4 → 20mA Current Loop



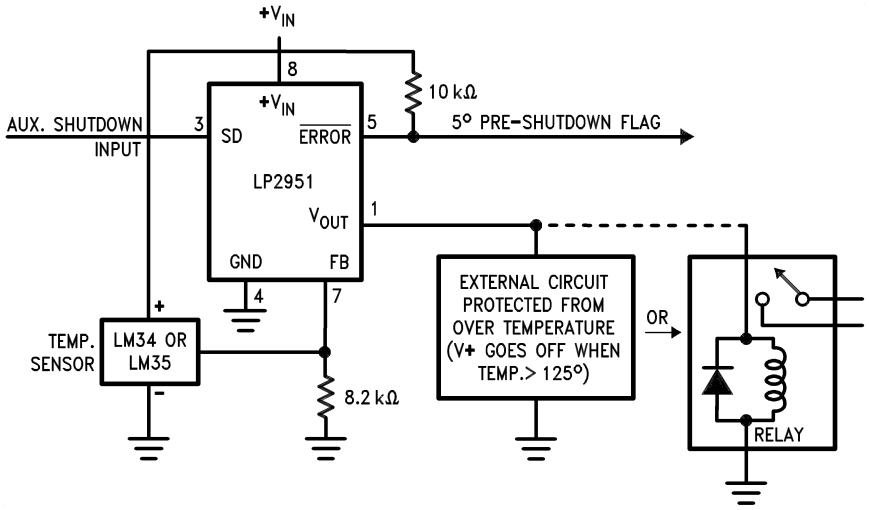
*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V
**Outputs go low when V_{IN} drops below designated thresholds.

Figure 58. Regulator with State-of-Charge Indicator



For values shown, Regulator shuts down when V_{in} < 5.5V and turns on again at 6.0V. Current drain in disconnected mode is ≈ 150μA.
*Sets disconnect Voltage
**Sets disconnect Hysteresis

Figure 59. Low Battery Disconnect

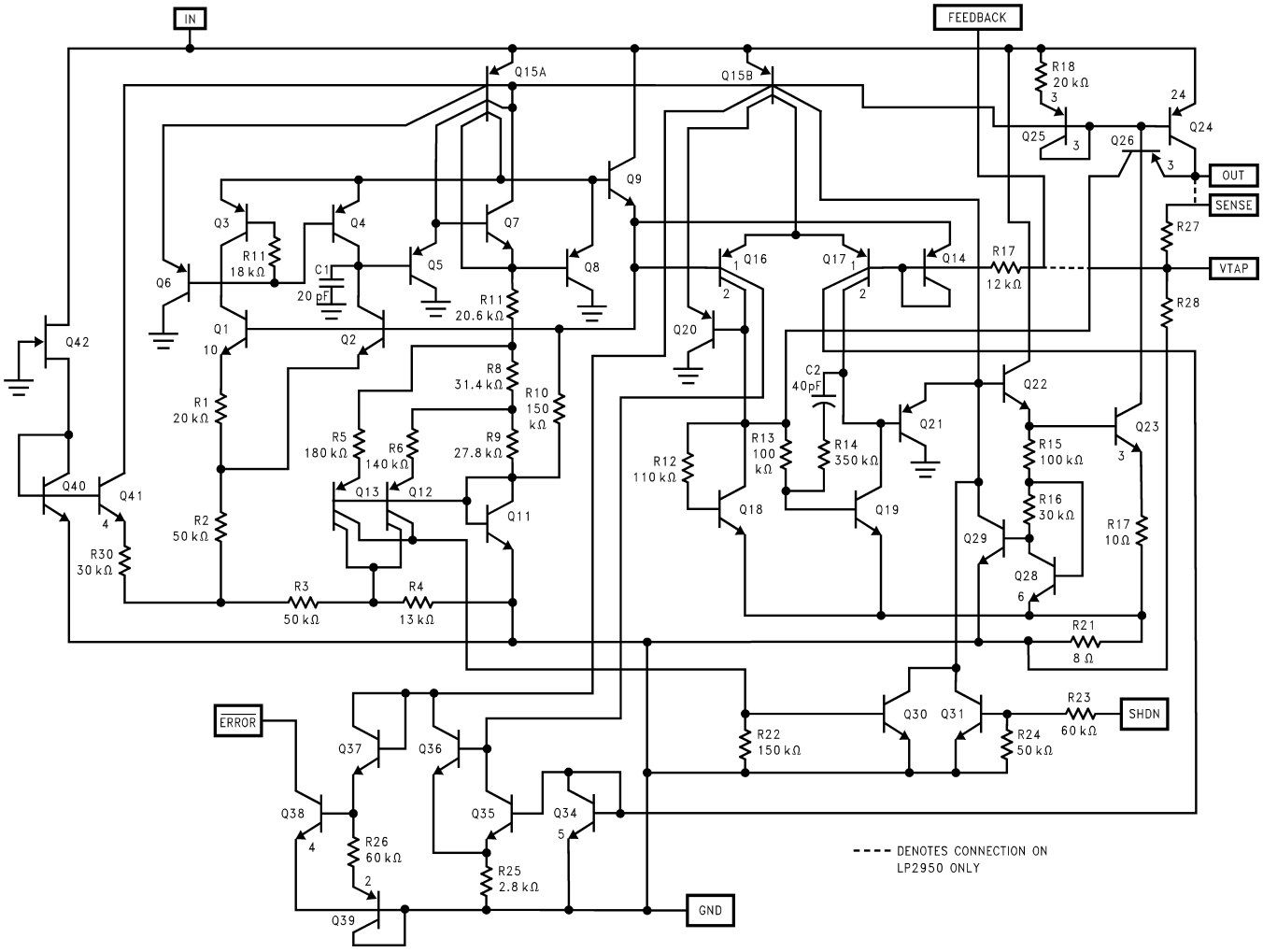


LM34 for 125°F Shutdown
LM35 for 125°C Shutdown

Figure 60. System Overtemperature Protection Circuit

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Schematic Diagram



REVISION HISTORY

Changes from Revision M (April 2013) to Revision N	Page
• Changed layout of National Data Sheet to TI format	23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2950ACZ-3.0/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950A CZ3.0	Samples
LP2950ACZ-3.3/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950A CZ3.3	Samples
LP2950ACZ-5.0/LFT1	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN | CU SN	N / A for Pkg Type		2950A CZ5.0	Samples
LP2950ACZ-5.0/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN | CU SN	N / A for Pkg Type		2950A CZ5.0	Samples
LP2950ACZ-5.0/LFT7	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU	N / A for Pkg Type		2950A CZ5.0	Samples
LP2950ACZ-5.0/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU	N / A for Pkg Type	-40 to 125	2950A CZ5.0	Samples
LP2950CDT-3.0	ACTIVE	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125		Samples
LP2950CDT-3.0/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-3.0	Samples
LP2950CDT-3.3	NRND	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125	LP2950 CDT-3.3	
LP2950CDT-3.3/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-3.3	Samples
LP2950CDT-5.0/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-5.0	Samples
LP2950CDTX-3.0	ACTIVE	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125		Samples
LP2950CDTX-3.0/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-3.0	Samples
LP2950CDTX-3.3	ACTIVE	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125		Samples
LP2950CDTX-3.3/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-3.3	Samples
LP2950CDTX-5.0	NRND	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125	LP2950 CDT-5.0	
LP2950CDTX-5.0/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-5.0	Samples
LP2950CN	LIFEBUY	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 125	LP	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										2951CN	
LP2950CZ-3.0/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN | CU SN	N / A for Pkg Type		2950 CZ3.0	Samples
LP2950CZ-3.0/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950 CZ3.0	Samples
LP2950CZ-3.3/LFT1	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN | CU SN	N / A for Pkg Type		2950 CZ3.3	Samples
LP2950CZ-3.3/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN | CU SN	N / A for Pkg Type		2950 CZ3.3	Samples
LP2950CZ-3.3/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950 CZ3.3	Samples
LP2950CZ-5.0/LFT1	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN | CU SN	N / A for Pkg Type		2950 CZ5.0	Samples
LP2950CZ-5.0/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN | CU SN	N / A for Pkg Type		2950 CZ5.0	Samples
LP2950CZ-5.0/LFT7	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU	N / A for Pkg Type		2950 CZ5.0	Samples
LP2950CZ-5.0/LFT8	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SN | CU SN	N / A for Pkg Type		2950 CZ5.0	Samples
LP2950CZ-5.0/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU	N / A for Pkg Type	-40 to 125	2950 CZ5.0	Samples
LP2951ACM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2951 ACM>D	
LP2951ACM-3.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951A CM30>D	Samples
LP2951ACM-3.3	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2951A CM33>D	
LP2951ACM-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2951A CM33>D	Samples
LP2951ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2951 ACM>D	Samples
LP2951ACMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L0DA	
LP2951ACMM-3.0	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L0BA	
LP2951ACMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0BA	Samples
LP2951ACMM-3.3	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L0CA	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2951ACMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CA	Samples
LP2951ACMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0DA	Samples
LP2951ACMMX-3.0	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	L0BA	
LP2951ACMMX-3.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0BA	Samples
LP2951ACMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CA	Samples
LP2951ACMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0DA	Samples
LP2951ACMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	2951 ACM>D	
LP2951ACMX-3.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951A CM30>D	Samples
LP2951ACMX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2951A CM33>D	Samples
LP2951ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2951 ACM>D	Samples
LP2951ACN	LIFEBUY	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 125	LP 2951ACN	
LP2951ACN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP 2951ACN	Samples
LP2951ACSD	NRND	WSON	NGT	8	1000	TBD	Call TI	Call TI	-40 to 125	2951AC	
LP2951ACSD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951AC	Samples
LP2951ACSDX-3.3/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	51AC33	Samples
LP2951ACSDX/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951AC	Samples
LP2951CM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2951 CM>D	
LP2951CM-3.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951C M30>D	Samples
LP2951CM-3.3	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2951C M33>D	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2951CM-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2951C M33>D	Samples
LP2951CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2951 CM>D	Samples
LP2951CMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L0DB	
LP2951CMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0BB	Samples
LP2951CMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CB	Samples
LP2951CMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0DB	Samples
LP2951CMMX	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	L0DB	
LP2951CMMX-3.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0BB	Samples
LP2951CMMX-3.3	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	L0CB	
LP2951CMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CB	Samples
LP2951CMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0DB	Samples
LP2951CMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	2951 CM>D	
LP2951CMX-3.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951C M30>D	Samples
LP2951CMX-3.3	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	2951C M33>D	
LP2951CMX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2951C M33>D	Samples
LP2951CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	2951 CM>D	Samples
LP2951CN	LIFEBUY	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 125	LP 2951CN	
LP2951CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP 2951CN	Samples
LP2951CSD-3.0/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	51AC30B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2951CSD-3.3/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	51AC33B	Samples
LP2951CSD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951ACB	Samples
LP2951CSDX-3.0/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	51AC30B	Samples
LP2951CSDX-3.3/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	51AC33B	Samples
LP2951CSDX/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951ACB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

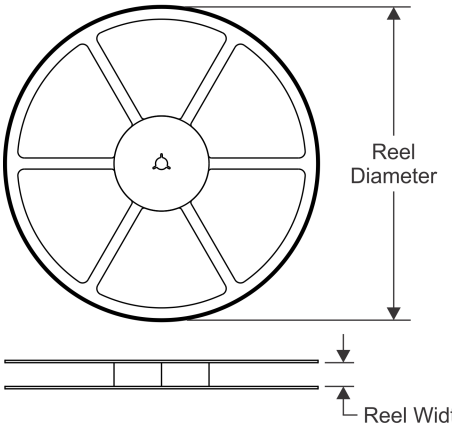
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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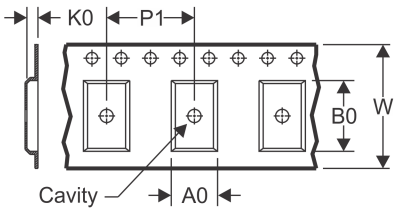
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

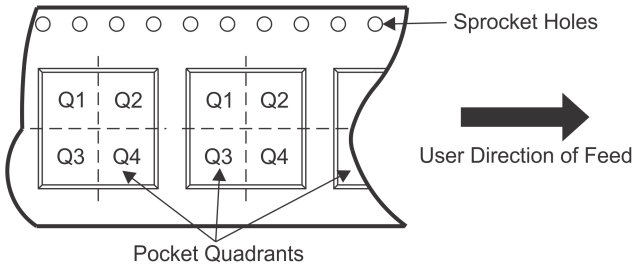


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

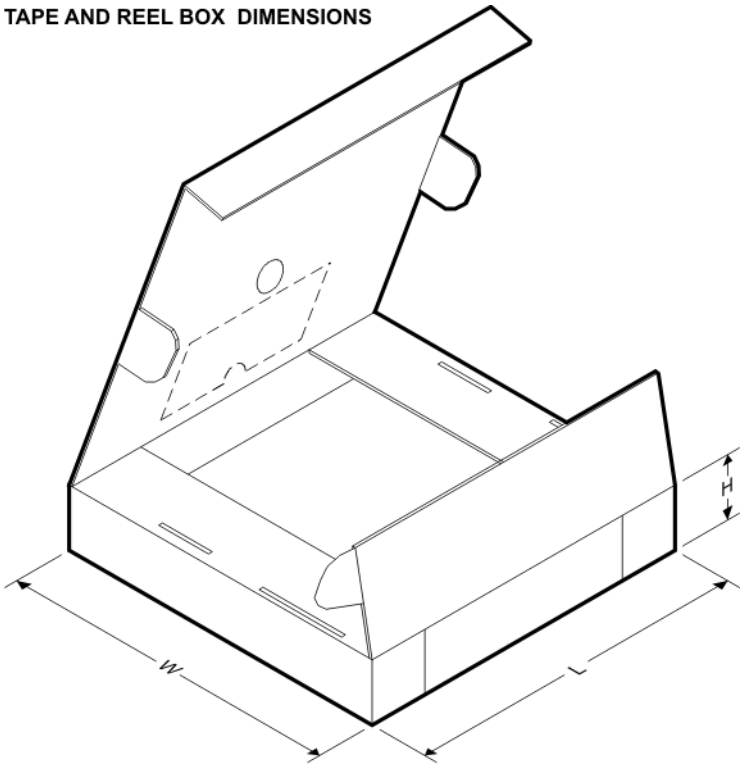


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2950CDTX-3.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP2950CDTX-3.3/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP2950CDTX-5.0	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP2950CDTX-5.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP2951ACMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM-3.0	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM-3.3	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMMX-3.0	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMMX-3.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951ACMX-3.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951ACMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2951ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951ACSD	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2951ACSDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2951CMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMMX-3.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMMX-3.3	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951CMX-3.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951CMX-3.3	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951CMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951CSD-3.3/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2951CSDX-3.0/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2951CSDX-3.3/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

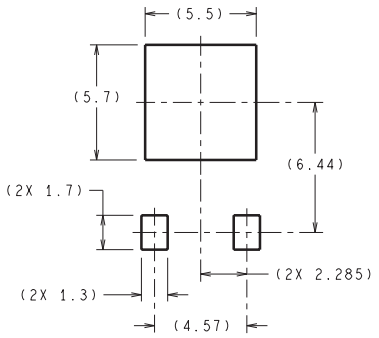
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

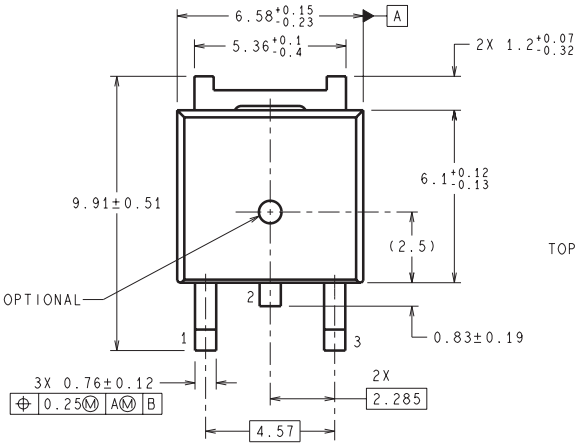
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2950CDTX-3.0/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP2950CDTX-3.3/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP2950CDTX-5.0	TO-252	NDP	3	2500	367.0	367.0	35.0
LP2950CDTX-5.0/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP2951ACMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM-3.0	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM-3.3	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMMX-3.0	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951ACMMX-3.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951ACMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951ACMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951ACMX	SOIC	D	8	2500	367.0	367.0	35.0
LP2951ACMX-3.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951ACMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951ACSD	WSON	NGT	8	1000	210.0	185.0	35.0
LP2951ACSDX/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LP2951CMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951CMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951CMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951CMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951CMMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951CMMX-3.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951CMMX-3.3	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951CMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951CMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951CMX	SOIC	D	8	2500	367.0	367.0	35.0
LP2951CMX-3.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951CMX-3.3	SOIC	D	8	2500	367.0	367.0	35.0
LP2951CMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951CSD-3.3/NOPB	WSON	NGT	8	1000	210.0	185.0	35.0
LP2951CSDX-3.0/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LP2951CSDX-3.3/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0

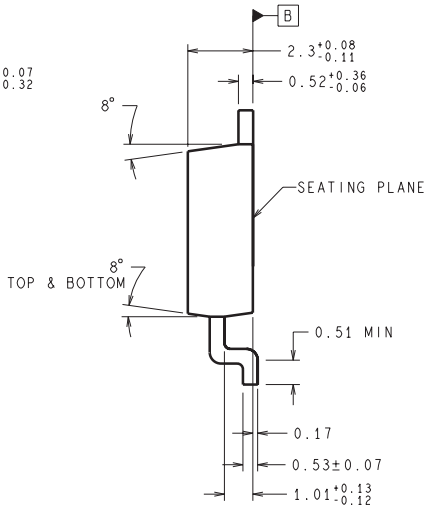
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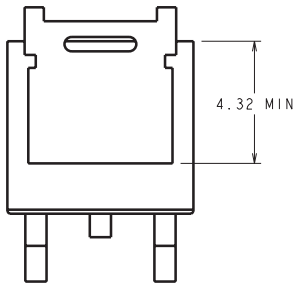


LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

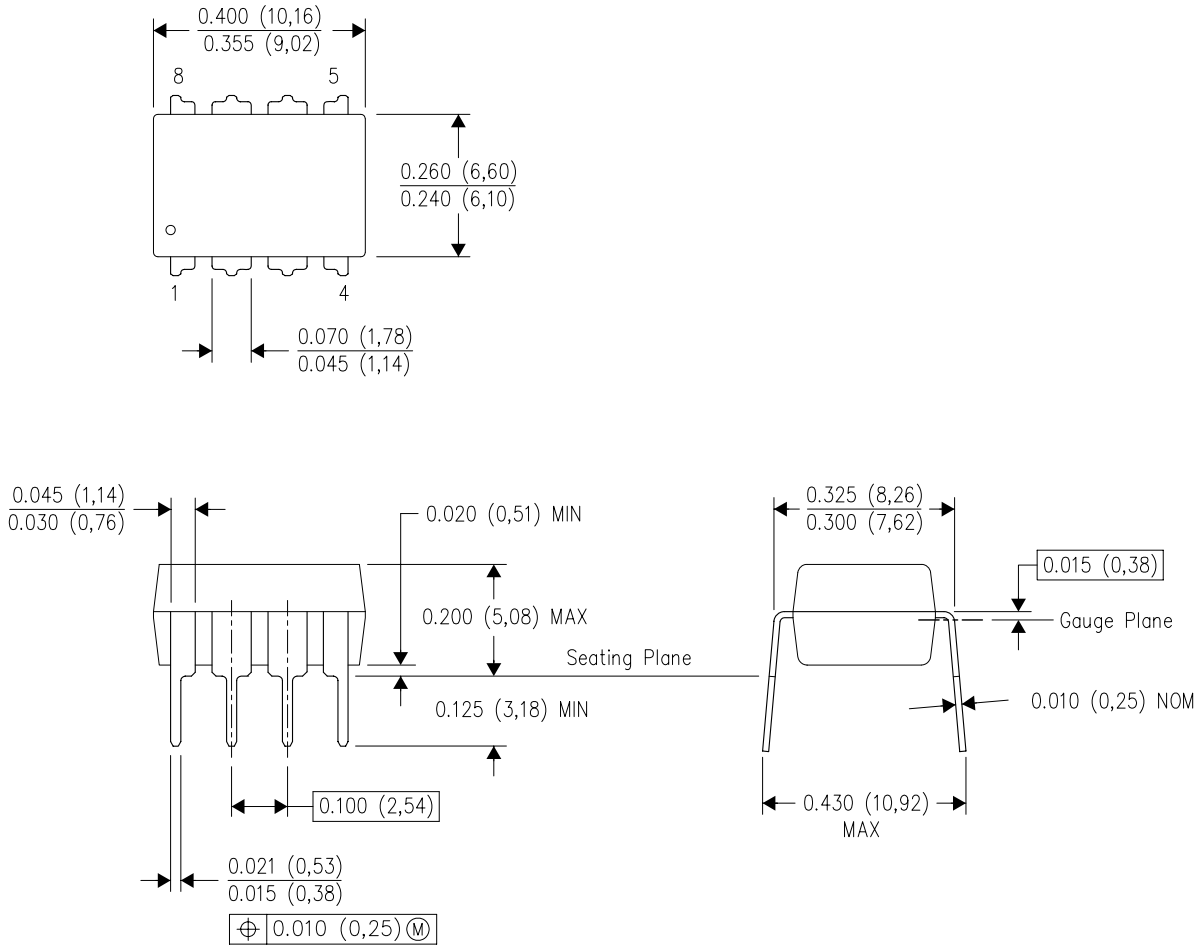






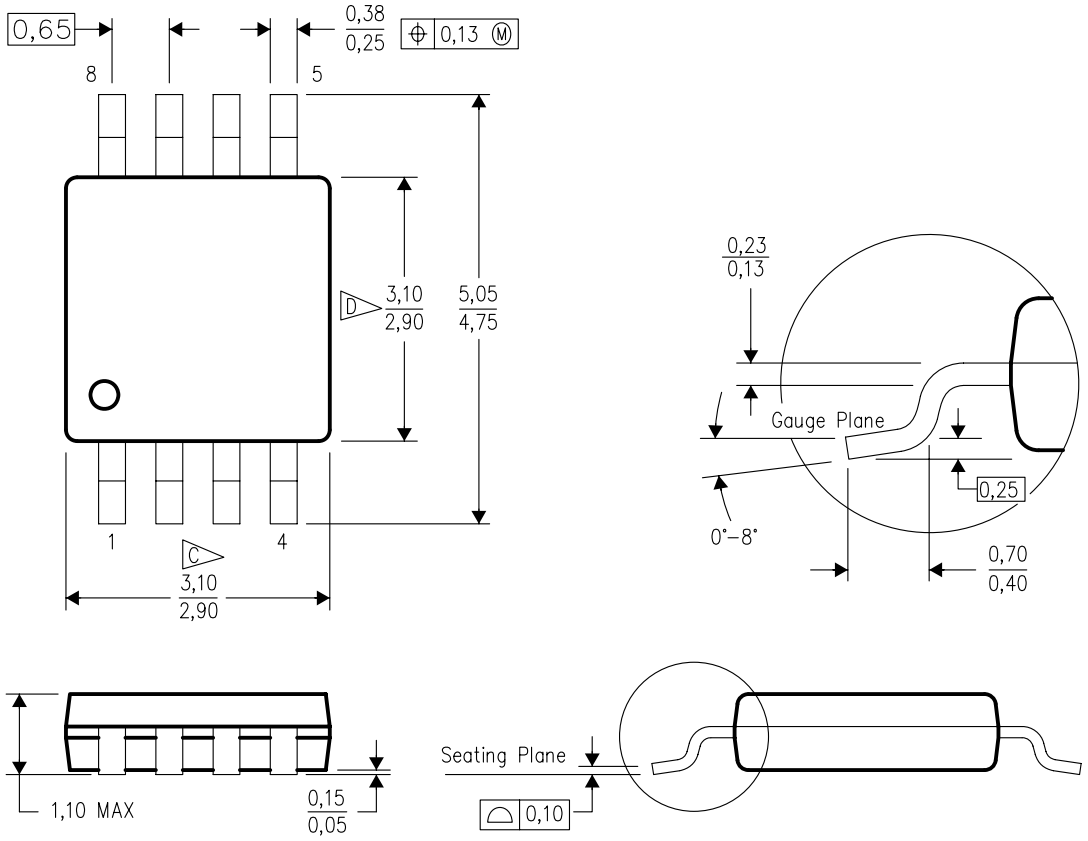
TD03B (Rev F)

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

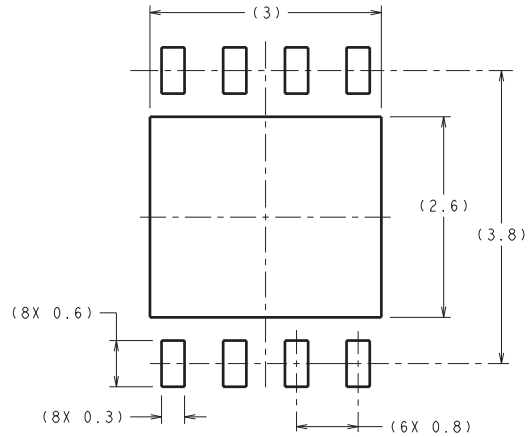
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



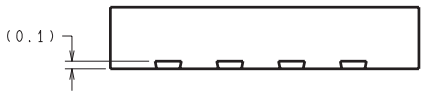
4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

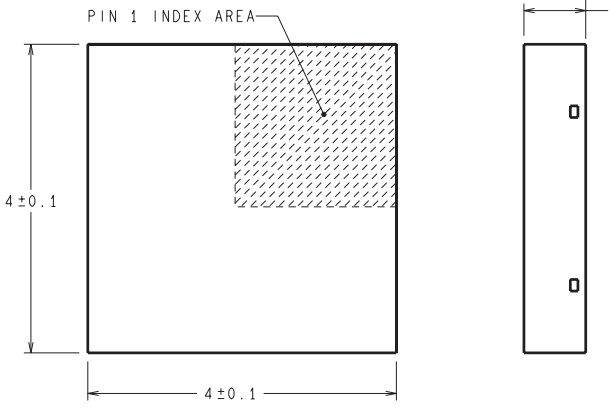
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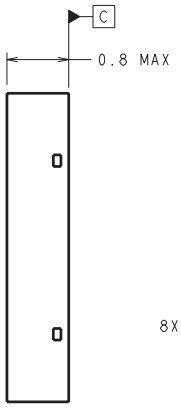


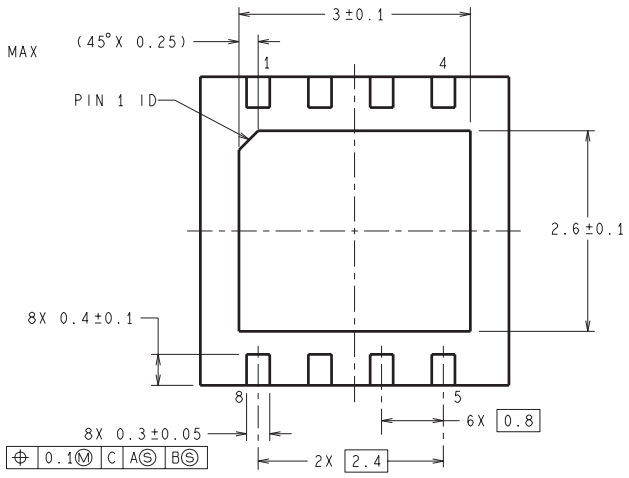
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DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN

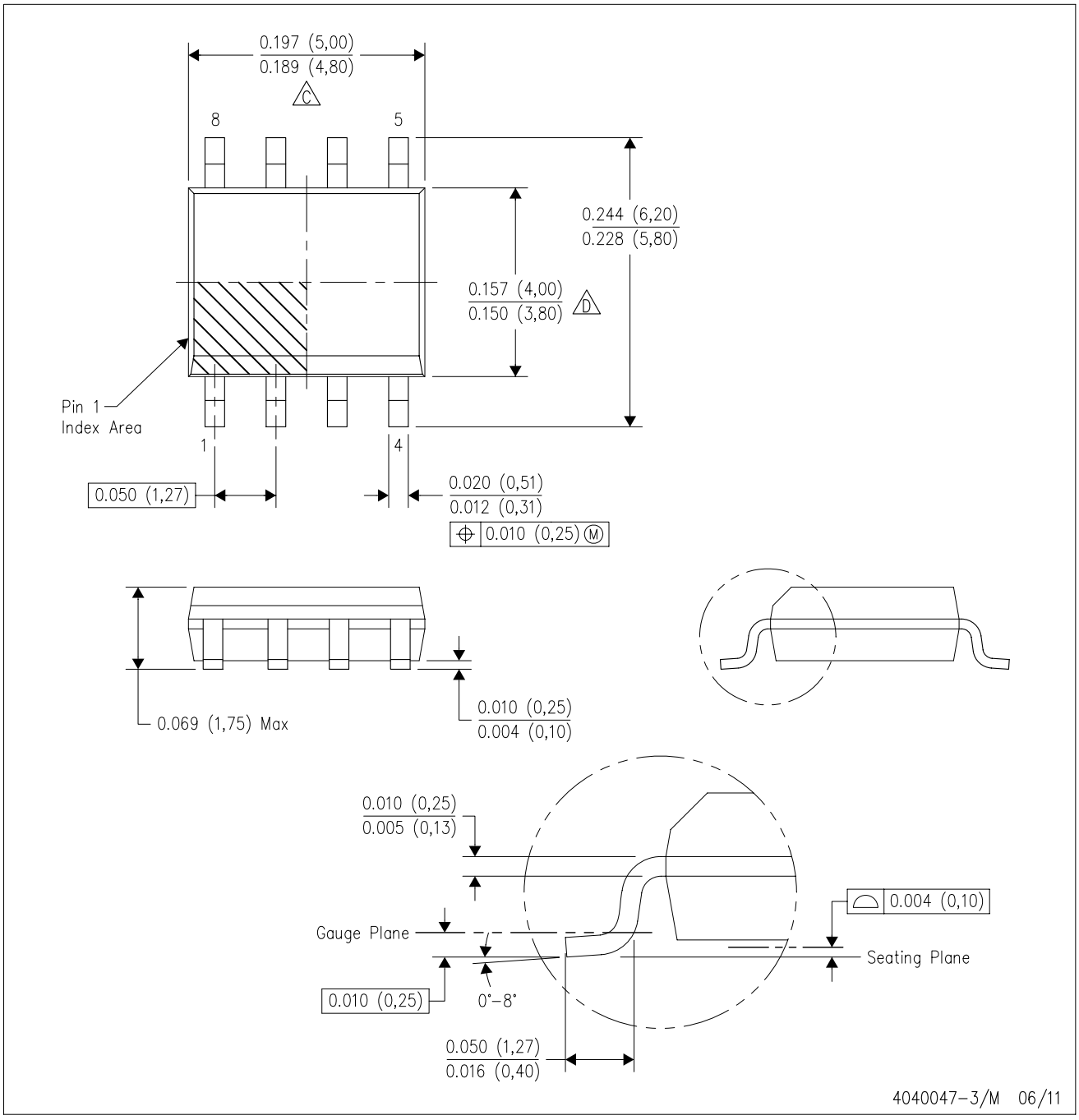






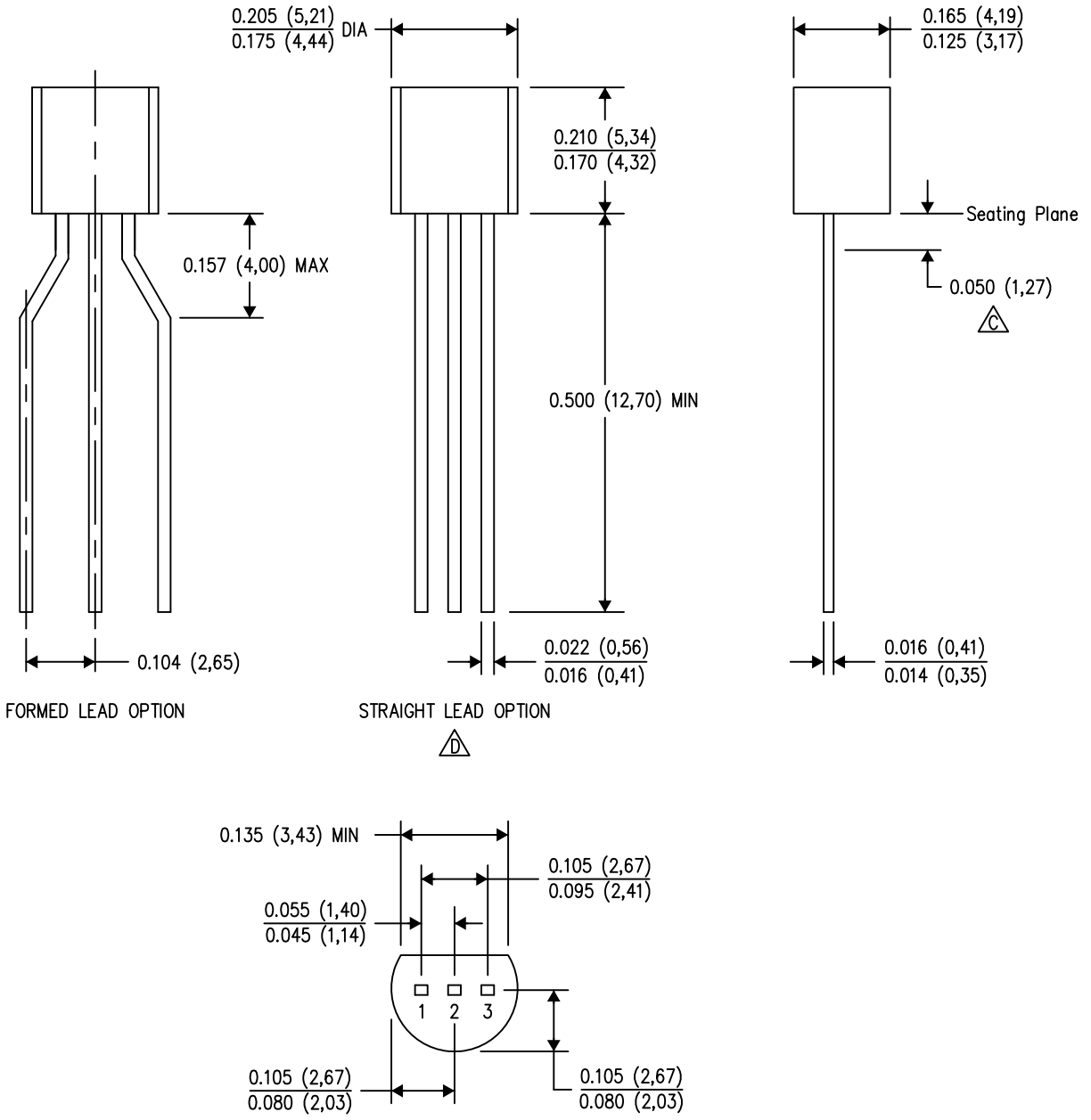
SDC08A (Rev A)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



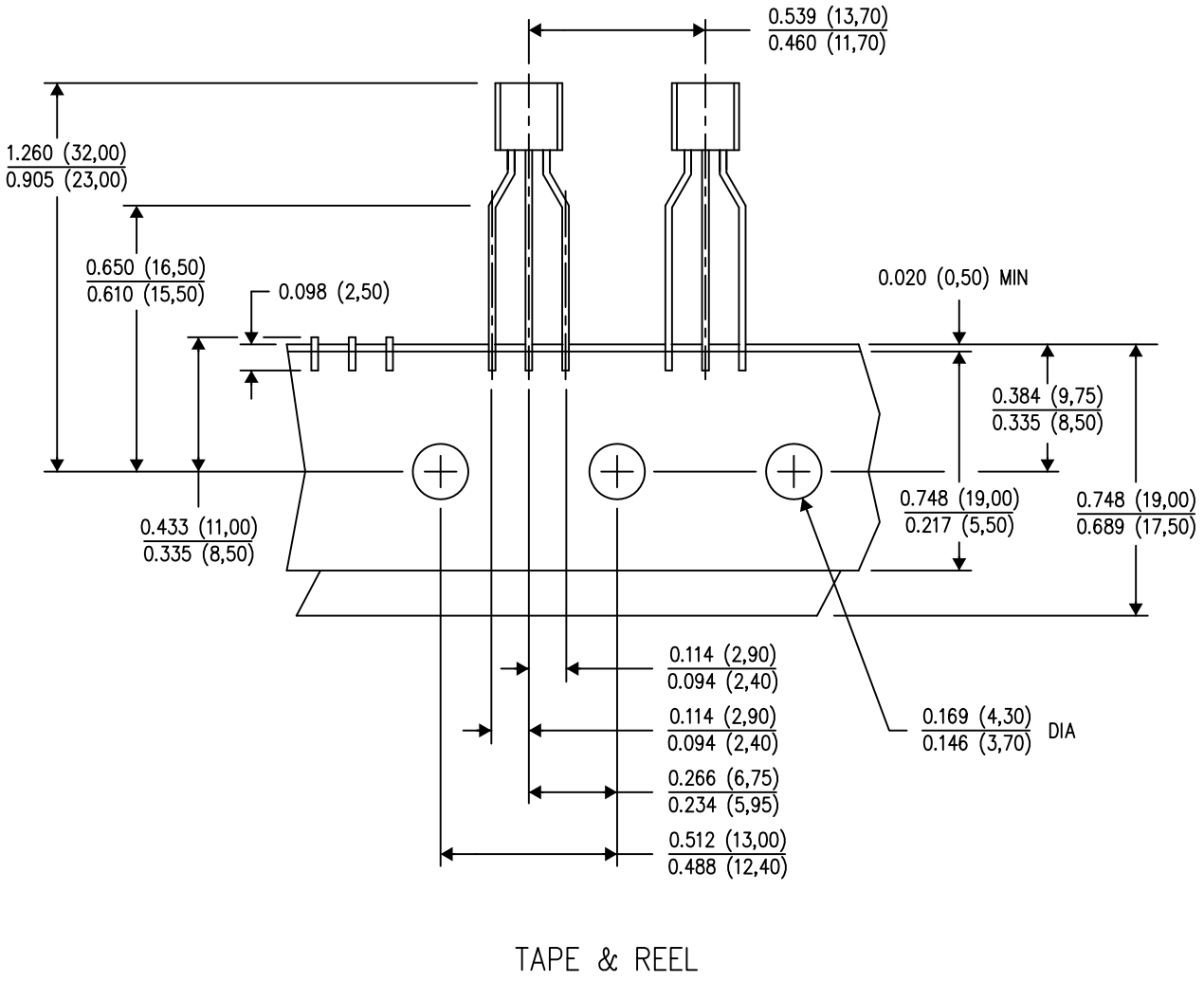
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

LP (O–PBCY–W3) PLASTIC CYLINDRICAL PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. Falls within JEDEC TO–226 Variation AA (TO–226 replaces TO–92).
E. Shipping Method:
Straight lead option available in bulk pack only.
Formed lead option available in tape & reel or ammo pack.
Specific products can be offered in limited combinations of shipping mediums and lead options.
Consult product folder for more information on available options.

LP (O–PBCY–W3) PLASTIC CYLINDRICAL PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Formed Lead Option package.

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