High Accuracy Ultralow I_Q, 200 mA, SOT-23, anyCAP™ Low Dropout Regulator

ADP3330

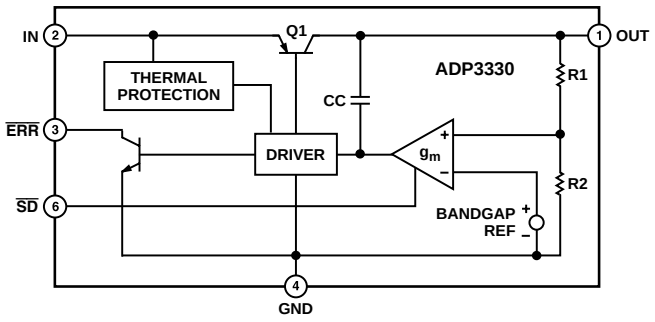
FEATURES

High Accuracy Over Line and Load: ±0.7% @ +25°C, ±1.4% Over Temperature
Ultralow Dropout Voltage: 140 mV (Typ) @ 200 mA
Requires Only C_O = 0.47 μF for Stability
anyCAP = Stable with Any Type of Capacitor (Including MLCC)
Current and Thermal Limiting
Low Noise
Low Shutdown Current: <2 μA
2.9 V to 12 V Supply Range
–40°C to +85°C Ambient Temperature Range
Ultrasmall Thermally Enhanced Chip-on-Lead™ SOT-23-6 6-Lead Package

APPLICATIONS

Cellular Telephones
Notebook, Palmtop Computers
Battery Powered Systems
PCMCIA Regulator
Bar Code Scanners
Camcorders, Cameras

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3330 is a member of the ADP330x family of precision low dropout anyCAP voltage regulators. The ADP3330 operates with an input voltage range of 2.9 V to 12 V and delivers a load current up to 200 mA. The ADP3330 stands out from the conventional LDOs with a novel architecture and an enhanced process that enables it to offer performance advantages and higher output current than its competition. Its patented design requires only a 0.47 μF output capacitor for stability. This device is insensitive to output capacitor Equivalent Series Resistance (ESR), and is stable with any good quality capacitor, including ceramic (MLCC) types for space-restricted applications. The ADP3330 achieves exceptional accuracy of ±0.7% at room temperature and ±1.4% over temperature, line and load variations. The dropout voltage of the ADP3330 is only 140 mV (typical) at 200 mA. This device also includes a safety current limit, thermal overload protection and a shutdown feature. In shutdown mode, the ground current is reduced to less than 2 μA. The ADP3330 has ultralow quiescent current 34 μA (typ) in light load situations.

The SOT-23-6 package has been thermally enhanced using Analog Devices' proprietary Chip-on-Lead feature to maximize power dissipation.

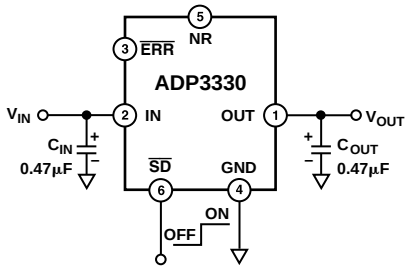


Figure 1. Typical Application Circuit

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REV. A

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ADP3330-xx–SPECIFICATIONS (@ T_A = –40°C to +85°C, V_{IN} = +7 V, C_{IN} = 0.47 µF, C_{OUT} = 0.47 µF, unless otherwise noted).[1, 2] The following specifications apply to all voltage options except –2.5.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE ACCURACY	V_{OUT}	V_{IN} = V_{OUTNOM} +0.25 V to +12 V I_L = 0.1 mA to 200 mA T_A = +25°C	–0.7		+0.7	%
		V_{IN} = V_{OUTNOM} +0.25 V to +12 V I_L = 0.1 mA to 150 mA T_A = –40°C to +85°C	–1.4		+1.4	%
		V_{IN} = V_{OUTNOM} +0.25 V to +12 V I_L = 0.1 mA to 200 mA T_A = –20°C to +85°C	–1.4		+1.4	%
LINE REGULATION	$\frac{\Delta V_O}{\Delta V_{IN}}$	V_{IN} = V_{OUTNOM} +0.25 V to +12 V T_A = +25°C		0.04		mV/V
LOAD REGULATION	$\frac{\Delta V_O}{\Delta I_L}$	I_L = 0.1 mA to 200 mA T_A = +25°C		0.04		mV/mA
GROUND CURRENT	I_{GND}	I_L = 200 mA, T_A = –20°C to +85°C		1.6	4.0	mA
		I_L = 150 mA		1.2	3.1	mA
		I_L = 50 mA		0.4	1.1	mA
		I_L = 0.1 mA		34	50	µA
GROUND CURRENT IN DROPOUT	I_{GND}	V_{IN} = V_{OUTNOM} – 100 mV I_L = 0.1 mA		37	55	µA
DROPOUT VOLTAGE	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 200 mA, T_A = –20°C to +85°C		0.14	0.23	V
		I_L = 150 mA		0.11	0.17	V
		I_L = 10 mA		0.042	0.06	V
		I_L = 1 mA		0.025	0.05[2]	V
PEAK LOAD CURRENT	I_{LDPK}	V_{IN} = V_{OUTNOM} + 1 V		300		mA
OUTPUT NOISE[3]	V_{NOISE}	f = 10 Hz–100 kHz, C_L = 10 µF I_L = 200 mA, C_{NR} = 10 nF, V_{OUT} = 3 V		47		µV rms
		f = 10 Hz–100 kHz, C_L = 10 µF I_L = 200 mA, C_{NR} = 0 nF, V_{OUT} = 3 V		95		µV rms
SHUTDOWN THRESHOLD	V_{THSD}	ON	2.0			V
		OFF			0.4	V
SHUTDOWN PIN INPUT CURRENT	I_{SD}	V_{IN} = 12 V, 0 < $\overline{SD}$, ≤ 12 V		1.9	9	µA
		0 < $\overline{SD}$, ≤ 5 V		1.4	6	µA
GROUND CURRENT IN SHUTDOWN MODE	I_{GNDSD}	$\overline{SD}$ = 0 V, V_{IN} = 12 V		0.01	2	µA
OUTPUT CURRENT IN SHUTDOWN MODE	I_{OSD}	T_A = +25°C @ V_{IN} = 12 V			1	µA
		T_A = +85°C @ V_{IN} = 12 V			2	µA
ERROR PIN OUTPUT LEAKAGE	I_{EL}	V_{EO} = 5 V			1	µA
ERROR PIN OUTPUT "LOW" VOLTAGE	V_{EOL}	I_{SINK} = 400 µA		0.19	0.40	V

NOTES

[1]Ambient temperature of +85°C corresponds to a junction temperature of +125°C under typical full load test conditions.

[2]Application stable with no load.

[3]See detail in Figure 19 and Application section of data sheet.

Specifications subject to change without notice.

ADP3330-2.5–SPECIFICATIONS (@ T_A = –40°C to +85°C, V_{IN} = +7 V ,C_{IN} = 0.47 µF, C_{OUT} = 0.47 µF, unless otherwise noted).[1, 2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE ACCURACY	V_{OUT}	V_{IN} = +2.9 V to +12 V I_L = 0.1 mA to 200 mA T_A = +25°C	–0.7		+0.7	%
		V_{IN} = +2.9 V to +12 V I_L = 0.1 mA to 150 mA T_A = –40°C to +85°C	–1.4		+1.4	%
		V_{IN} = +2.9 V to +12 V I_L = 0.1 mA to 200 mA T_A = –20°C to +85°C	–1.4		+1.4	%
LINE REGULATION	$\frac{\Delta V_O}{\Delta V_{IN}}$	V_{IN} = +2.9 V to +12 V T_A = +25°C		0.04		mV/V
LOAD REGULATION	$\frac{\Delta V_O}{\Delta I_L}$	I_L = 0.1 mA to 200 mA T_A = +25°C		0.04		mV/mA
GROUND CURRENT	I_{GND}	I_L = 200 mA, T_A = –20°C to +85°C		1.6	4.0	mA
		I_L = 150 mA		1.2	3.1	mA
		I_L = 50 mA		0.4	1.1	mA
		I_L = 0.1 mA		34	50	µA
GROUND CURRENT IN DROPOUT	I_{GND}	V_{IN} = V_{OUTNOM} – 100 mV I_L = 0.1 mA		37	55	µA
DROPOUT VOLTAGE	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 200 mA, T_A = –20°C to +85°C		0.14	0.4	V
		I_L = 150 mA		0.11	0.3	V
		I_L = 10 mA		0.042	0.06	V
		I_L = 1 mA		0.025	0.05[2]	V
PEAK LOAD CURRENT	I_{LDPK}	V_{IN} = V_{OUTNOM} + 1 V		300		mA
OUTPUT NOISE[3]	V_{NOISE}	f = 10 Hz–100 kHz, C_L = 10 µF I_L = 200 mA, C_{NR} = 10 nF, V_{OUT} = 3 V		47		µV rms
		f = 10 Hz–100 kHz, C_L = 10 µF I_L = 200 mA, C_{NR} = 0 nF, V_{OUT} = 3 V		95		µV rms
SHUTDOWN THRESHOLD	V_{THSD}	ON	2.0			V
		OFF			0.4	V
SHUTDOWN PIN INPUT CURRENT	I_{SD}	V_{IN} = 12 V, 0 < $\overline{SD}$, ≤ 12 V		1.9	9	µA
		0 < $\overline{SD}$, ≤ 5 V		1.4	6	µA
GROUND CURRENT IN SHUTDOWN MODE	I_{GNDSD}	$\overline{SD}$ = 0 V, V_{IN} = 12 V		0.01	2	µA
OUTPUT CURRENT IN SHUTDOWN MODE	I_{OSD}	T_A = +25°C @ V_{IN} = 12 V			1	µA
		T_A = +85°C @ V_{IN} = 12 V			2	µA
ERROR PIN OUTPUT LEAKAGE	I_{EL}	V_{EO} = 5 V			1	µA
ERROR PIN OUTPUT "LOW" VOLTAGE	V_{EOL}	I_{SINK} = 400 µA		0.19	0.40	V

NOTES
[1]Ambient temperature of +85°C corresponds to a junction temperature of +125°C under typical full load test conditions.
[2]Application stable with no load.
[3]See detail in Figure 19 and Application section of data sheet.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage . . . . . –0.3 V to +16 V
Shutdown Input Voltage . . . . . –0.3 V to +16 V
Power Dissipation . . . . . Internally Limited
Operating Ambient Temperature Range . . . . . –40°C to +85°C
Operating Junction Temperature Range . . . . –40°C to +125°C
θ_{JA} (4-Layer Board) . . . . . +165°C/W
θ_{JA} (2-Layer Board) . . . . . +190°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

ORDERING GUIDE

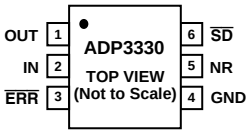
Model	Voltage Output	Package Option*	Marking Code
ADP3330ART-2.5	2.5 V	RT-6 (SOT-23-6)	L1B
ADP3330ART-2.75	2.75 V	RT-6 (SOT-23-6)	L2B
ADP3330ART-2.85	2.85 V	RT-6 (SOT-23-6)	L3B
ADP3330ART-3	3.0 V	RT-6 (SOT-23-6)	L4B
ADP3330ART-3.3	3.3 V	RT-6 (SOT-23-6)	L5B
ADP3330ART-3.6	3.6 V	RT-6 (SOT-23-6)	L6B
ADP3330ART-5	5.0 V	RT-6 (SOT-23-6)	L8B

*Contact the factory for the availability of other output voltage options.

PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1	OUT	Output of the Regulator. Bypass to ground with a 0.47 μF or larger capacitor.
2	IN	Regulator Input.
3	$\overline{\text{ERR}}$	Open Collector Output that goes low to indicate that the output is about to go out of regulation.
4	GND	Ground Pin.
5	NR	Noise Reduction Pin. Used for further reduction of output noise (see text for detail). No connection if not used.
6	$\overline{\text{SD}}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin should be connected to the input pin.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3330 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



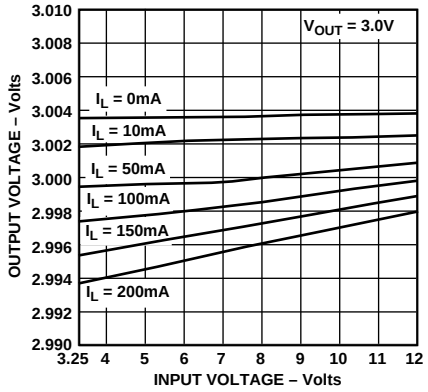


Figure 2. Line Regulation Output Voltage vs. Supply Voltage

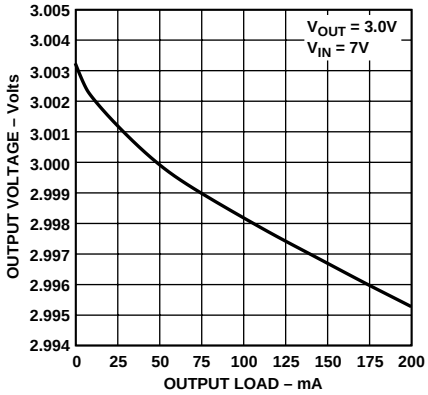


Figure 3. Output Voltage vs. Load Current

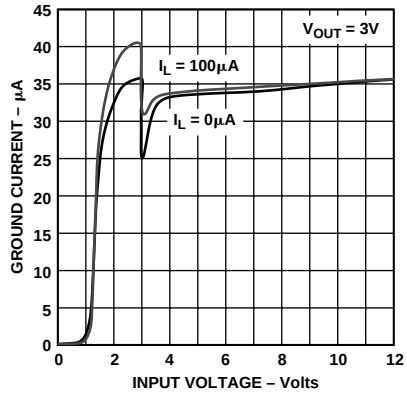


Figure 4. Ground Current vs. Supply Voltage

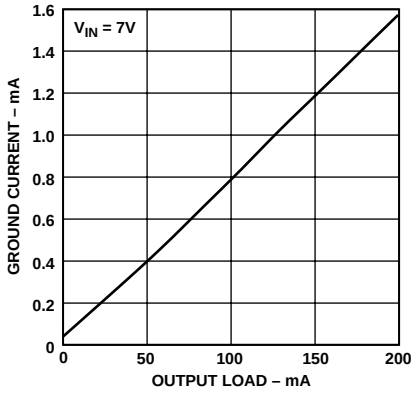


Figure 5. Ground Current vs. Load Current

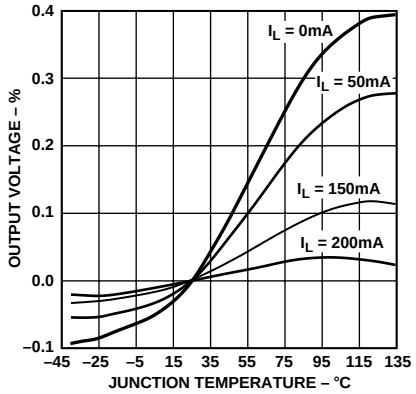


Figure 6. Output Voltage Variation % vs. Junction Temperature

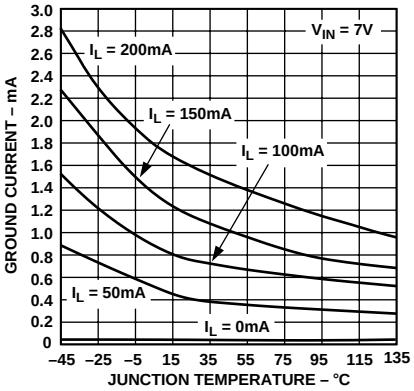


Figure 7. Ground Current vs. Junction Temperature

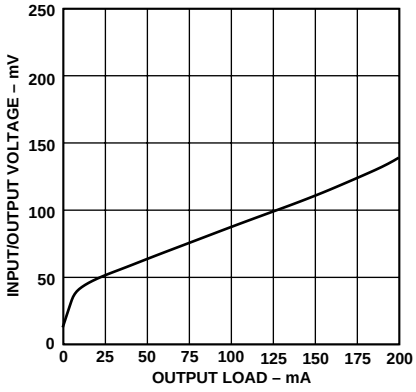


Figure 8. Dropout Voltage vs. Output Current

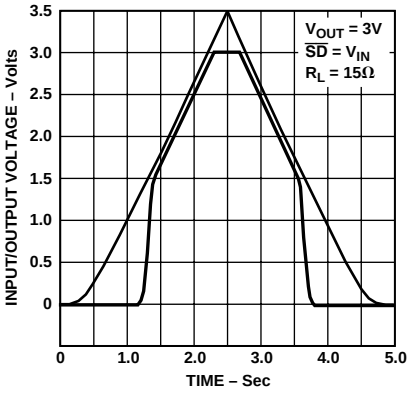


Figure 9. Power-Up/Power-Down

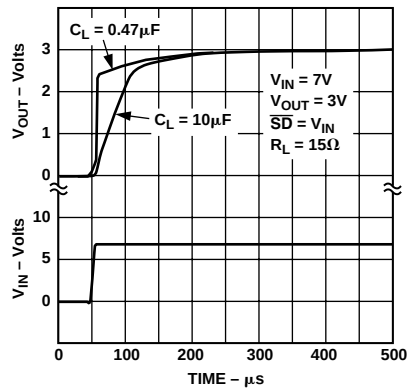


Figure 10. Power-Up Response

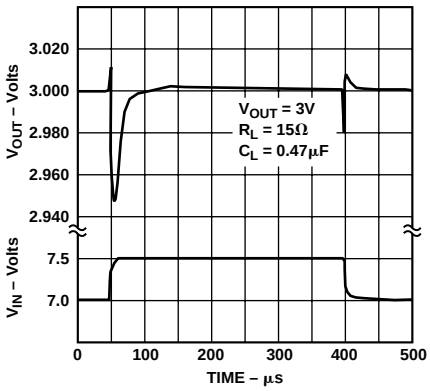


Figure 11. Line Transient Response

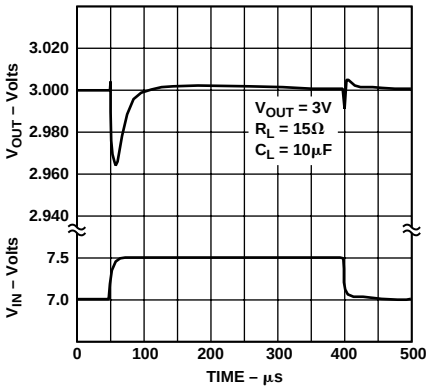


Figure 12. Line Transient Response

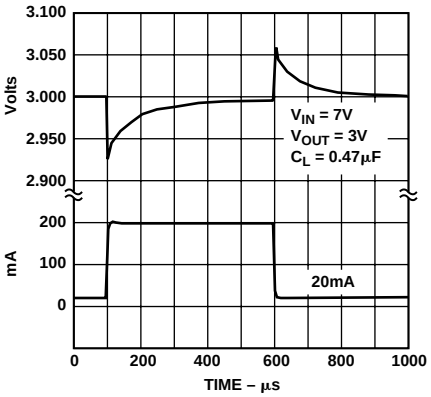


Figure 13. Load Transient Response

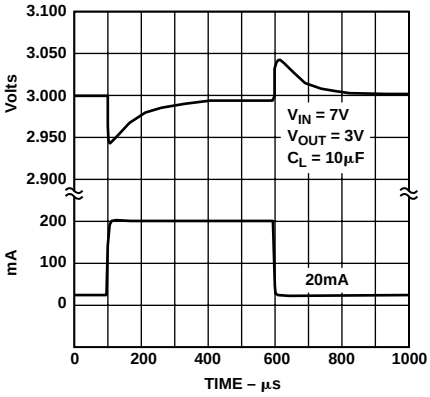


Figure 14. Load Transient Response

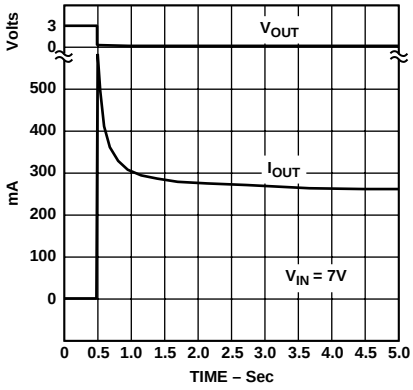


Figure 15. Short Circuit Current

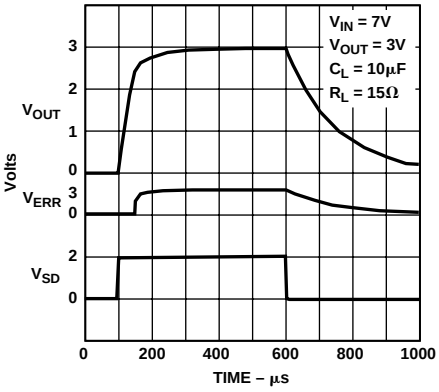


Figure 16. Turn On–Turn Off Response

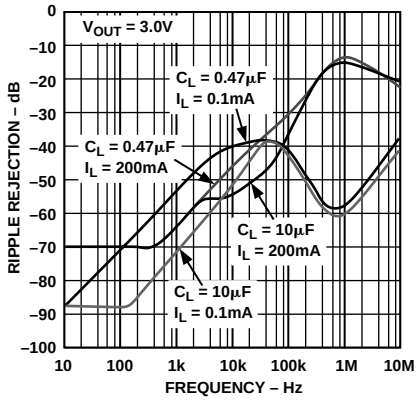


Figure 17. Power Supply Ripple Rejection

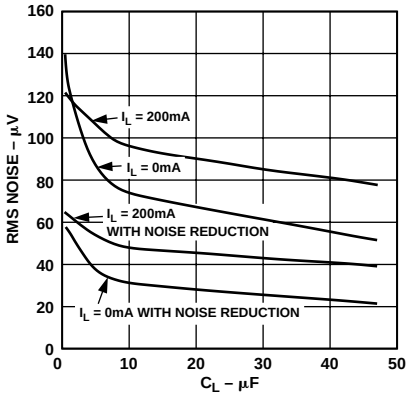


Figure 18. RMS Noise vs. C_L (10 Hz–100 kHz)

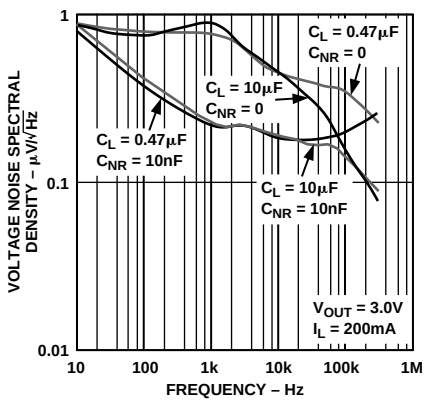


Figure 19. Output Noise Density

THEORY OF OPERATION

The new anyCAP LDO ADP3330 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2 which is varied to provide the available output voltage options. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

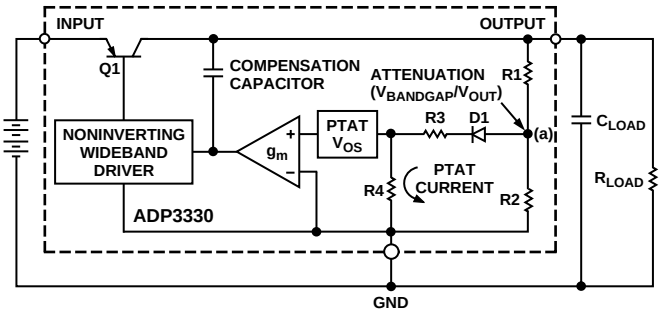


Figure 20. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that at equilibrium it produces a large, temperature-proportional input "offset voltage" that is repeatable and very well controlled. The temperature-proportional offset voltage is combined with the complementary diode voltage to form a "virtual bandgap" voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the tradeoff of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the bandgap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1, and a second divider consisting of R3 and R4, the values are chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider so that the error resulting from base current loading in conventional circuits is avoided.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type and ESR of the load capacitance.

Most LDOs place strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3330 anyCAP LDO, this is no longer true. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. The innovative design allows the circuit to be stable with just a small 0.47 µF capacitor on the output. Additional advantages of the pole splitting scheme include superior line noise rejection and very high regulator gain which leads to excellent line and load regulation. An impressive ±1.4% accuracy is guaranteed over line, load and temperature.

Additional features of the circuit include current limit, thermal shutdown and noise reduction. Compared to standard solutions that give warning after the output has lost regulation, the ADP3330 provides improved system performance by enabling the $\overline{\text{ERR}}$ pin to give warning just before the device loses regulation.

As the chip's temperature rises above +165°C, the circuit activates a soft thermal shutdown, indicated by a signal low on the $\overline{\text{ERR}}$ pin, to reduce the current to a safe level.

APPLICATION INFORMATION

Capacitor Selection

Output Capacitors: as with any micropower device, output transient response is a function of the output capacitance. The ADP3330 is stable with a wide range of capacitor values, types and ESR (anyCAP). A capacitor as low as 0.47 µF is all that is needed for stability; larger capacitors can be used if high output current surges are anticipated. The ADP3330 is stable with extremely low ESR capacitors (ESR ≈ 0), such as Multilayer Ceramic Capacitors (MLCC) or OSCON. Note that the effective capacitance of some capacitor types may fall below the minimum at cold temperature. Ensure that the capacitor provides more than 0.47 µF at minimum temperature.

Input Bypass Capacitor: an input bypass capacitor is not strictly required but it is advisable in any application involving long input wires or high source impedance. Connecting a 0.47 µF capacitor from IN to ground reduces the circuit's sensitivity to PC board layout. If a larger value output capacitor is used, then a larger value input capacitor is also recommended.

Noise Reduction

A noise reduction capacitor (C_{NR}) can be used to further reduce the noise by 6 dB–10 dB (Figure 21). Low leakage capacitors in 10 pF–500 pF range provide the best performance. Since the noise reduction pin (NR) is internally connected to a high impedance node, any connection to this node should be carefully done to avoid noise pickup from external sources. The pad connected to this pin should be as small as possible and long PC board traces are not recommended.

When adding a noise reduction capacitor, use the following guidelines:

- Maintain a minimum load current of 1 mA when not in shutdown.
- For CNR values greater than 500 pF, add a 100 kΩ series resistor (RNR).

It is important to note that as CNR increases, the turn-on time will be delayed. With CNR values greater than 1 nF, this delay may be on the order of several milliseconds.

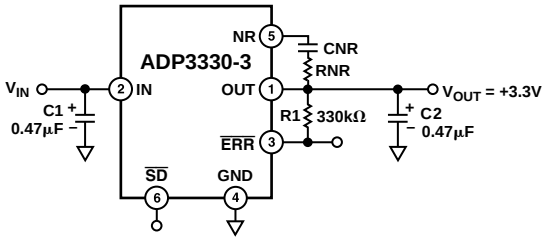
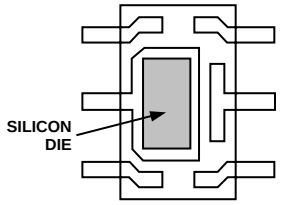


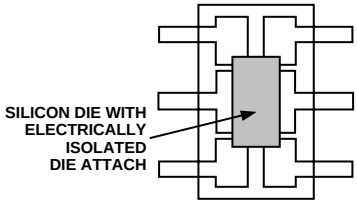
Figure 21. Noise Reduction Circuit

Chip-on-Lead Package

The ADP3330 uses a patented Chip-on-Lead package design to ensure the best thermal performance in an SOT-23 footprint. In a standard SOT-23, the majority of the heat flows out of the ground pin. This new package uses an electrically isolated die attach that allows all pins to contribute to heat conduction. This technique reduces the thermal resistance to 190°C/W on a 2-layer board as compared to >230°C/W for a standard SOT-23 leadframe. Figure 22 shows the difference between the standard SOT-23 and the Chip-on-Lead leadframes.



a. Normal SOT-23-6 Package



b. Thermally Enhanced Chip-on-Lead Package

Figure 22.

Thermal Overload Protection

The ADP3330 is protected against damage due to excessive power dissipation by its thermal overload protection circuit which limits the die temperature to a maximum of +165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where die temperature starts to rise above +165°C, the output current is reduced until the die temperature has dropped to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Calculating Junction Temperature

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT})\, I_{LOAD} + (V_{IN})\, I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, V_{IN} and V_{OUT} are input and output voltages respectively.

Assuming I_{LOAD} = 200 mA, I_{GND} = 4 mA, V_{IN} = 4.2 V and V_{OUT} = 3.0 V, device power dissipation is:

$$P_D = (4.2 - 3)\ 200\ mA + 4.2\ (4\ mA) = 257\ mW$$

The proprietary package used in the ADP3330 has a thermal resistance of 165°C/W, significantly lower than a standard 6-lead SOT-23 package. Assuming a 4-layer board, the junction temperature rise above ambient temperature will be approximately equal to:

$$\Delta T_{JA} = 0.257\ W \times 165\,°C/W = 42.4\,°C$$

To limit the maximum junction temperature to +125°C, maximum allowable ambient temperature will be:

$$T_{A\,MAX} = 125\,°C - 42.4\,°C = 82.6\,°C$$

Printed Circuit Board Layout Considerations
All surface mount packages rely on the traces of the PC board to conduct heat away from the package.

In standard packages the dominant component of the heat resistance path is the plastic between the die attach pad and the individual leads. In typical thermally enhanced packages one or more of the leads are fused to the die attach pad, significantly decreasing this component. To make the improvement meaningful, however, a significant copper area on the PCB must be attached to these fused pins.

The patented chip-on-lead frame design of the ADP3330 uniformly minimizes the value of the dominant portion of the thermal resistance. It ensures that heat is conducted away by all pins of the package. This yields a very low 165°C/W thermal resistance for an SOT-23-6 package, without any special board layout requirements, just relying on the normal traces connected to the leads. This yields a 17% improvement in heat dissipation capability as compared to a standard SOT-23-6 package. The thermal resistance can be decreased by, approximately, an additional 10% by attaching a few square cm of copper area to the V_{IN} pin of the ADP3303 package.

It is not recommended to use solder mask or silkscreen on the PCB traces adjacent to the ADP3330's pins since it will increase the junction to ambient thermal resistance of the package.

Error Flag Dropout Detector
The ADP3330 will maintain its output voltage over a wide range of load, input voltage and temperature conditions. If the output is about to lose regulation by reducing the supply voltage below the combined regulated output and dropout voltages, the $\overline{ERR}$ flag will be activated. The $\overline{ERR}$ output is an open collector, which will be driven low.

Once set, the $\overline{ERR}$ flag's hysteresis will keep the output low until a small margin of operating range is restored either by raising the supply voltage or reducing the load.

Shutdown Mode
Applying a TTL high signal to the shutdown ($\overline{SD}$) pin, or tying it to the input pin, will turn the output ON. Pulling $\overline{SD}$ down to 0.4 V or below, or tying it to ground, will turn the output OFF. In shutdown mode, quiescent current is reduced to much less than 1 μA.

Low Power, Low Dropout Applications
ADP3330 is well suited for applications such as cellular phone handsets that require low quiescent current and low dropout voltage features. ADP3330 draws 34 μA typical under light load situations (i.e., load current = 100 μA), which results in low power consumption when the cell phone is in standby mode.

Figure 23 shows an application in which the ADP3330 is used in a handset to provide 2.75 V nominal output voltage. The cell phone is powered from 3 cell NiCd or 1 cell Li-Ion battery. ADP3330 guarantees an accuracy of 1.4%, even when the input/output differential is merely 250 mV (worst case). This implies that the output is regulated and within specification even when the battery voltage has reached its end-of-discharge voltage of 3 V. The output voltage never falls below 2.7 V, even under worst case load and temperature conditions. The low dropout feature coupled with the high accuracy of the ADP3330 ensures that the system is reliably powered until the end of the life of the battery, which results in increased system talk time.

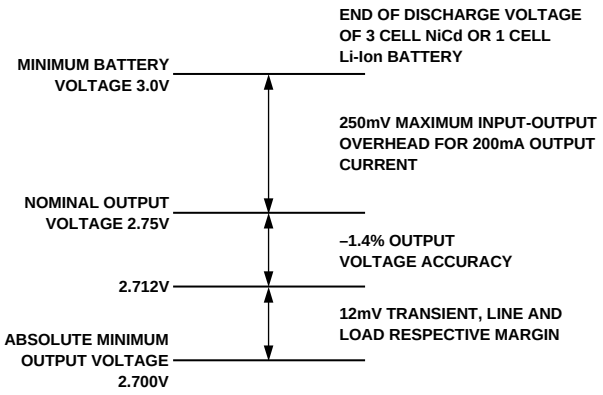


Figure 23. LDO Budgeting for a 3 Cell NiCd/1 Cell Li-Ion Supply

APPLICATION CIRCUITS

Crossover Switch

The circuit in Figure 24 shows how two ADP3330s can be used to form a mixed supply voltage system. The output switches between two different levels selected by an external digital input. Output voltages can be any combination of voltages from the Ordering Guide of the data sheet.

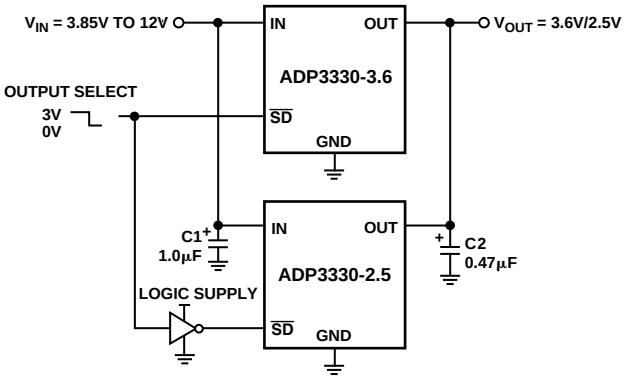


Figure 24. Crossover Switch

Higher Output Current

The ADP3330 can source up to 200 mA at room temperature without any heatsink or pass transistor. If higher current is needed, an appropriate pass transistor can be used, as in Figure 25, to increase the output current to 1 A.

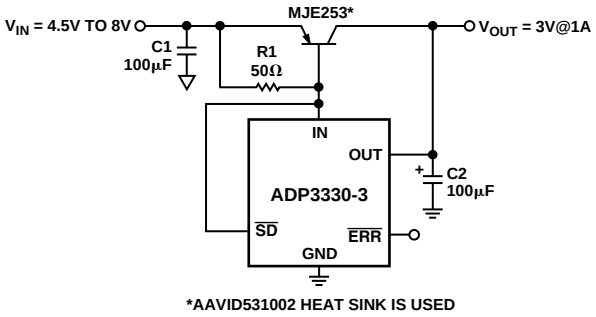
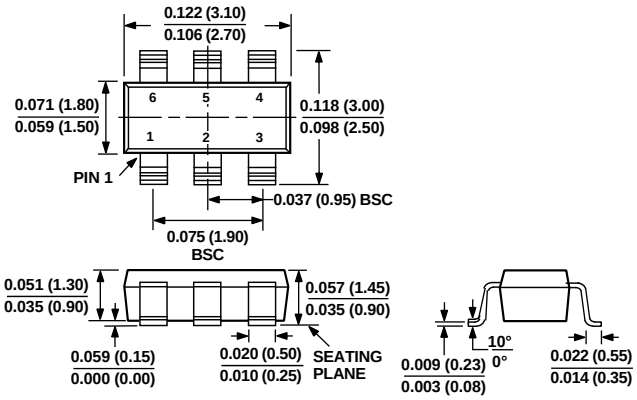


Figure 25. High Output Current Linear Regulator

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead Surface Mount
RT-6 (SOT-23-6)



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