High Input Voltage, Low Quiescent Current, 150mA LDO Regulator

Features

- **Wide Operating Voltage : 6.5V~25V**
- **Ultra Low Ground Current : 70㎂**
- **High Output Accuracy : ±2% Over Temperature**
- **Excellent Load/Line Transient**
- **Low Dropout Voltage : 1900mv @ 150mA**
- **Fixed Output Voltages for 5V/3.3V or Adjustable Voltage**
- **Built-In Reverse Battery Protection**
- **Built-In Reverse Leakage Protection**
- **Built-In Current-Limit Protection**
- **Built-In Over-Temperature Protection**
- **Zero Shutdown Current**
- **Internal Soft-Start Function 0.5ms~1.5ms (max) Over Temperature**
- **POR Scheme to Prevent V_{OUT} Spike**
- **Stable with Aluminum, Tantalum, or Ceramic Capacitors**
- **SOT-23-5, SOT-89, and SOP-8P Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **USB Power Supply**
- **Keep-Alive Supply in Notebook and Portable Computers**
- **Logic Supply for High-Voltage Batteries**
- **Battery Powered Systems**

General Description

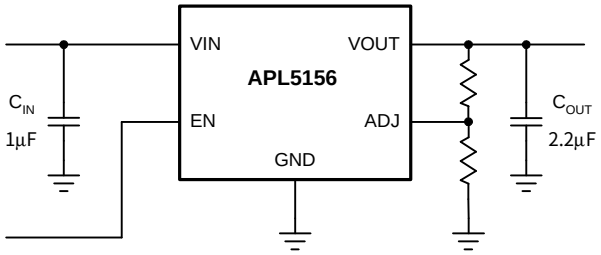
The APL5156 is a low ground current linear regulator, which operates with input voltage from 6.5V to 25V and delivers output current up to 150mA. Typical dropout voltage is only 1.9V at 150mA loading. This combination of the high voltage and the low ground current makes the APL5156 ideal for USB and portable devices, using 2-cell or 3-cell Li-Ion battery inputs.

The APL5156 is stable with aluminum, tantalum, and ceramic capacitors. It requires a 2.2µF or greater capacitor for stability.

The APL5156 has many protection functions, including over-temperature, current-limit, reverse battery, and reverse leakage protections which prevent the device from thermal over-load, current over-load, reverse connection of the battery and output current reversing to the VIN.

The APL5156 regulator is available in miniature SOT-23-5, SOT-89, and SOP-8P packages.

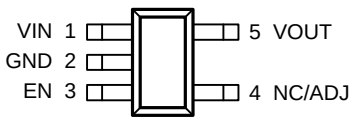
Simplified Application Circuit



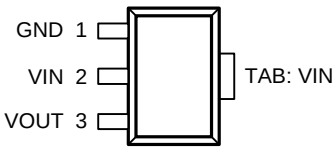
Adjustable Output Voltage (SOT-23-5/SOP-8P)

Pin Configuration

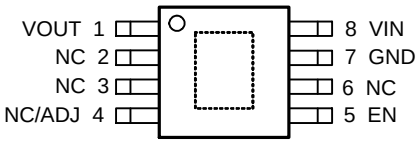
SOT-23-5



SOT-89



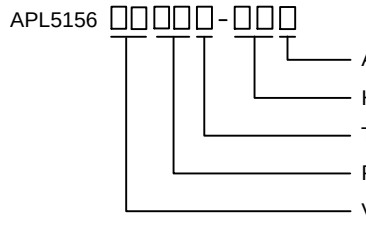
SOP-8P



Thermal Pad (connected to GND plane for better dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information



Package Code
B : SOT-23-5 D : SOT-89 KA : SOP-8P
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Voltage Code :
33 : 3.3V 50 : 5.0V Blank : Adjustable Version
Assembly Material
G : Halogen and Lead Free Device

APL5156 B :	L56X	X - Date Code
APL5156 33B :	56RX	X - Date Code ; 33 - 3.3V
APL5156 50B :	56ZX	X - Date Code ; 50 - 5.0V
APL5156 D :	APL5156 XXXXX33	XXXXX - Date Code ; 33 - 3.3V
APL5156 KA :	APL5156 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN},V_{EN}	VIN, EN to GND Voltage	- 27 to 27	V
	EN to VIN Voltage	-27 to 27	V
V_{OUT},V_{ADJ}	VOUT, ADJ to GND Voltage	- 0.3 to 27	V
	VOUT, ADJ to VIN Voltage	-27 to 27	V
P_D	Power Dissipation	Internally Limited	W
T_J	Operating Junction Temperature	-40 to 125	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient (Note 2) SOT-23-5 SOT-89 SOP-8P	 235 180 50	°C/W

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Thermal Characteristics (Cont.)

Symbol	Parameter	Typical Value	Unit
θ_{JC}	Thermal Resistance-Junction to Case		°C/W
	SOT-23-5	130	
	SOT-89	38	
	SOP-8P	20	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Electrical Characteristics

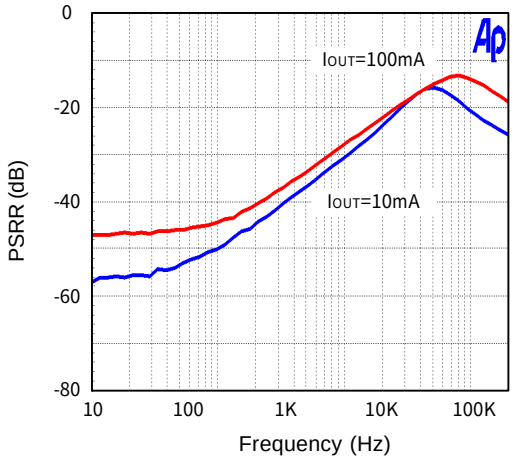
Unless otherwise noted, these specifications apply over V_{IN}=V_{OUT}+2.5V, C_{IN}=1µF, C_{OUT}=2.2µF, T_A=-40°C to 85°C. Typical values refer to T_A=25°C.

Symbol	Parameter	Test Conditions	APL5156			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage		6.5	-	25	V
V_{OUT}	Output Voltage Accuracy		-2	-	2	%
	Output Voltage Range		3	-	20	V
I_Q	Quiescent Current	I_{OUT}=0.1mA	-	70	100	µA
		I_{OUT}=50mA	-	0.5	1	mA
		I_{OUT}=100mA	-	2	3.5	mA
		I_{OUT}=150mA	-	5	7	mA
I_{OUT}	Load Current Range		0	-	150	mA
V_{REF}	Reference Voltage		-2%	1.24	+2%	V
REG_{LINE}	Line Regulation	V_{OUT}+2.5V<V_{IN}<25V, I_{OUT}=1mA	-	0.01	-	%
REG_{LOAD}	Load Regulation	0.1mA<I_{OUT}<150mA	-	0.4	1	%
V_{DROP}	Dropout Voltage	I_{OUT}=0.1mA	-	1300	1900	mV
		I_{OUT}=50mA	-	1600	2000	
		I_{OUT}=100mA	-	1700	2100	
		I_{OUT}=150mA	-	1900	2300	
POWER-ON-RESET (POR)						
	Rising V_{IN} Threshold		4	5	6	V
PROTECTIONS						
OTS	Over-Temperature Shutdown		-	150	-	°C
	Over-Temperature Shutdown Hysteresis		-	10	-	°C
I_{LIMIT}	Circuit Current Limit	V_{IN} =V_{OUT} +2.5V	250	350	500	mA
I_{SHORT}	Short Current	V_{OUT}=0V	-	50	-	mA
	Output Leakage, Reverse Polarity Input	Load=500Ω,V_{IN}= -15V, EN=GND	-	-3	-5	µA
		Load=500Ω, V_{IN}=V_{EN}= -15V	-	-4	-5	mA
SOFT-START AND SHUTDOWN						
T_{SS}	Soft-Start Interval	From enable to V_{OUT} = 90%	0.5	1	1.5	ms
V_{EN}	Input High Voltage		2.5	-	-	V
	Input Low Voltage		-	-	0.6	
I_{EN}	EN Pin Input Bias Current	V_{EN}=25V	-	1	5	µA
I_{QSHDN}	Shutdown Supply Current	EN=Low, V_{IN}=19V	-	0.1	1	µA

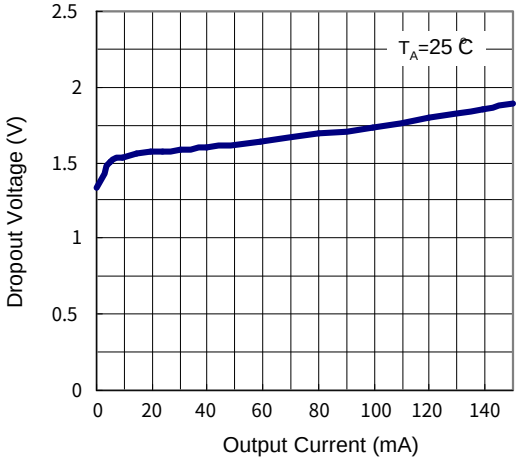
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Typical Operating Characteristics

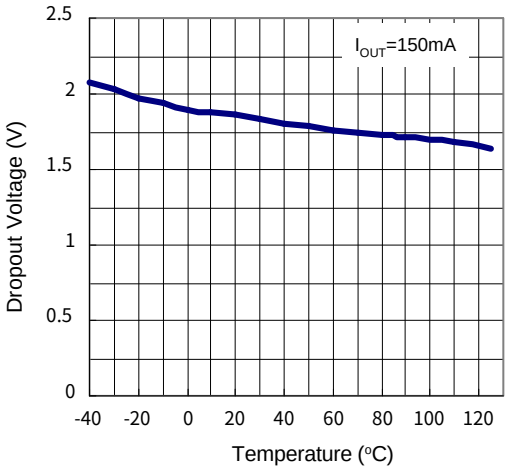
PSRR vs. Frequency



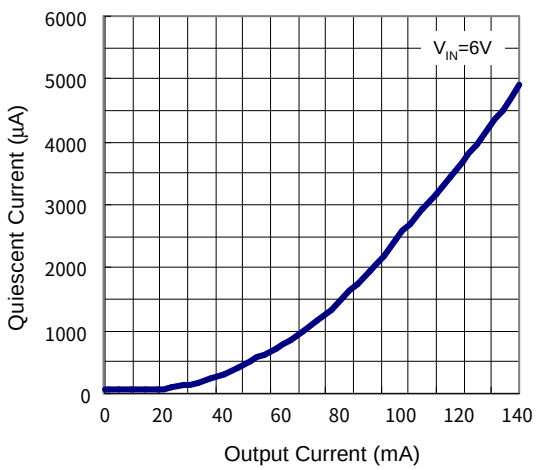
Dropout Voltage vs. Output Current



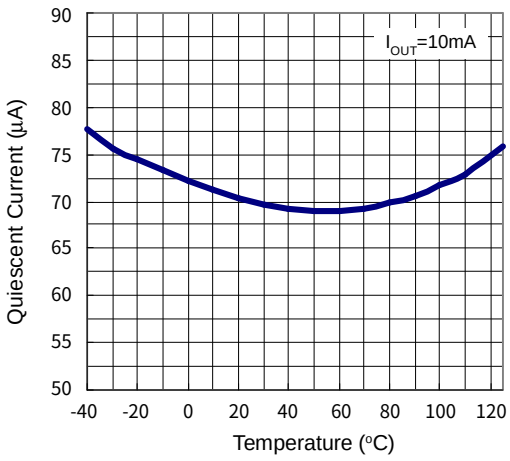
Dropout Voltage vs. Temperature



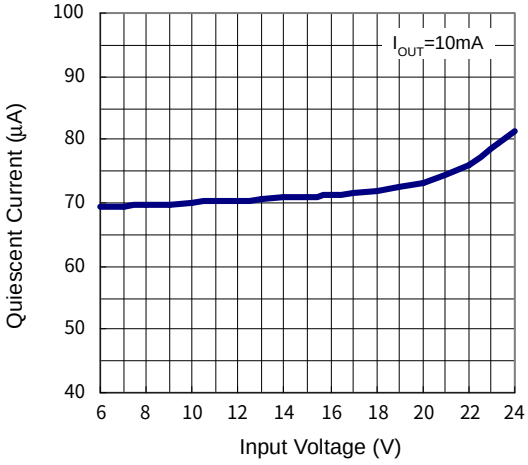
Quiescent Current vs. Output Current



Quiescent Current vs. Temperature

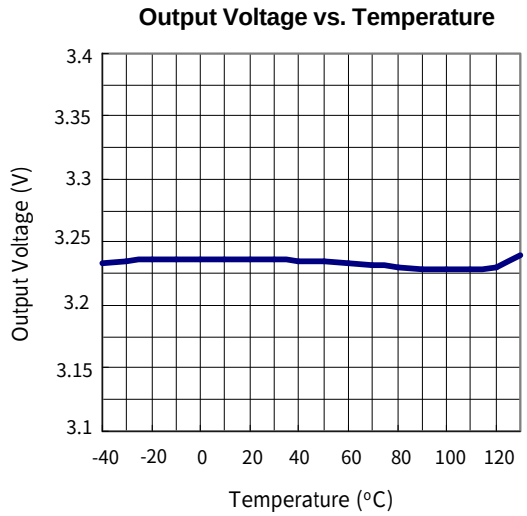


Quiescent Current vs. Input Voltage



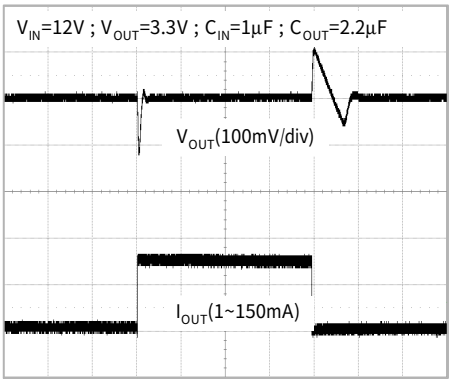
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Typical Operating Characteristics (Cont.)



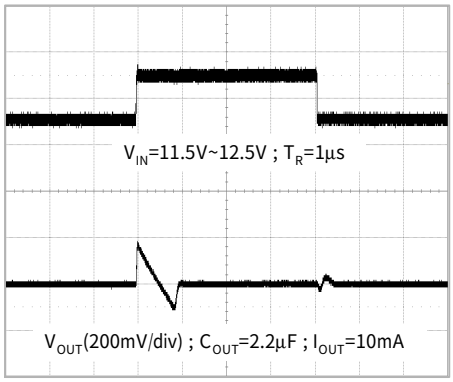
Operating Waveforms

Load Transient



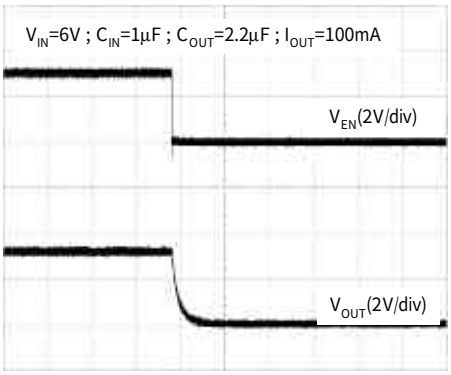
Time (50µs/div)

Line Transient



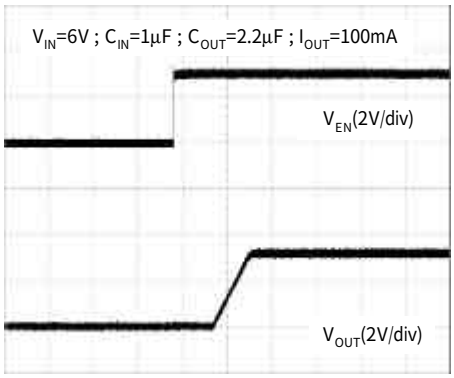
Time (50µs/div)

Entering Shutdown Delay



Time (0.5ms/div)

Exiting Shutdown Waveform



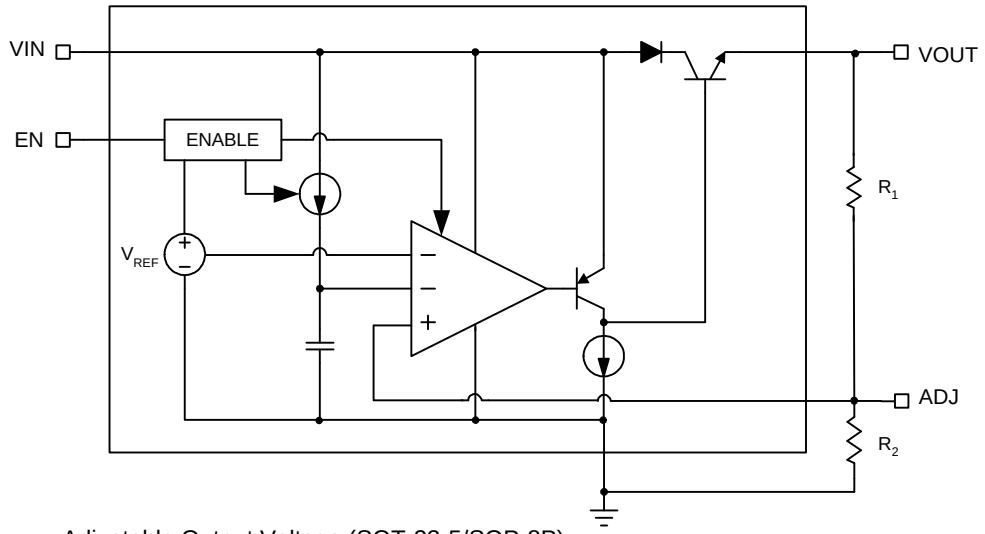
Time (0.5ms/div)

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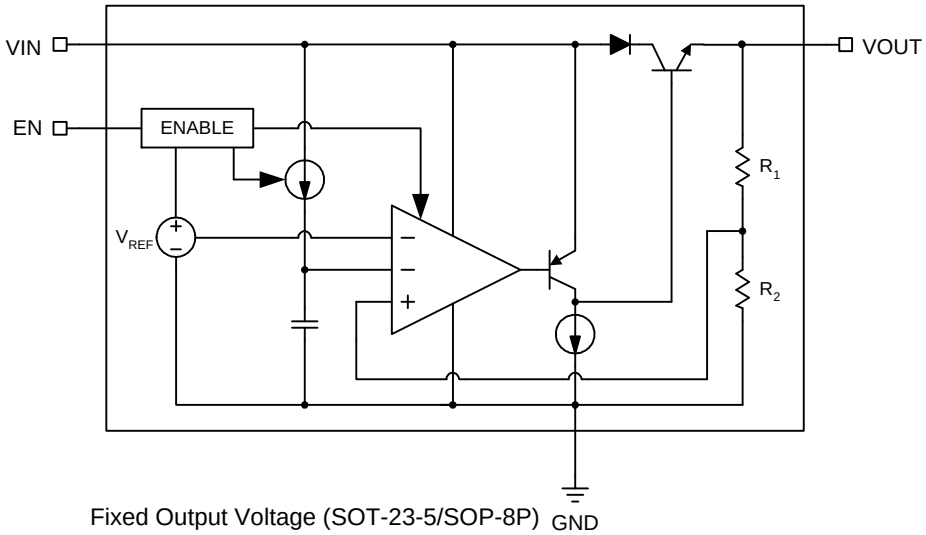
Pin Description

PIN				FUNCTION
NO.			NAME	
SOT-23-5	SOT-89	SOP-8P		
1	2	8	VIN	Voltage supply input pin
2	1	7	GND	Ground
3	-	5	EN	Enable pin, Logic low=shutdown; Logic high=enable
4	-	4	NC/ADJ	NC: No Connection ADJ: Output voltage feedback pin
5	3	1	VOUT	Regulator output pin

Block Diagram

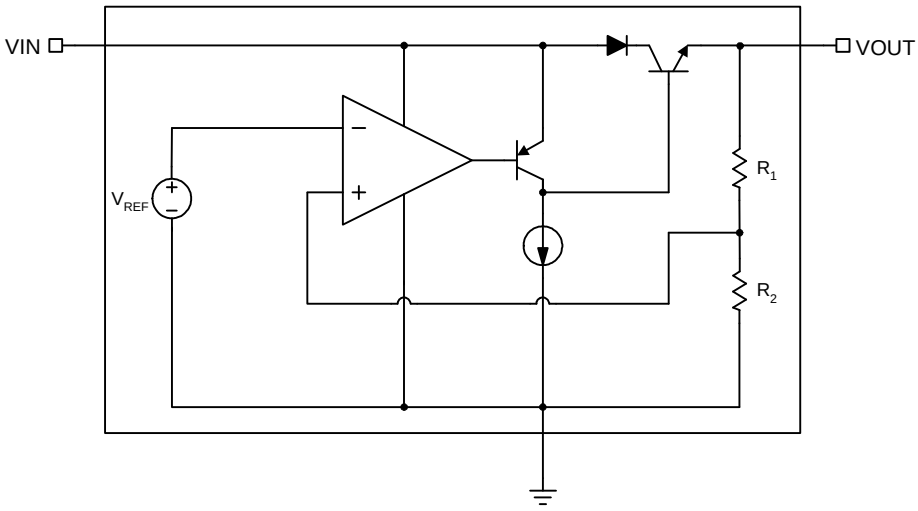


Adjustable Output Voltage (SOT-23-5/SOP-8P)



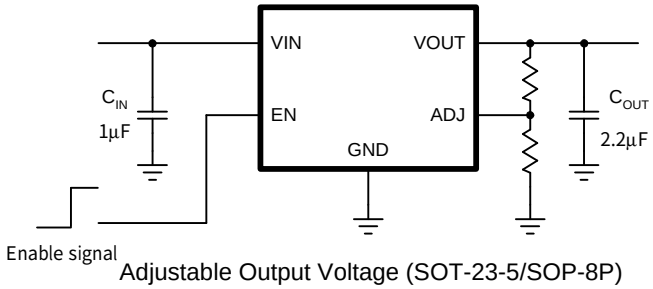
Fixed Output Voltage (SOT-23-5/SOP-8P)

Block Diagram (Cont.)

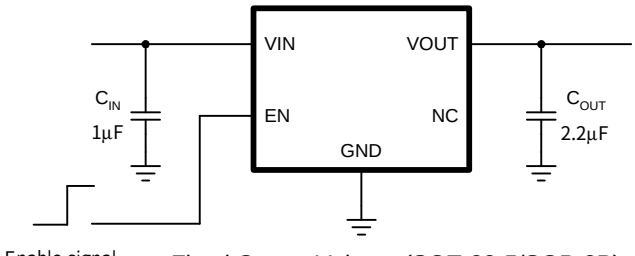


Fixed Output Voltage (SOT-89)

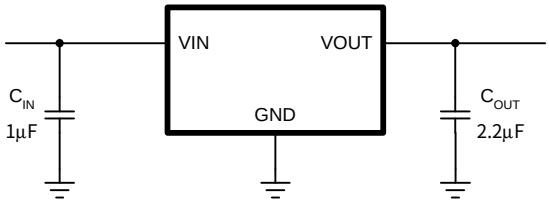
Typical Application Circuit



Adjustable Output Voltage (SOT-23-5/SOP-8P)



Fixed Output Voltage (SOT-23-5/SOP-8P)



Fixed Output Voltage (SOT-89)

Application Information

Enable/Shutdown

The APL5156 features an active-high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator, so current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. The enable pin can not float.

Input Capacitor

The APL5156 has high input voltage up to 25V. The input capacitor must be rated to sustain voltages that may be used on the input. An input capacitor may be required when the device is not near the source power supply or when supplied by a battery. Small and surface-mounted ceramic capacitors can be used for bypassing. A larger value may be required if the source supply has high ripple.

Output Capacitor

The APL5156 requires an output capacitor for stability. The design requires 2.2µF or greater on the output to maintain stability. It is optimized by using low-ESR ceramic chip capacitors. The maximum allowable ESR is 3Ω. More capacitance improves transient response. Place the output capacitor as close to the VOUT pin as possible. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R type capacitors change capacitance by 15% over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

No-Load Stability

The APL5156 will remain stable and in regulation with no load unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

Thermal Consideration

The thermal resistance of junction to ambient controls the APL5156's maximum power dissipation. The power dissipation across the device is $P_D=I_{OUT}(V_{IN}-V_{OUT})$, and the maximum power dissipation is:

$$P_{D(MAX)}=\frac{T_J-T_A}{\theta_{JA}}$$

where T_J-T_A is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air.

For continual operation, do not exceed the absolute maximum junction temperature rating of T_J=125°C.

For example:

In SOT-23-5 package θ_{JA}=235°C/W. When operates the APL5156 at T_A=50°C, the maximum power dissipation can be determined as below:

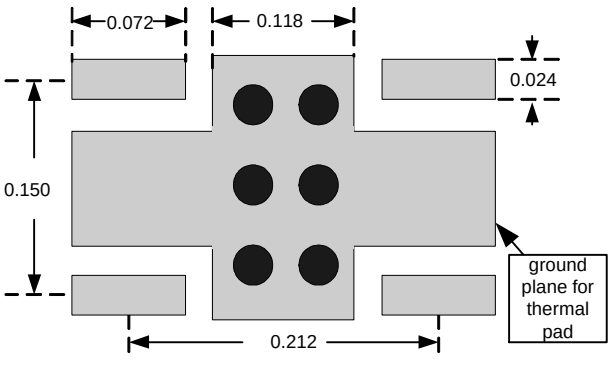
$P_{D(MAX)}$=(125°C-50°C)/(235°C/W)

$P_{D(MAX)}$=319.1mW

Thermal Pad Consideration

The SOP-8P is a cost-effective package which features a small size, like a standard SOP-8, and a bottom thermal pad to minimize the thermal resistance of the package is applicable to high current applications. The thermal pad must be soldered down to the copper plane on circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 4 or 6 vias should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.



SOP-8P Layout Recommendation

Application Information (Cont.)

Adjustable Regulator Application

The output voltage of APL5156 can be adjusted from 3V to 20V by using two external resistors. The resistors set the output voltage based on the following equation:

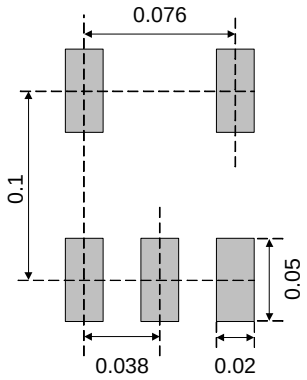
$$V_{OUT} = V_{REF}\left(1+\left(\frac{R_1}{R_2}\right)\right)$$

where V_{REF}=1.24V

Feedback resistor R_2 should be larger than 100kΩ and smaller than 1MΩ. The resistors should be placed as close the device as possible to avoid noise.

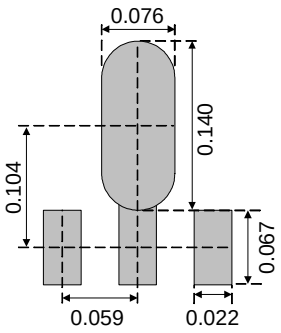
Recommended Minimum Footprint

SOT-23-5



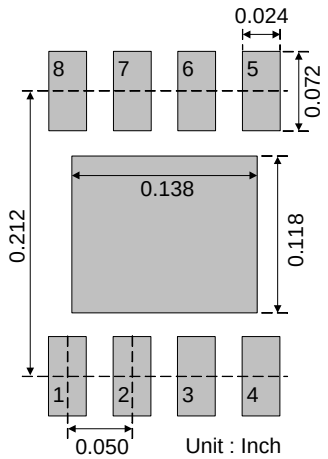
Unit : Inch

SOT-89



Unit : Inch

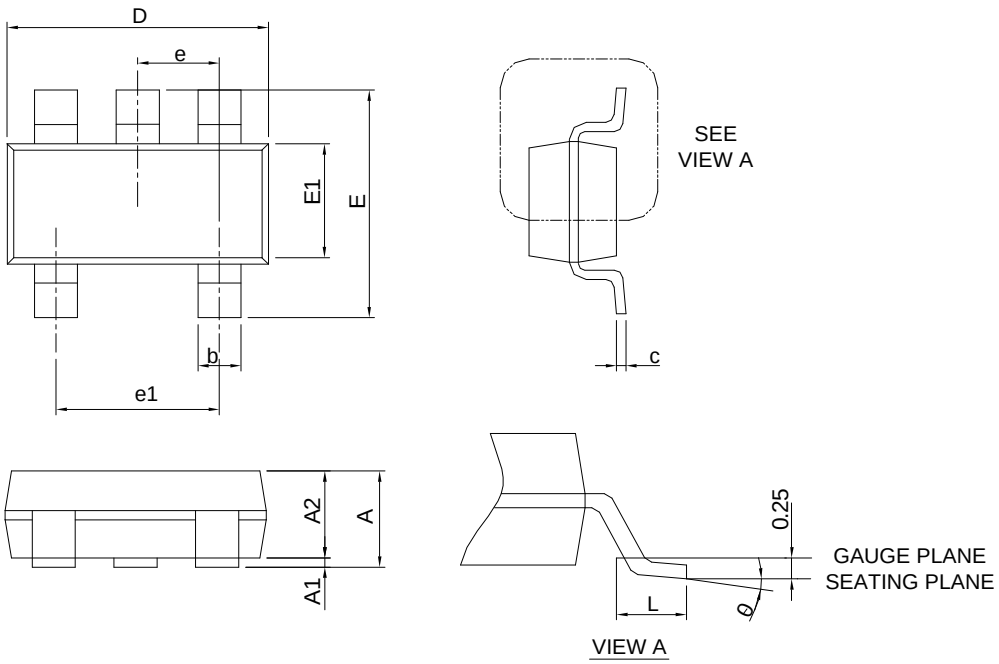
SOP-8P



Unit : Inch

Package Information

SOT-23-5



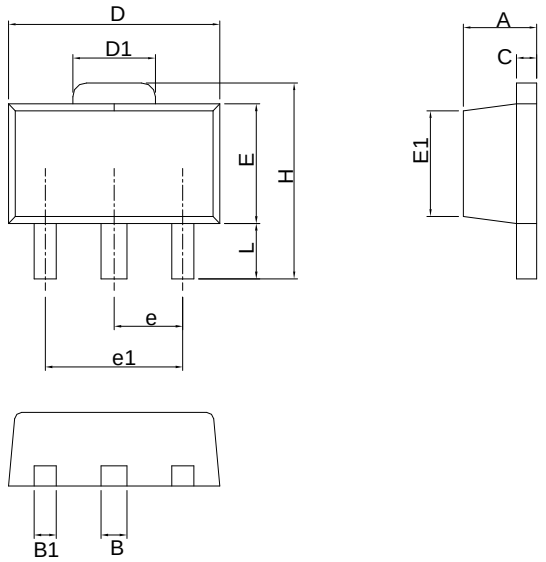
SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

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Package Information

SOT-89



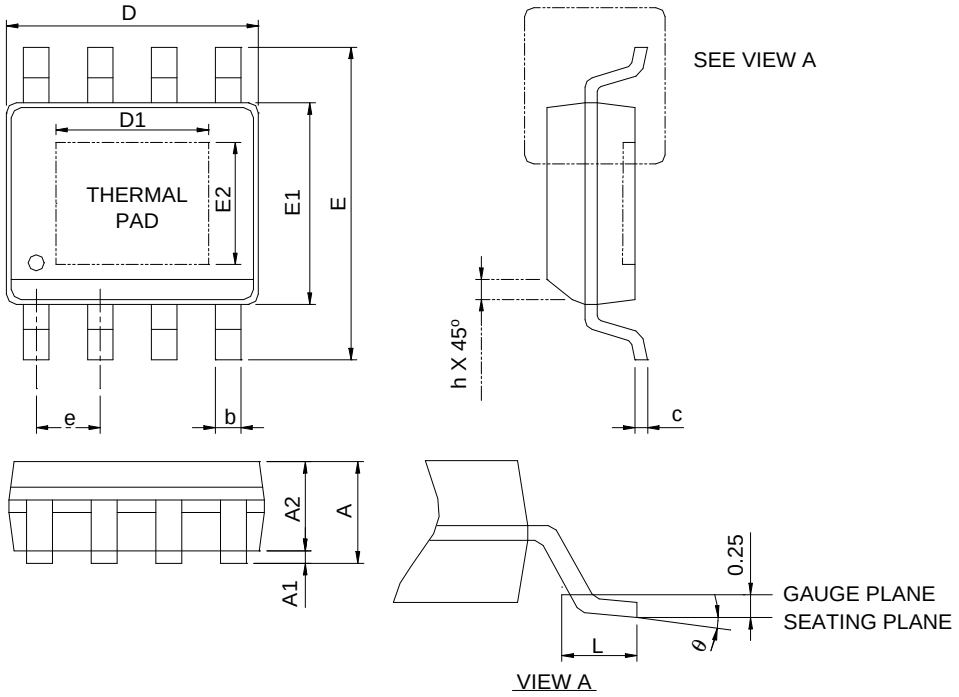
SYMBOL	SOT-89			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.40	1.60	0.055	0.063
B	0.44	0.56	0.017	0.022
B1	0.36	0.48	0.014	0.019
C	0.35	0.44	0.014	0.017
D	4.40	4.60	0.173	0.181
D1	1.62	1.83	0.064	0.072
E	2.29	2.60	0.090	0.102
E1	2.13	2.29	0.084	0.090
e	1.50 BSC		0.059 BSC	
e1	3.00 BSC		0.118 BSC	
H	3.94	4.25	0.155	0.167
L	0.89	1.20	0.035	0.047

Note : Follow JEDEC TO-243 AA.

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Package Information

SOP-8P

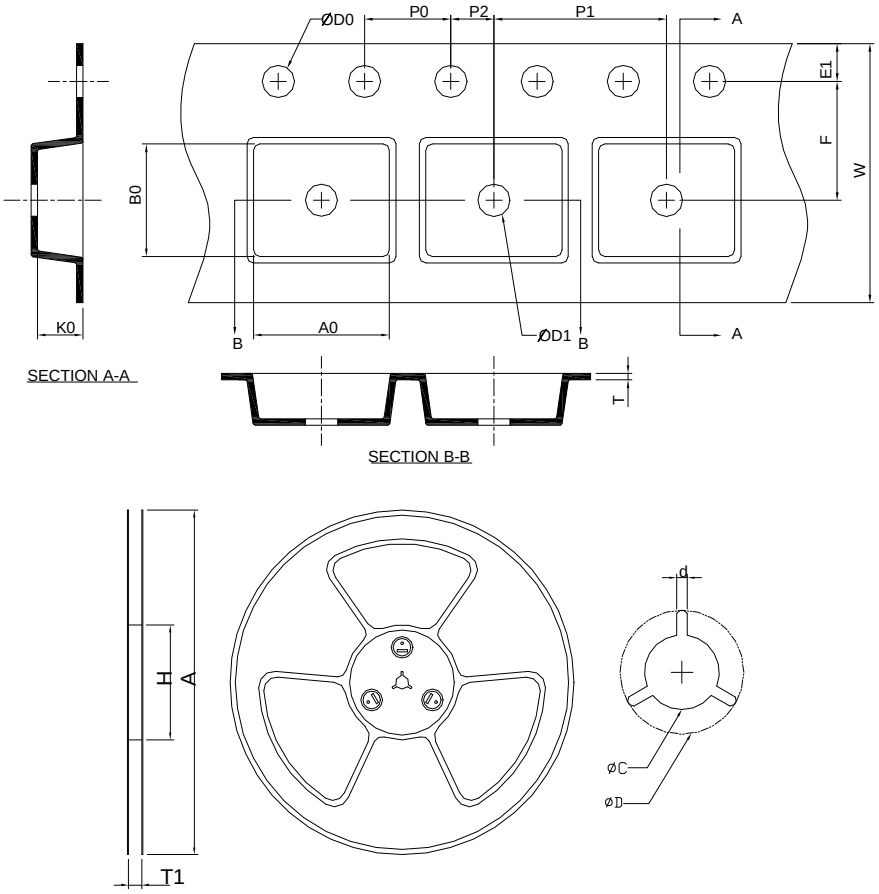


SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

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Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SOT-89	178.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.80±0.20	4.50±0.20	1.80±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

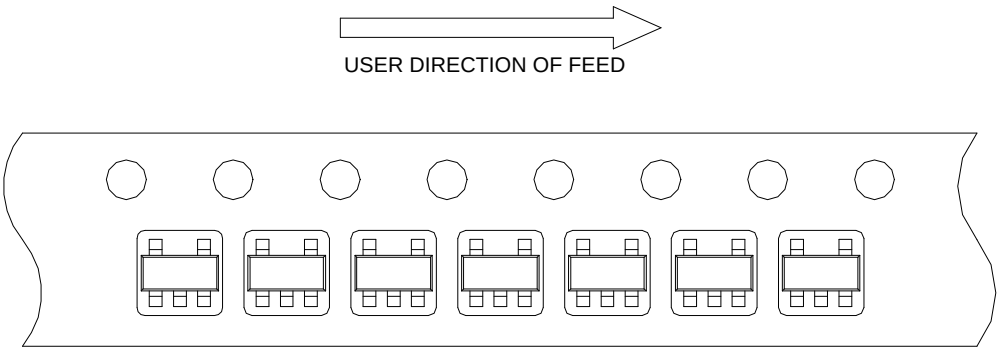
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Devices Per Unit

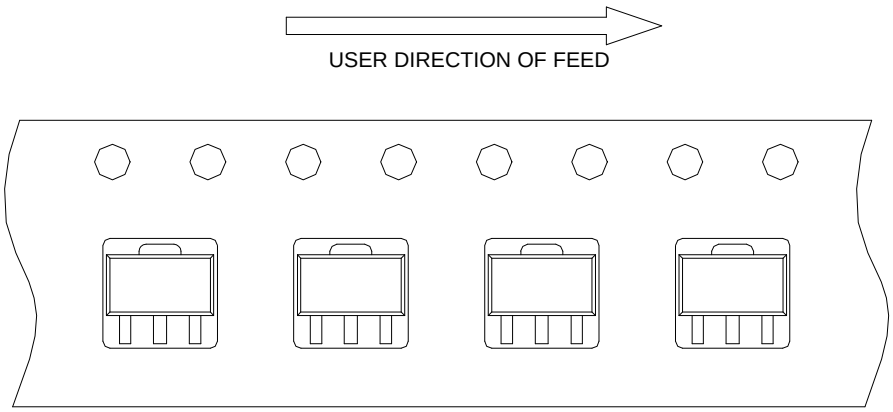
Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000
SOT-89	Tape & Reel	1000
SOP-8P	Tape & Reel	2500

Taping Direction Information

SOT-23-5

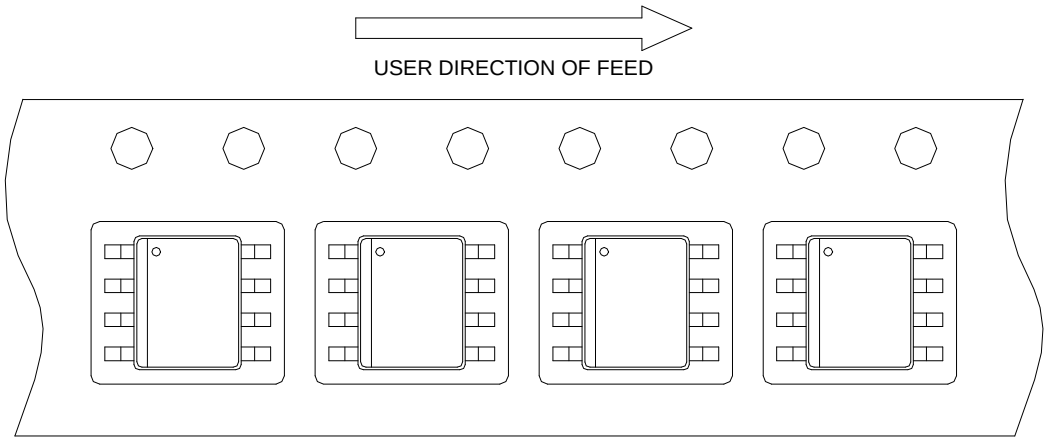


SOT-89

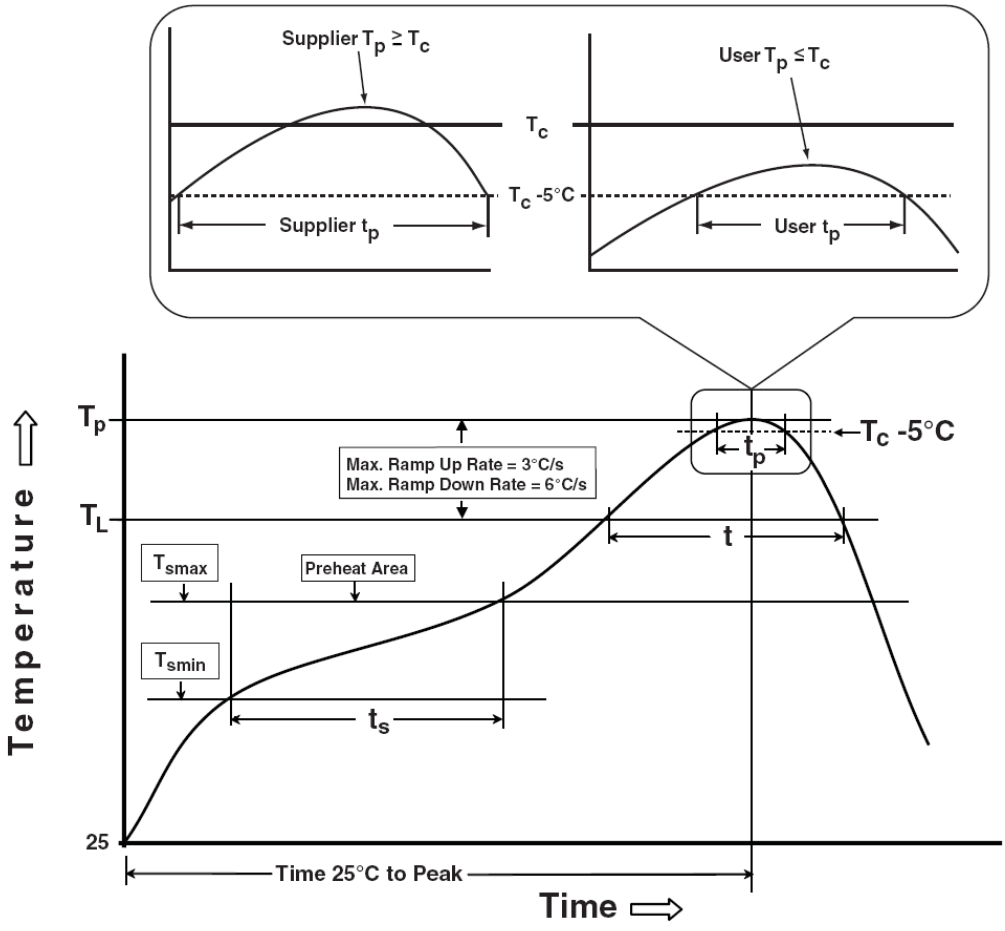


Taping Direction Information

SOP-8P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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