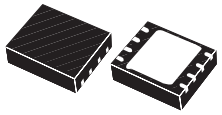
STLD41

White LED driver for mid-size LCD display backlight

Datasheet – production data

Features

- Boost DC-DC converter
- Drives up to 40 LEDs (4 strings of 10) with a total current up to 120 mA
- Input voltage range: 3.0 V to 21 V
- Output current control
- 1.4 MHz fixed frequency PWM control
- PWM input for output current dimming with frequency range 25 kHz - 50 kHz
- 2 A integrated switch
- Overvoltage protection
- Chip overtemperature detection and protection
- Less than 1 µA standby current
- Soft-start function
- Package DFN8 (3 x 3) 0.65 mm pitch



DFN8 (3 x 3 mm)

Applications

- Mini PCs
- PMP & PND
- Printers
- Game consoles

Description

The STLD41 is a boost converter that operates from 3.0 V to 21 V and can provide an output voltage as high as 38 V. It can drive up to 40 white LEDs connected in 4 strings of 10 LEDs in series. The total output current capability is 120 mA at an output voltage of 38 V. Regulation is performed by the internal error amplifier which works with the feedback voltage from the sensing resistor. The device can be turned ON/OFF by way of the logic signal connected to the EN pin. The LEDs can be dimmed by applying a PWM signal to the PWM pin.

Table 1. Device summary

Order code	Package	Packaging
STLD41PUR	DFN8 (3 x 3 mm)	3000 parts per reel

This is information on a product in full production. www.st.com

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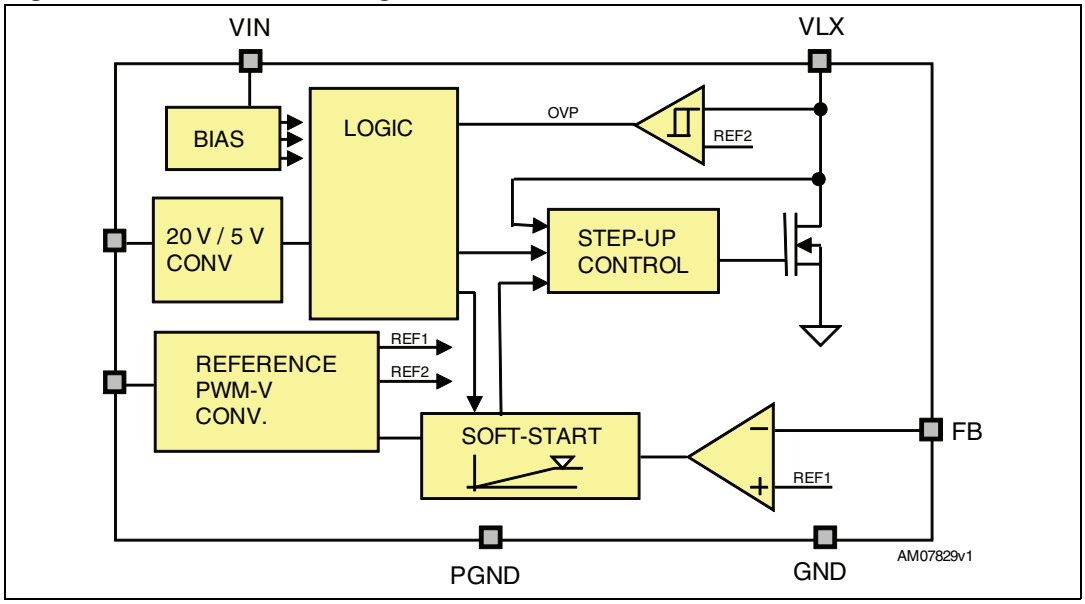
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1 Block diagram

Figure 1. STLD41 block diagram



2 Pin configuration

Figure 2. Pin connections (top view)

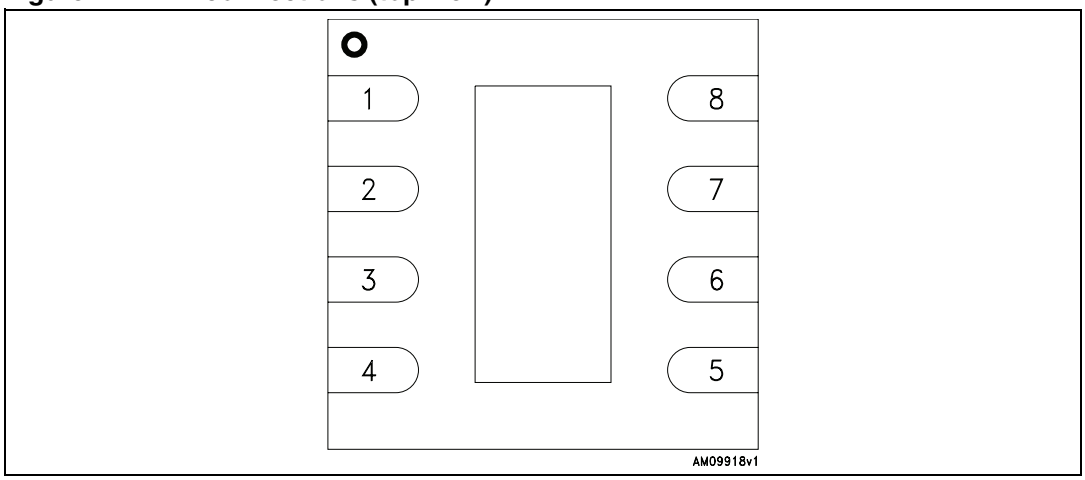


Table 2. Pin description

Pin n°	Symbol	Description
1	GND	Ground
2	FB	Feedback connection
3	GND	Analog ground
4	PGND	Power ground
5	VLX	Inductor connection
6	EN	Enable input
7	VIN	Supply voltage
8	PWM_IN	PWM input for the output current dimming
Exposed pad	PGND	Power ground

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VIN	Signal supply voltage	- 0.3 to 23	V
VLX	Inductor connection	- 0.3 to 40	V
FB	Feedback connection	- 0.3 to 2	V
EN	Logic pin	- 0.3 to 21	V
PWM_IN	PWM input	- 0.3 to 6	V
ESD	Human body model	± 2	kV
P_{TOT}	Continuous power dissipation (at T_A = 70 °C) (1)	TBD	mW
T_{OP}	Operating ambient temperature range	- 40 to 85	°C
T_J	Junction temperature	- 40 to 150	°C
T_{STG}	Storage temperature range	- 65 to 150	°C

1. Power dissipation is dependent on the PCB. PCB design recommendations are included in *Section 7.5: PCB layout*.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	46	°C/W

4 Typical application circuit

Figure 3. Application circuit schematic

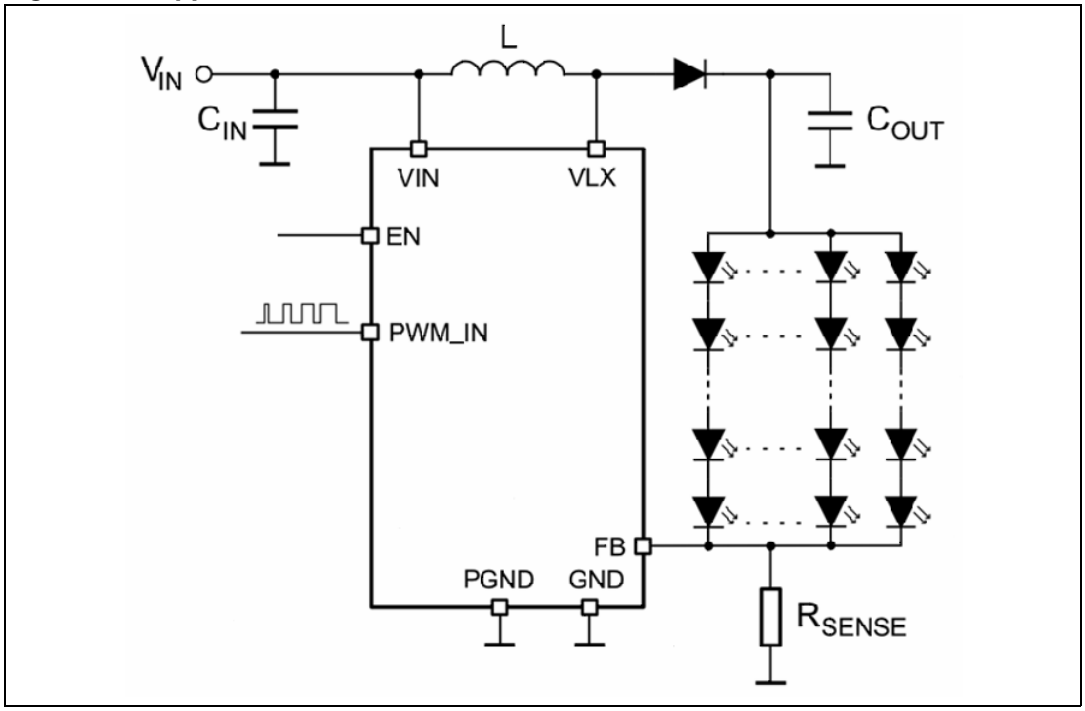


Table 5. List of external components

Component	Manufacturer	Part number	Value	Size
C_{IN}	Murata	GRM32ER71H106K	10 µF / 50 V	3.2 x 2.5 x 2.5 mm
C_{OUT}	Murata	GRM31CR61H225KA88L	2.2 µF / 50 V	3.2 x 1.6 x 1.6 mm
L	Murata	LQH6PPN470M43	47 µH / 1.25 A	6 x 6 x 4.3 mm
	Coilcraft	LPS6235-473MLB	47 µH / 1.2 A	6 x 6 x 3.5 mm
R_{SENSE}	Tyco Electronics		1.3 Ω	0603 size
Schottky diode	STMicroelectronics	STPS1L40M	1 A / 40 V	3.75 x 1 x 1.9 mm
LED	OSRAM	LWL283-Q1R2-3K8L-1-Z	20 mA / 3.1 V	0603

Note: The above listed components refer to a typical application with a maximum performance setting. Operation of the STLD41 is not limited to the choice of these external components.

5 Electrical characteristics

C_{IN} = 10 µF, C_{OUT} = 2.2 µF, L = 47 µH / 1.25 A, R_{SENSE} = 1.3 Ω, T_A = 25 °C, V_{IN} = 5.5 V typ. Values are at 25 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input operating supply voltage		3.0		21	V
I_O	Output current adjustment range	V_{IN} = 3.0 V to 5.0 V; V_{OUT} = 38 V			40	mA
		V_{IN} = 5.0 V to 7.0 V; V_{OUT} = 38 V			78	
		V_{IN} = 7.0 V to 18 V; V_{OUT} = 38 V			120	
V_{OUT}	Regulated voltage range	V_{IN} = 3.0 V to 21 V	1.15*V_{IN}		38	V
I_{PEAK}	Inductor peak current	V_{IN} = 3 V, V_{OUT} = 38 V		2		A
ΔI_O	Output current variation	V_{IN} = 3 V, I_{LED} = 120 mA	-10		10	%
I_Q	Quiescent current in Standby mode	EN = LOW, V_{IN} = 5.5 V			1	µA
V_{FB}	Feedback voltage	I_{LED} = 120 mA, PWM_IN=HIGH	144	160	176	mV
V_{FBMIN}	Min. feedback voltage	PWM_IN = 30 kHz, duty cycle = 10%		35		mV
f_s	Frequency	V_{IN} = 3.0 V		1.4		MHz
ν	Efficiency of the chip itself (1)	V_{IN} = 7 to 21 V, I_O = 120 mA, V_O = 10 x V_{FLED_max}+V_{RSENSE} = 38 V		87		%
ν	Efficiency of the whole application (2)	V_{IN} = 3 to 21 V, I_O = 78 mA		79		%
OVP	Output overvoltage protection	V_{IN} = 21 V, No load		40		V
OTP	Overtemperature protection	V_{IN} = 21 V		140		°C
OT_{HYST}	Overtemperature hysteresis	V_{IN} = 21 V		20		°C
V_{IL}	Low and high level input logic signal on EN pin	V_{IN} = 3.0 V to 21 V	0		0.4	V
V_{IH}			1.4		V_I	
I_{ENHIGH}	Enable input current	V_{IN} = 3.0 V to 21 V, V_{EN} = 21 V		10		µA
T_{ON}	LED current rise time I_{LED} = 0 to I_{LED} = max	V_{IN} = 10 V		1		ms
f_{PWM}	PWM dimming signal frequency	V_{IN} = 3.0 V to 21 V	25		50	kHz
V_{PWM}	PWM signal level	V_{IN} = 3.0 V to 21 V	1.4		5.5	V

1. Calculated as (V_{OUT}*I_{LED})/(V_{IN}*I_{IN}), guaranteed by design
2. Calculated as (V_{LED}*I_{LED})/(V_{IN}*I_{IN}), guaranteed by design

6 Introduction

The STLD41 is a boost converter, dedicated to power and control the current of white LEDs in an LCD backlight. The device operates at a typical constant switching frequency of 1.4 MHz. It steps an input voltage ranging from 3.0 V to 21 V up to 40 V. The output current is dimmable by the PWM signal applied to the PWM pin.

6.1 PWM input

The light intensity can be dimmed by a signal applied to the PWM input. It is recommended to use a signal whose frequency is between 25 kHz to 50 kHz. The maximum amplitude of the signal is limited to 5.5 V. The minimum level of the signal must be at least 1.4 V. The dimming range is from 20% to 100% of the current set by the R_{SENSE}.

7 Selection of external components

7.1 C_{IN} selection

It is recommended to use 10 µF as the input capacitor to achieve good stability of the device and low noise on the V_{IN} track.

7.2 C_{OUT} selection

It is recommended to use 2.2 µF as the optimal value of output capacitor to achieve the best compromise between output voltage ripple and load transient response. The output ripple can be checked using the equation for step-up architecture:

Equation 1

$$V_{PK-PK} = \frac{I_{OUT(MAX)} * (V_{OUT} - V_{IN(MIN)}) * 100}{C_{OUT} * V_{OUT}^2 * f} [V; A, V, F, Hz]$$

7.3 Inductor selection

A thin shielded inductor with a low DC series winding resistance is recommended for this application. To achieve good efficiency in step-up mode, it is recommended to use an inductor with a DC series resistance $R_{DCL} = R_D / 10$ [Ω, Ω, 1], where R_D is the dynamic resistance of the LED [Ω, Ω, 1].

For nominal operation, the peak inductor current can be calculated using this formula:

Equation 2

$$I_{PEAK} = \frac{I_{OUT}}{n} + \frac{(V_{OUT} - V_{IN}) * V_{IN}^2}{2 * L * f * V_{OUT}^2} * \frac{V_{OUT}}{V_{IN}}$$

where:

I_{PEAK} = Peak inductor current

I_{OUT} = Current sourced at the V_{OUT} pin

n = Efficiency of the STLD41

V_{OUT} = Output voltage at the V_{OUT} pin

V_{IN} = Input voltage at the VBAT-pin

L = Inductance value of the inductor

f = Switching frequency

For optimal performance of the STLD41 device, is recommended to use an inductor value of 47 µH or higher with low serial resistance and relevant saturation current calculated from the equation above.

7.4 R_{SENSE} value

$R_{SENSE} = V_{REF1} / I_{LED}$

If using a typical setting of I_{LED} = 120 mA, V_{REF1} = 160 mV, and R_{SENSE} = 1.3 Ω, the resistor must be rated for a power dissipation of 1.3 x 0.12^2 W = 0.02 W.

7.5 PCB layout

Because the STLD41 is a powerful switched device, the PCB must be designed in line with rules for designing switched supplies. It is recommended to use a two-layer PCB. The power wirings must be as short as possible and wide. Place all external components close to the STLD41 device. High-energy switched loops should be as small as possible to reduce EMI. Most LEDs need cooling, which can be attained utilizing a defined copper area on the PCB. Use the reference guide for each LED to design the heatsink. Place the R_{SENSE} resistor as close as possible to pin 2 and ground of the system. The ground of the system is represented by the size of the area created by the connections GND-PGDN-GND_{CIN}-GND_{COUT}. When a change of PCB layer is needed, use sufficient vias. During routing, the PCB must be focused on the minimum area of the application ground; the smaller the ground area of the DC-DC converter[(a)], the better the stability and there will be fewer noise issues. It is recommended to place the copper plate connected through the vias to the exposed pad to the bottom layer to create the heatsink of the device.

a. The application ground area is represented by the area which is created by the ground pins of the C_{IN}, C_{OUT}, and ground of the DEVICE and GND connection of the load.

Figure 4. Top layer

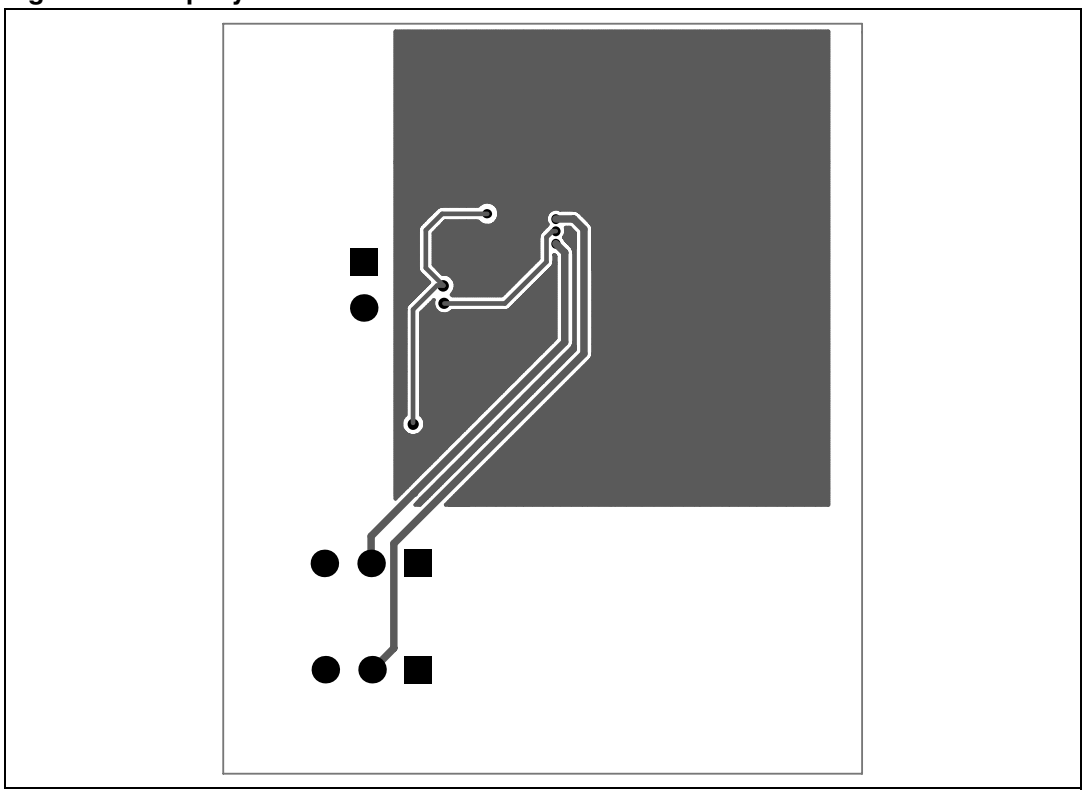


Figure 5. Bottom layer

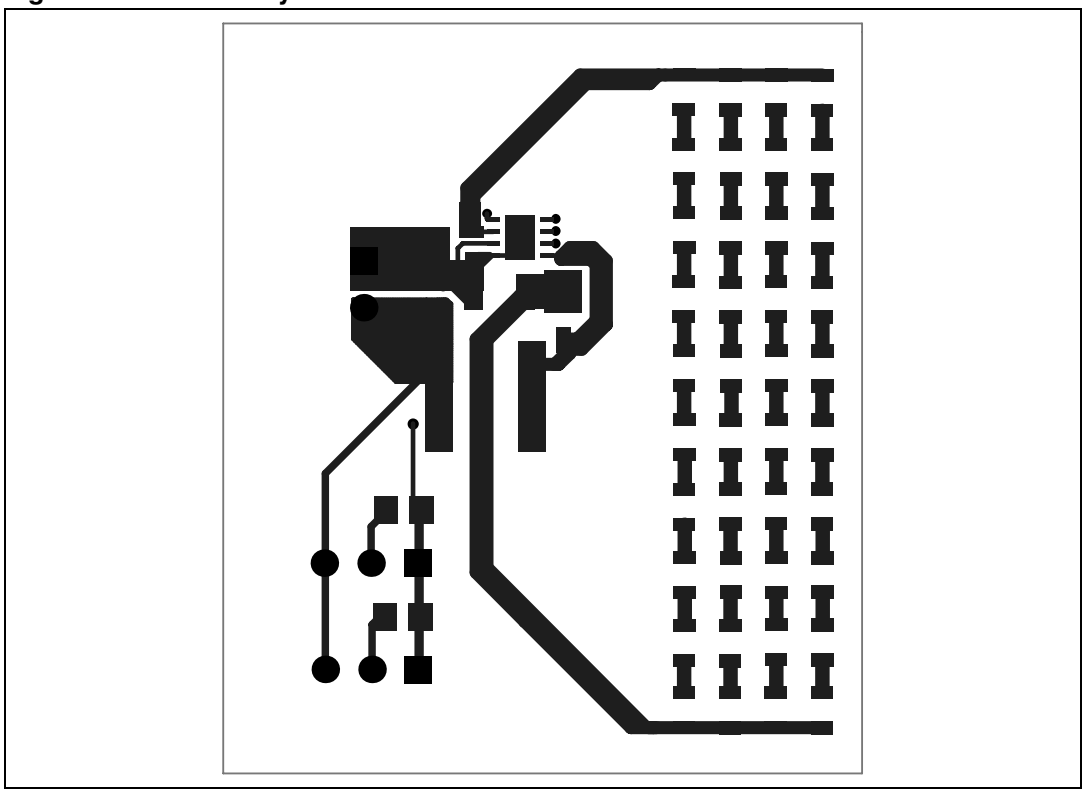
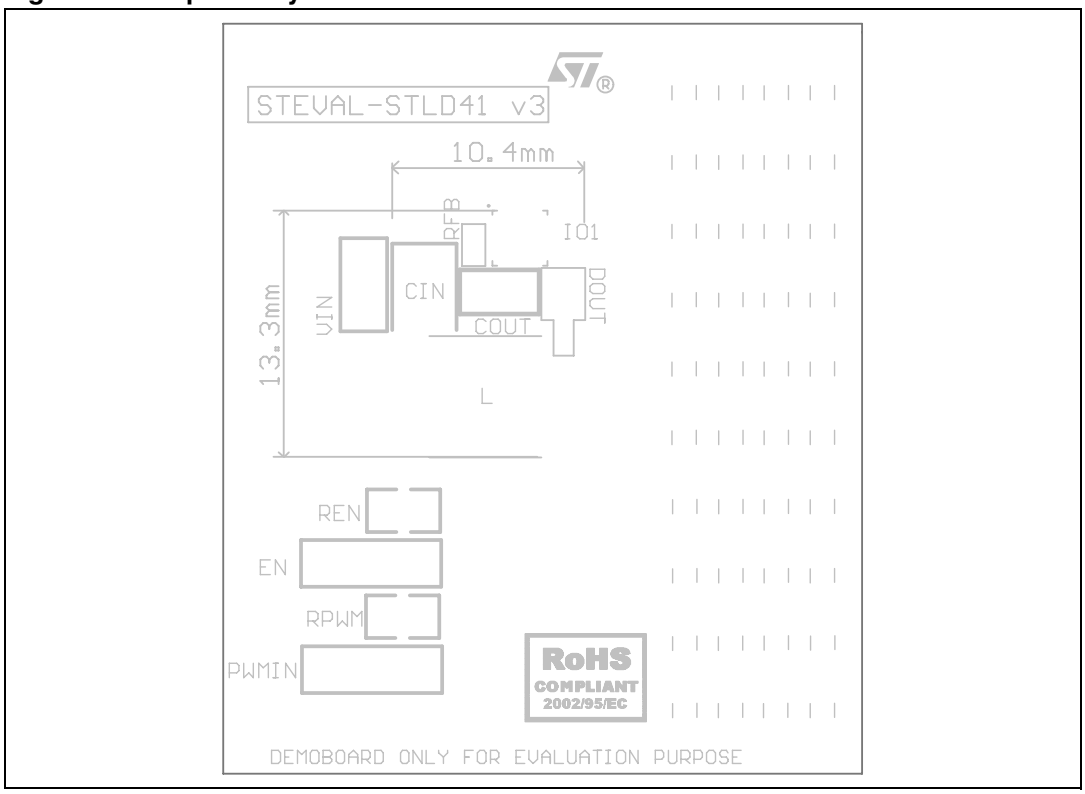


Figure 6. Top overlay



8 Typical performance characteristics

Figure 7. Eff. vs. V_{IN}, 6 x 6 LEDs, V_{OUT} = 24 V

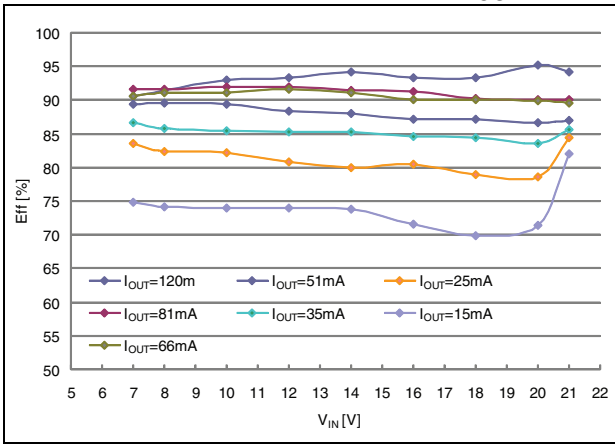


Figure 8. Eff. vs. V_{IN}, 5 x 7 LEDs, V_{OUT} = 27 V

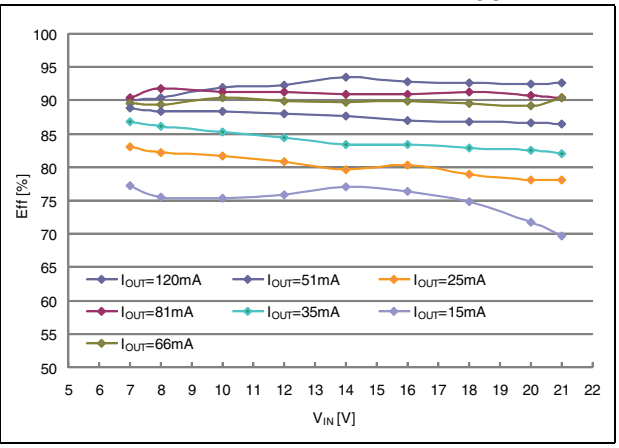


Figure 9. Eff. vs. V_{IN}, matrix 4 x 9 LEDs, V_{OUT} = 33 V

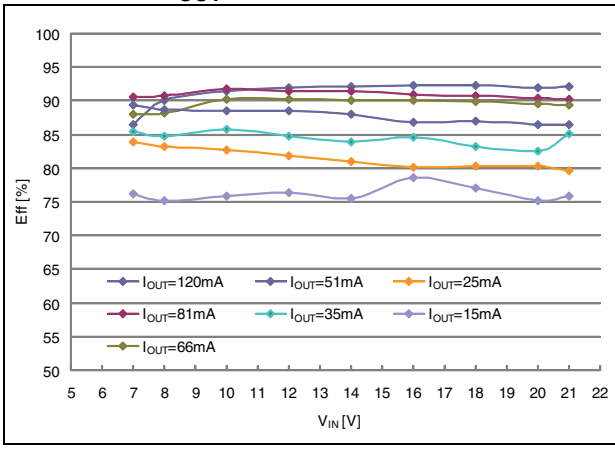


Figure 10. Application eff. vs. V_{IN}, matrix 4 x 10 LEDs

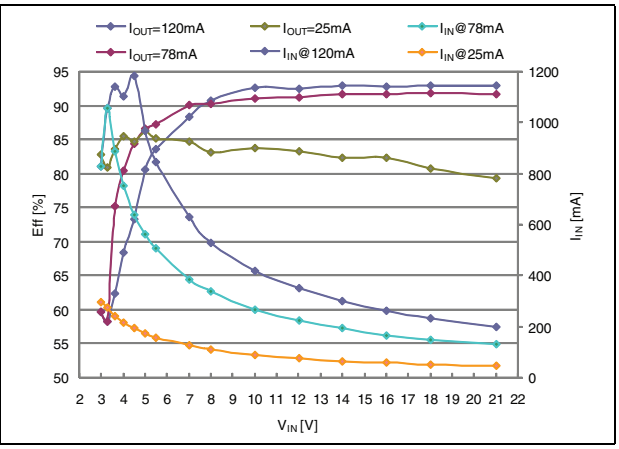


Figure 11. Output current regulation at 4 x 10 LEDs

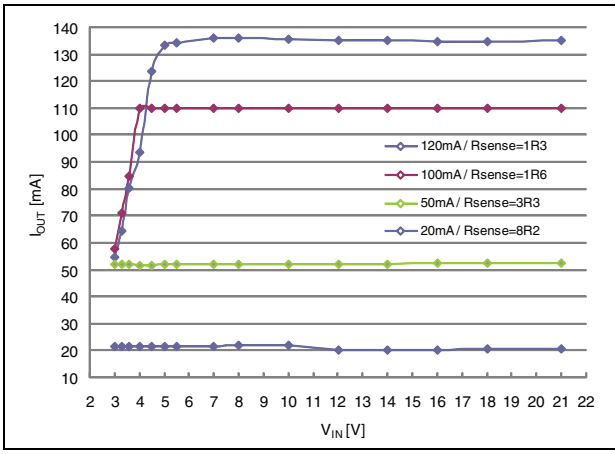
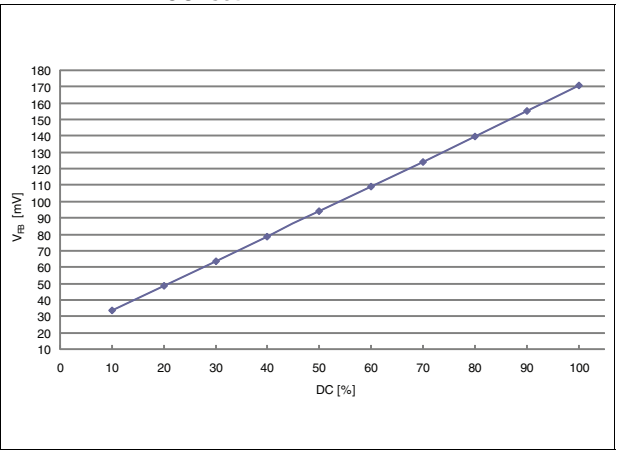


Figure 12. V_{FB} vs. PWM 25 kHz, V_{IN} = 5.5 V, I_{OUTset} = 120 mA



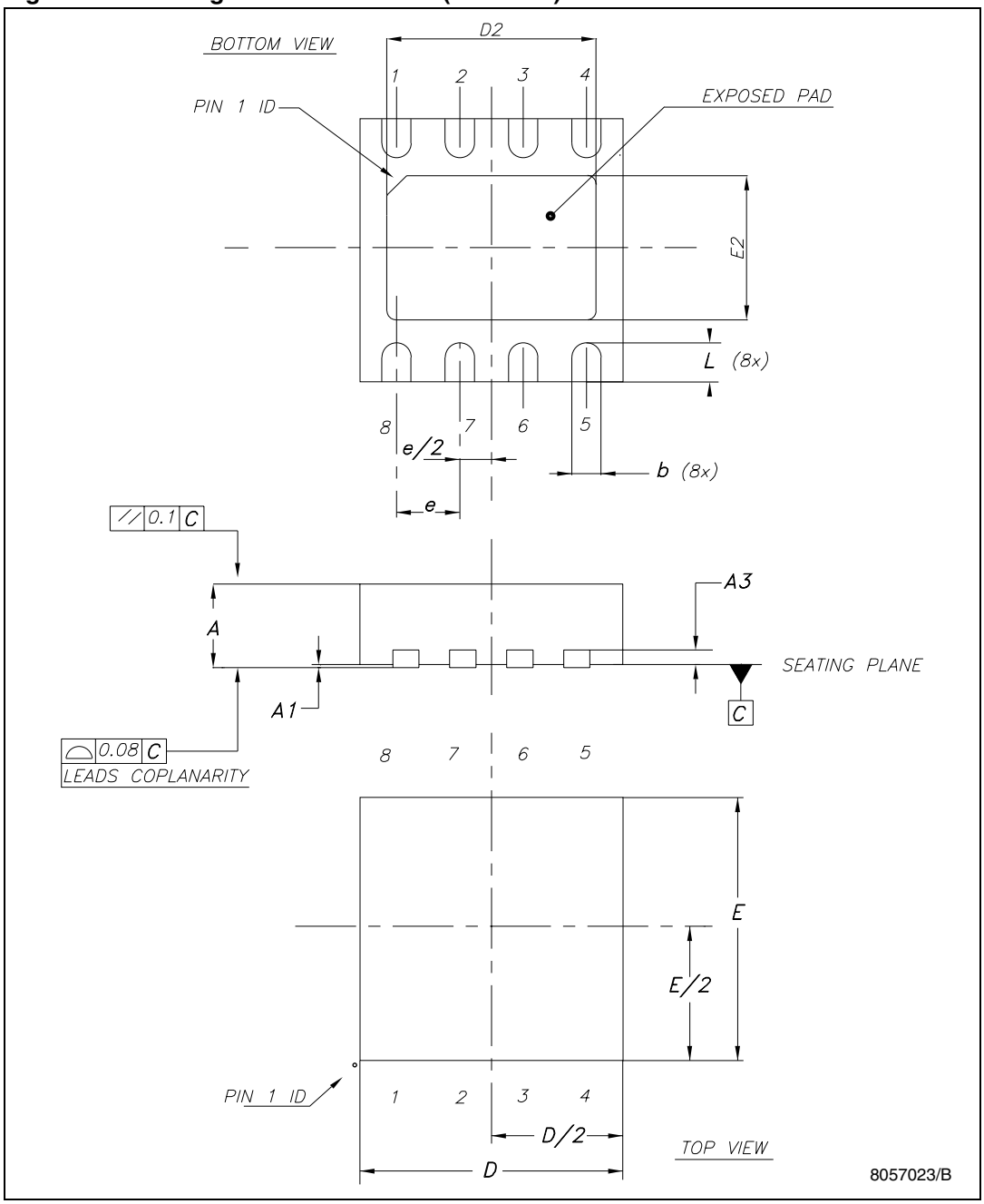
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 7. DFN8 (3 x 3 mm) mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
D		3.00	
D2	2.234	2.384	2.484
E		3.00	
E2	1.496	1.646	1.746
e		0.65	
L	0.30	0.40	0.50

Figure 13. Package dimension DFN8 (3 x 3 mm)



Tape & reel QFNxx/DFNxx (3x3) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.087
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

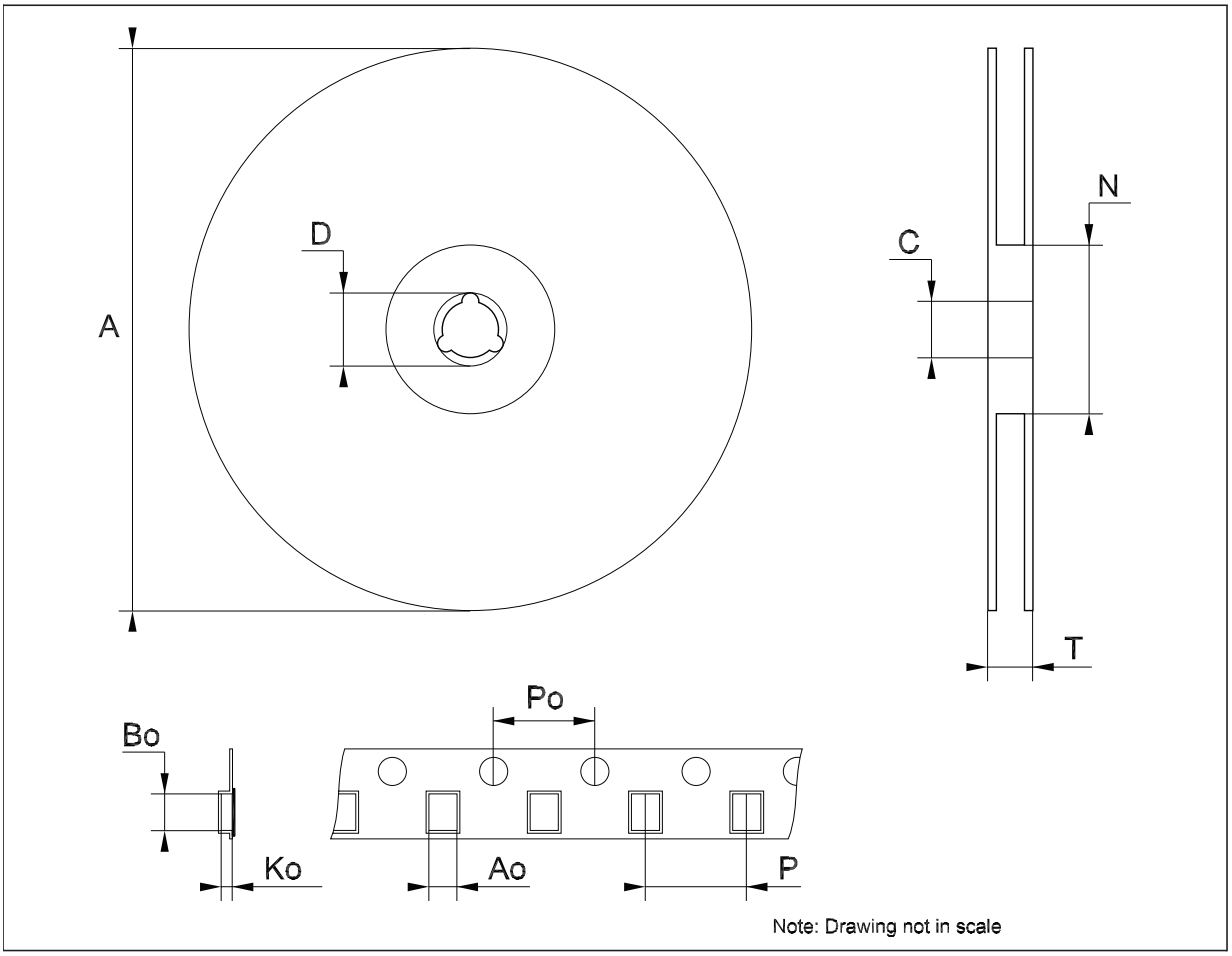
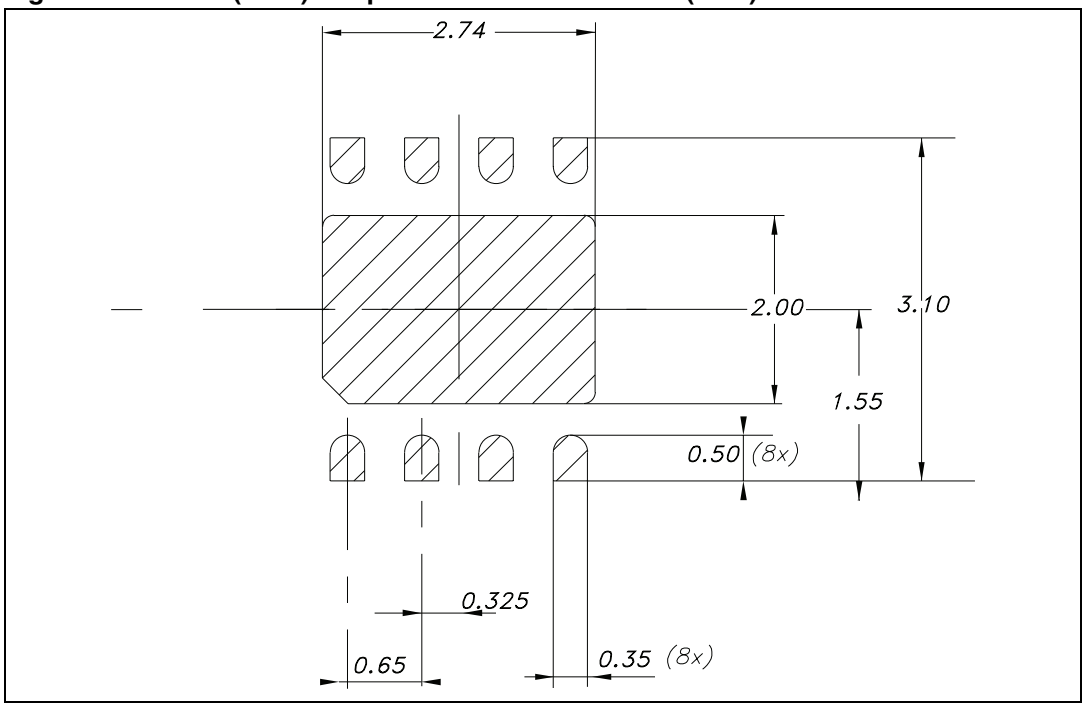


Figure 14. DFN8 (3 x 3) footprint recommended data (mm.)



10 Revision history

Table 8. Document revision history

Date	Revision	Changes
28-Sep-2011	1	Initial release.
16-Nov-2011	2	Change value 1.8 MHz ==> 1.4 MHz*: Features on page 1*.
15-Mar-2012	3	Modified: 1.3 x 0.122 W ==> 1.3 x 0.12^2 W *Section 7.4 on page 10*.
23-May-2012	4	Document status promoted from preliminary data to production data.
27-Jun-2012	5	Added: new L component Coilcraft *Table 5 on page 6*.

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