NL17SZ16

Single Input Buffer

The NL17SZ16 is a single input Buffer in two tiny footprint packages. The device performs much as LCX multi−gate products in speed and drive.

Features

- Tiny SOT−353 and SOT−553 Packages
- Source/Sink 24 mA at 3.0 Volts
- Over−Voltage Tolerant Inputs and Outputs
- Chip Complexity: FETs = 20
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Pb−Free Packages are Available

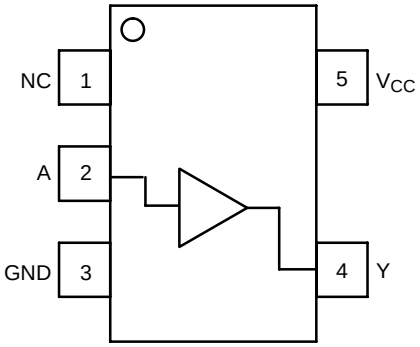


Figure 1. Pinout (Top View)

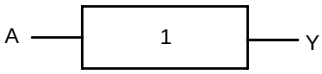


Figure 2. Logic Symbol

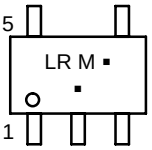
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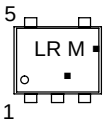


SOT−353/SC70−5/SC−88A
DF SUFFIX
CASE 419A





SOT−553
XV5 SUFFIX
CASE 463B



LR = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

Pin	Function
1	NC
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

A Input	Y Output
L	L
H	H

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_I	DC Input Voltage	Output in High or Low State (Note 2)	$-0.5 \le V_I \le +7.0$	V
V_O	DC Output Voltage	V_I < GND	$-0.5 \le V_O \le +7.0$	V
I_{IK}	DC Input Diode Current	V_O < GND	−50	mA
I_{OK}	DC Output Diode Current		−50	mA
I_{OUT}	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground per Supply Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance	SOT−353 SOT−553	350 360	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOT−353 SOT−553	150 180	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
ESD	ESD Classification	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	Class IC Class A N/A	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 6)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
2. I_O Absolute Maximum Rating Must be Obtained.
3. Tested to EIA/JESD22−A114−A, rated to EIA/JESD22−A114−B.
4. Tested to EIA/JESD22−A115−A, rated to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage	Operations Only Data Retention	1.65 1.5	5.5 5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	5.5	V
T_A	Operating Temperature Range		−40	+85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.5 V ±0.2 V V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	0 0 0	20 10 5	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

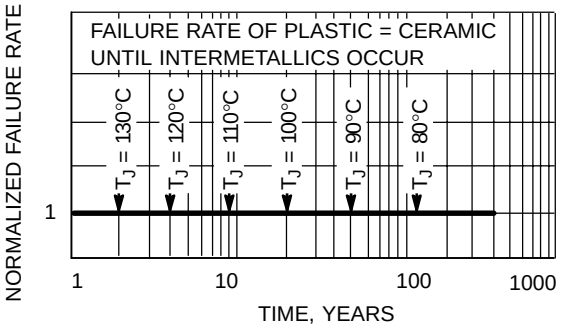


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC}		V
V_{IL}	Low−Level Input Voltage		1.65 to 1.95 2.3 to 5.5			0.25 V_{CC} 0.3 V_{CC}		0.25 V_{CC} 0.3 V_{CC}	V
V_{OH}	High−Level Output Voltage V_{IN} = V_{IL} or V_{IH}	I_{OH} = −100 μA I_{OH} = −3 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V_{CC} 1.52 2.1 2.4 2.7 2.5 4.0		V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8		V
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IH} or V_{OH}	I_{OL} = 100 μA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 12 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.0 0.08 0.20 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I_{OFF}	Power Off−Output Leakage Current	V_{OUT} = 5.5 V	0			1		10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS $t_R = t_F$ = 3.0 ns

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure 4 and 5)	R_L = 1 MΩ, C_L = 15 pF	1.65 1.8 2.5 ± 0.2 3.3 ± 0.3 5.0 ± 0.5	2.0 2.0 0.8 0.5 0.5	5.3 4.4 2.9 2.1 1.8	11.4 9.5 6.5 4.5 3.9	2.0 2.0 0.8 0.5 0.5	12 10 7.0 4.7 4.1	ns
		R_L = 500 Ω, C_L = 50 pF	3.3 ± 0.3 5.0 ± 0.5	1.5 0.8	2.9 2.4	5.0 4.3	1.5 0.8	5.2 4.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	>4	pF
C_{PD}	Power Dissipation Capacitance (Note 7)	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC} 10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	25 30	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

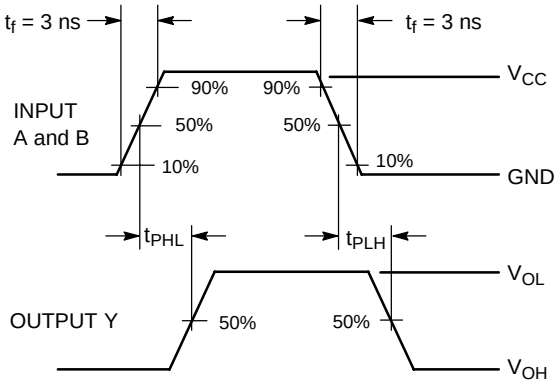
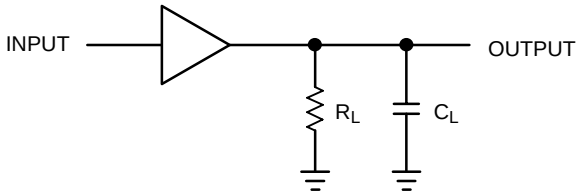


Figure 4. Switching Waveform



A 1−MHz square input wave is recommended for propagation delay tests.

Figure 5. Test Circuit

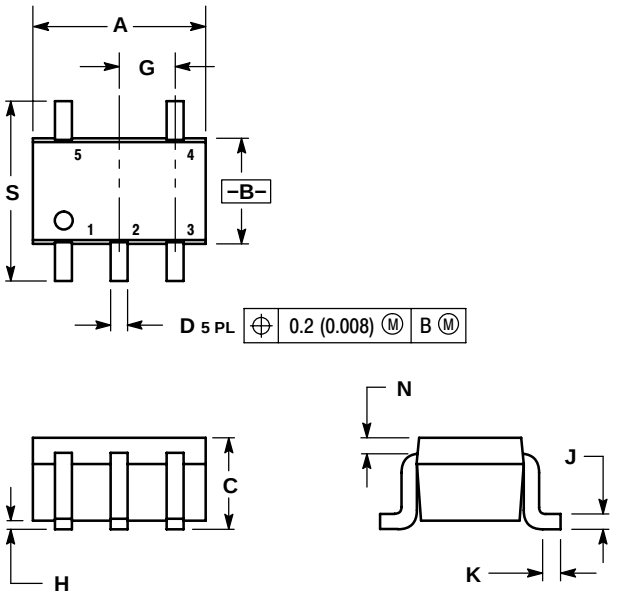
ORDERING INFORMATION

Device	Package	Shipping†
NL17SZ16DFT2	SOT−353/SC70−5/SC−88A	3000/Tape & Reel
NL17SZ16DFT2G	SOT−353/SC70−5/SC−88A (Pb−Free)	
NL17SZ16XV5T2	SOT−553*	4000/Tape & Reel
NL17SZ16XV5T2G	SOT−553*	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*All Devices in Package SOT553 are Inherently Pb−Free.

PACKAGE DIMENSIONS

SC−88A, SOT−353, SC−70
CASE 419A−02
ISSUE J

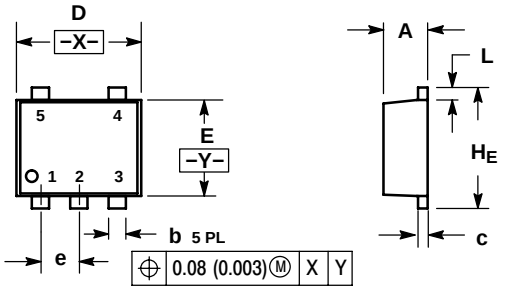


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

PACKAGE DIMENSIONS

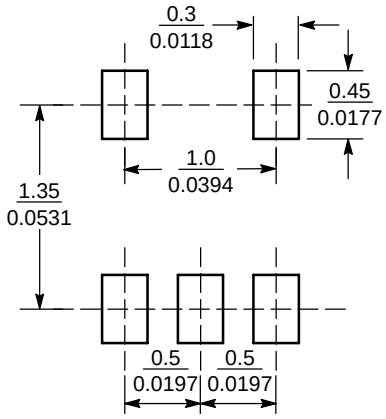
SOT−553, 5 LEAD
CASE 463B−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e		0.50 BSC			0.020 BSC	
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.063	0.067

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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