

Actual Size
3 mm x 3 mm



SLVS530B – SEPTEMBER 2005 – REVISED NOVEMBER 2007

# DC-DC INVERTER

## FEATURES

- **Adjustable Output Voltage Down to –15 V**
- **2.7-V to 5.5-V Input Voltage Range**
- **Up to 360-mA Output Current**
- **1000-mA Typical Switch Current Limit**
- **Up to 84% Efficiency**
- **Typical 1.4-MHz Fixed-Frequency PWM Operation**
- **Thermal Shutdown**
- **Typical –19 V Output Overvoltage Protection**
- **1.5-μA Shutdown Current**
- **Small 3-mm × 3-mm SON-10 Package (DRC)**

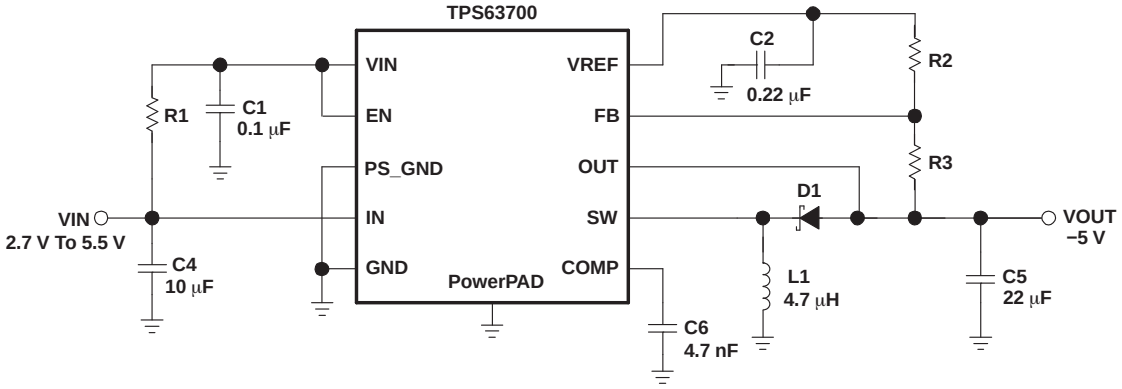
## APPLICATIONS

- **Generic Negative Voltage Supply**
- **Small-to-Medium Size OLED Displays**
- **PDAs, Pocket PCs, Smartphones**
- **Bias Supply**

## DESCRIPTION

The TPS63700 is an inverting dc-dc converter generating a negative output voltage down to –15 V with output currents up to 360-mA, depending on input-voltage to output-voltage ratio. With a total efficiency up to 84%, the device is ideal for portable battery-powered equipment. The input voltage range of 2.7-V to 5.5-V allows the TPS63700 to be directly powered from a Li-ion battery, from 3-cell NiMH/NiCd, from a 3.3-V or 5-V supply rail. The TPS63700 comes in a small 3-mm × 3-mm SON-10 package. Furthermore, the high switching frequency of typically 1.4 MHz allows the use of small external components. This, and the small package make a small power supply solution possible.

The inverter operates with a fixed-frequency PWM control topology. The device has an internal current limit, overvoltage protection, and a thermal shutdown for highest reliability under fault conditions.




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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| $T_A$ | SWITCH CURRENT LIMIT | PACKAGE TYPE | SYMBOL | PART NUMBER(2) |
|---|---|---|---|---|
| –40°C to 85°C | 1000 mA | SON-10 | NUB | TPS63700DRC |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) The DRC package is available taped and reeled. Add an R suffix to the device type (i.e., TPS63700DRCR) to order quantities of 3000 devices per reel. Add a T suffix to the device type (i.e., TPS63700DRCT) to order quantities of 250 devices peer reel.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | TPS63700 |
|---|---|
| Input voltage range at VIN(2) | –0.3 V to +6.0 V |
| Input voltage range at IN(2) | VIN |
| Minimum voltage at VOUT (2) | –18 V |
| Voltage at EN, FB, COMP, PS (2) | –0.3 V to $V_{IN}$ + 0.3 V |
| Differential voltage between OUT to $V_{IN}$(2) | 24 V |
| Operating virtual junction temperature, $T_J$ | –40°C to 150°C |
| Storage temperature range, $T_{STG}$ | –65°C to 150°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

## DISSIPATION RATINGS TABLE(1)

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| DRC | 2053 mW | 21 mW/°C | 1130 mW | 821 mW |

(1) The thermal resistance junction to ambient of the 10-pin DRC is $\Theta_{JA}$ = 48.7 °C/W. Exceeding the maximum junction temperature forces the device into thermal shutdown.

## RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Input voltage range, $V_I$ | 2.7 | | 5.5 | V |
| Operating free-air temperature range, $T_A$ | –40 | | 85 | °C |
| Operating virtual junction temperature range, $T_J$ | –40 | | 125 | °C |


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## ELECTRICAL CHARACTERISTICS

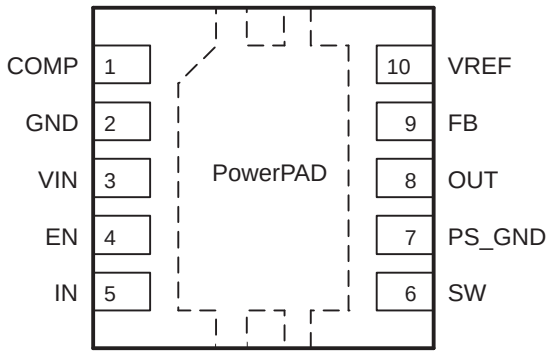
–40°C to 85°C, over recommended input voltage range, typical at an ambient temperature of 25°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DC-DC STAGE** | | | | | | | |
| $V_{OUT}$ | Adjustable output voltage range | | | –15 | | –2 | V |
| $V_{IN}$ | Input voltage range | | PIN VIN, IN | 2.7 | | 5.5 | V |
| $V_{REF}$ | Reference voltage | | $I_{REF}$ = 10 µA | 1.2 | 1.213 | 1.225 | V |
| $I_{FB}$ | Negative feedback input bias current | | $V_{FBN}$ = 0.1 $V_{REF}$ | | 2 | | nA |
| $V_{FB}$ | Negative feedback regulation voltage | | $V_{IN}$ = 2.7 V to 5.5 V | –0.024 | 0 | 0.024 | V |
| $V_{OUT}$ | DC output accuracy | | PWM mode, device switching, | | ±3 | | % |
| $V_{OVP}$ | Output overvoltage protection | | | | –19 | | V |
| $R_{DS(ON)}$ | Inverter switch on-resistance | | $V_{IN}$ = 3.6 V | | 440 | 600 | mΩ |
| | | | $V_{IN}$ = 5 V | | 370 | 500 | |
| $I_{LIM}$ | Inverter switch current limit | | 2.7 V < $V_{IN}$ < 5.5 V | 860 | 1000 | 1140 | mA |
| $D_{MAX}$ | Maximum duty cycle inverting converter | | | | 87.5% | | |
| $D_{MIN}$ | Minimum duty cycle inverting converter | | | | 12.5% | | |
| **CONTROL STAGE** | | | | | | | |
| $f_S$ | Oscillator frequency | | | 1250 | 1380 | 1500 | kHz |
| $V_{EN}$ | High level input voltage | | | 1.4 | | | V |
| $V_{EN}$ | Low level input voltage | | | | | 0.4 | V |
| $I_{EN}$ | Input current | | EN = $V_{IN}$ or GND | | 0.01 | 0.1 | µA |
| $I_{(Q)}$ | Quiescent current | VIN | $V_{IN}$ = 3.6 V, $I_{OUT}$ = 0, EN = $V_{IN}$, no switching $V_{OUT}$ = –5 V | | 330 | 400 | µA |
| | | IN | | | 640 | 750 | µA |
| $I_{SD}$ | Shutdown supply current | | EN = GND | | 0.2 | 1.5 | µA |
| UVLO | Undervoltage lockout threshold | | | 2.1 | 2.35 | 2.7 | V |
| | Thermal shutdown | | | | 150 | | °C |
| | Thermal shutdown hysteresis | | Junction temperature decreasing | | 5 | | °C |

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## PIN ASSIGNMENTS

**DRC PACKAGE PowerPAD™**
**(TOP VIEW)**

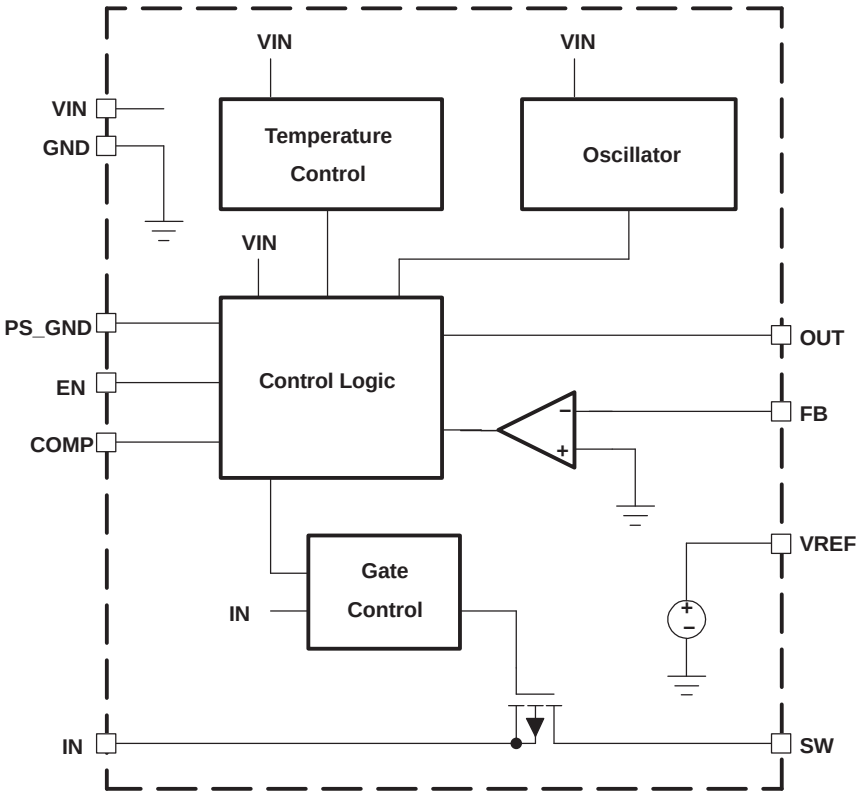



### Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| COMP | 1 | I/O | Compensation pin for control, connect a 4.7nF capacitor between this pin and GND |
| EN | 4 | I | Enable pin (EN=GND: disabled; EN=VIN: enabled) |
| FB | 9 | I | Feedback pin for the voltage divider |
| GND | 2 | | Ground pin |
| IN | 5 | I | supply voltage for the power switch |
| OUT | 8 | I | Output voltage sense input |
| PS_GND | 7 | I | Connect to GND for control logic |
| SW | 6 | O | Inverter switch output |
| VIN | 3 | I | supply voltage input for control logic, connect a RC circuit of 10R and 100nF to filter this supply voltage |
| VREF | 10 | O | Reference voltage output. Connect a 220-nF capacitor to ground. Connect the lower resistor of the negative output voltage divider to this pin. |

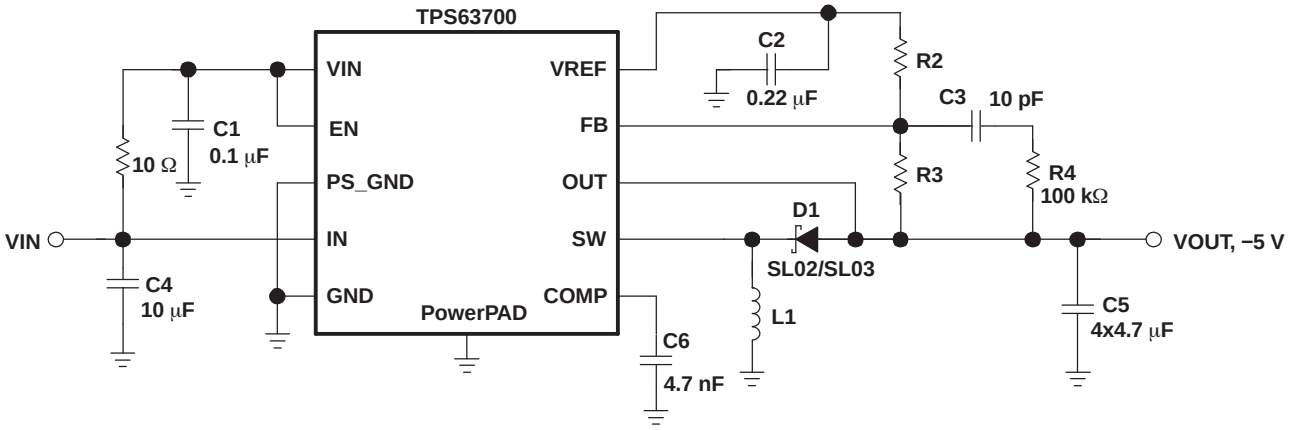

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## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS

## PARAMETER MEASUREMENT INFORMATION




### List of Components

| REFERENCE | DESCRIPTION |
|---|---|
| C1, C2, C3, C4, | X7R/X5R ceramic |
| C5 | 4 × 4.7 µF X7R/X5R ceramic |
| D1 | SL03/SL02 Vishay |
| L1 | –5V: TDK VLF4012 4R7, TDK SLF6025-4R7, Coilcraft LPS4018-472, |
| | –12V: Sumida CDRH5D18 10 µH |


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## Table of Graphs

| GRAPH | DESCRIPTION |
|---|---|
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| Figure 3 | Efficiency versus output current, $V_{OUT}$ = –12 V |
| Figure 4 | Efficiency versus output current, $V_{OUT}$ = –15V |
| Figure 5 | Efficiency versus input voltage, $V_{OUT}$ = –5 V |
| Figure 6 | Efficiency versus input voltage, $V_{OUT}$ = –12 V |
| Figure 7 | Output voltage versus output current, $V_{OUT}$ = –5 V |
| Figure 8 | Output voltage versus output current, $V_{OUT}$ = –12 V |
| Figure 9 | Output voltage in discontinuous conduction mode, $V_{IN}$= 3.6 V, $V_{OUT}$ = –5 V |
| Figure 10 | Output voltage in continuous conduction mode, $V_{IN}$= 3.6 V, $V_{OUT}$ = –5 V |
| Figure 11 | Load transient response, $V_{IN}$= 3.6 V, $V_{OUT}$ = –5 V, 45 to 150 mA |
| Figure 12 | Line transient response, $V_{IN}$= 3.6 V to 4.2 V, $V_{OUT}$ = –5 V |
| Figure 13 | Start-up after enable,$V_I$ = 3.6 V, $V_{OUT}$ = –5 V |

## PERFORMANCE GRAPHS

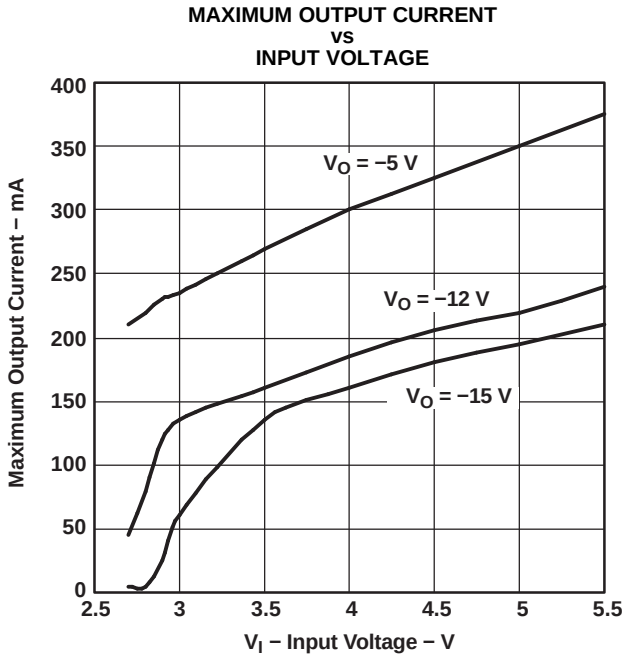



Figure 1.

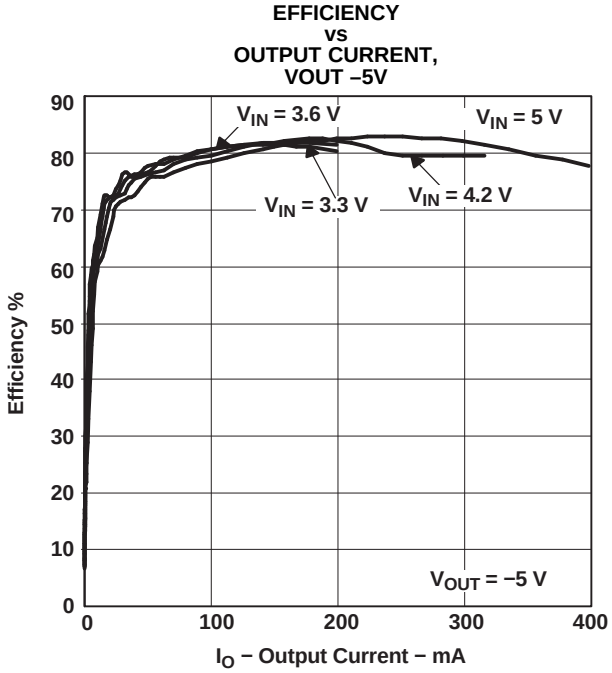



Figure 2.

## PERFORMANCE GRAPHS (continued)

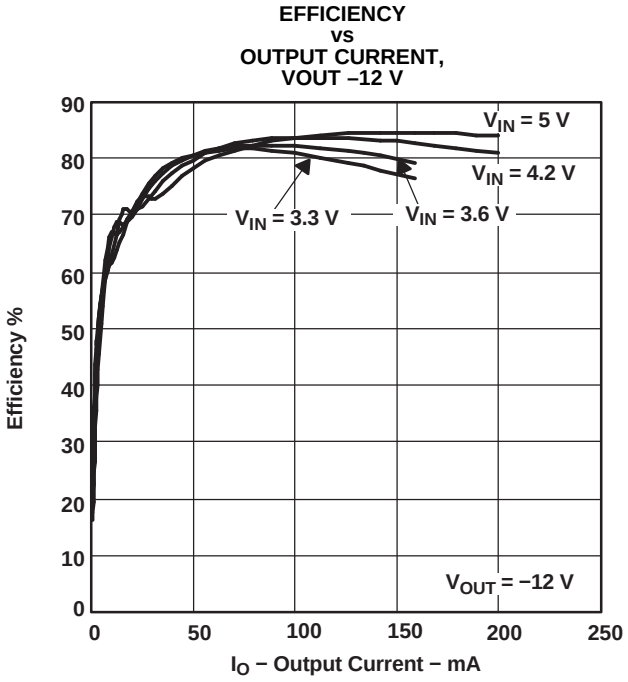



Figure 3.

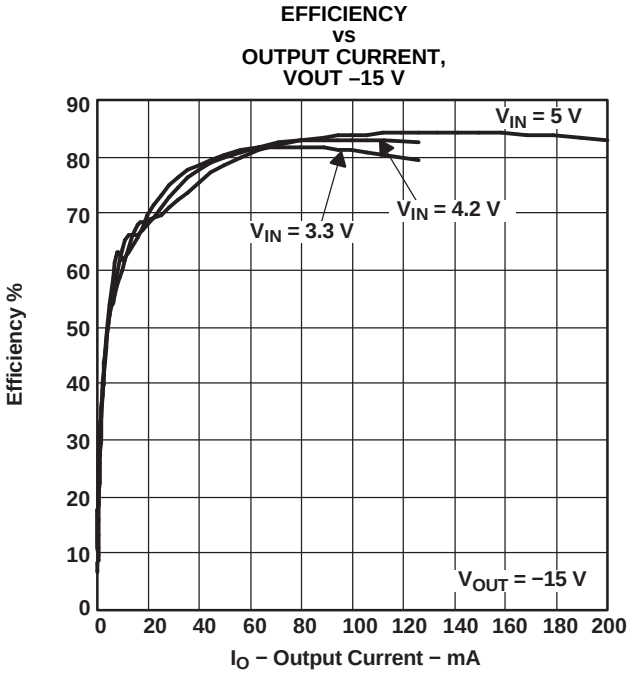



Figure 4.

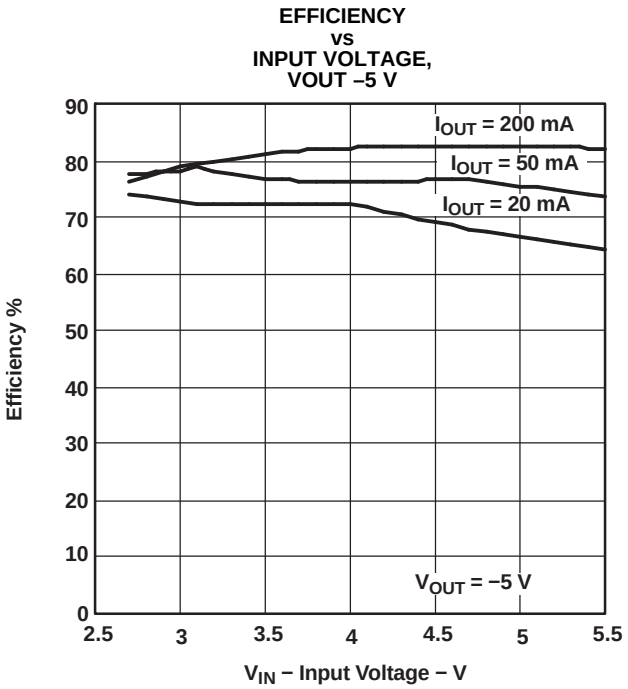



Figure 5.

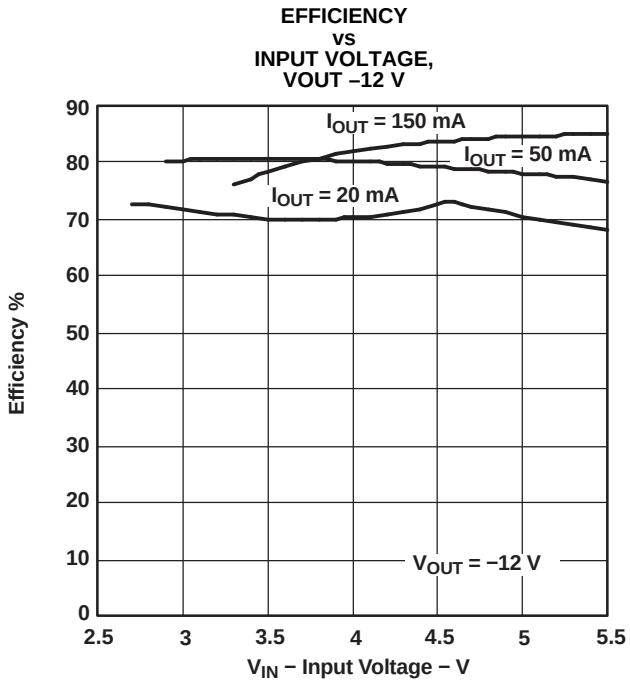



Figure 6.


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## PERFORMANCE GRAPHS (continued)

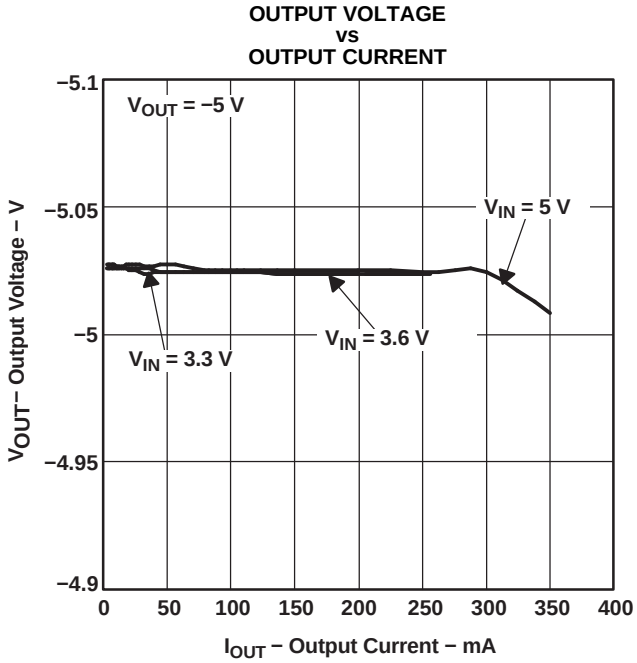



Figure 7.

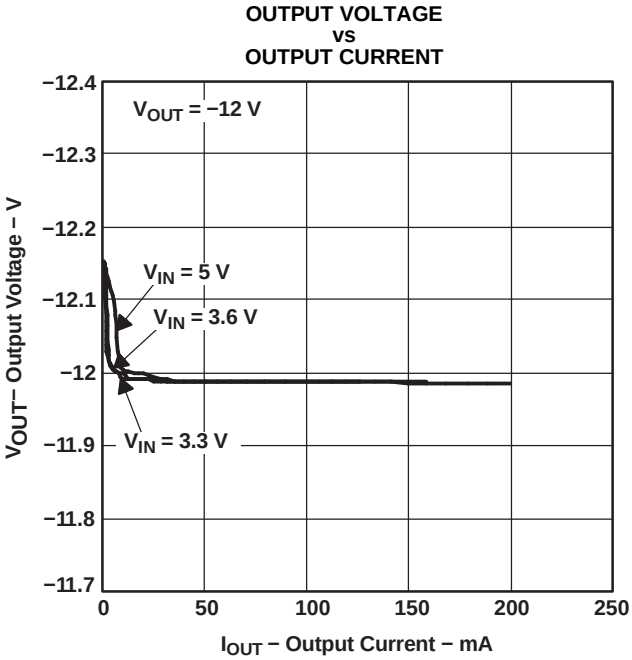



Figure 8.

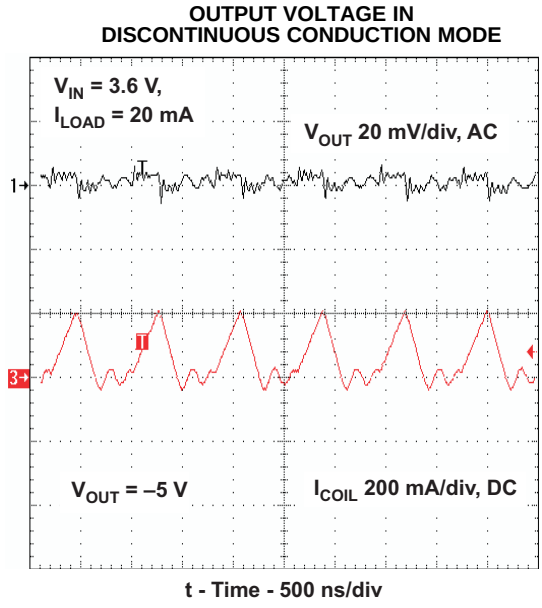



Figure 9.

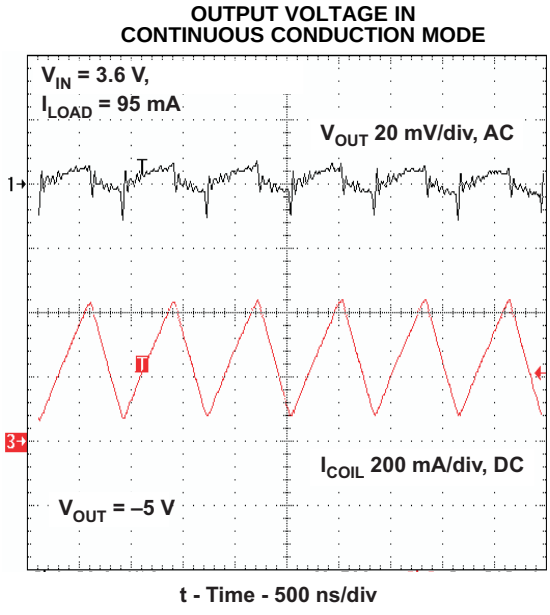
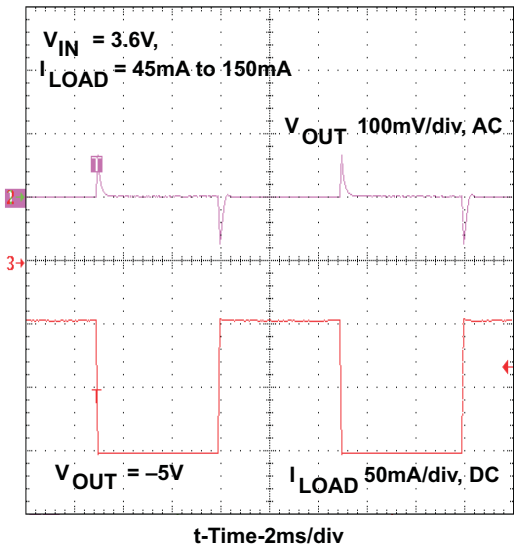



Figure 10.

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## PERFORMANCE GRAPHS (continued)

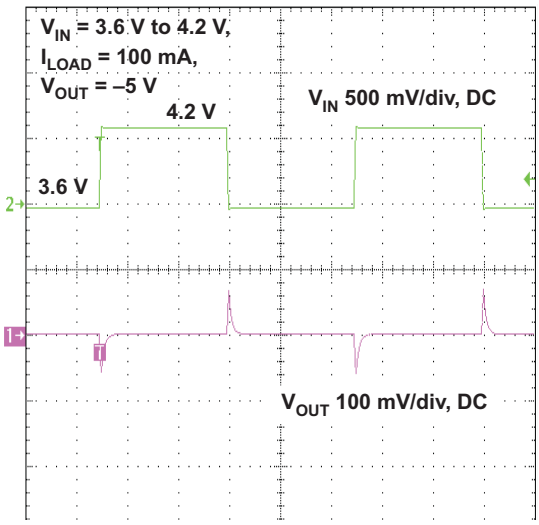
LOAD TRANSIENT RESPONSE,
–5 V, 45 TO 150 mA




t-Time-2ms/div

Figure 11.

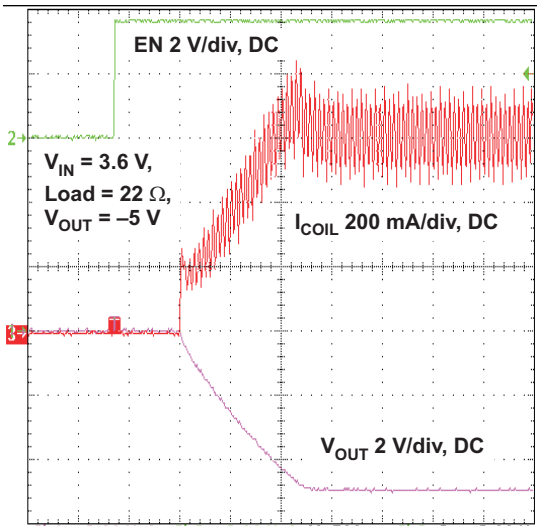
LINE TRANSIENT RESPONSE, –5 V




t - Time - 2 ms/div

Figure 12.

START-UP AFTER ENABLE, –5 V




t - Time - 500 µs/div

Figure 13.


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## DETAILED DESCRIPTION

The TPS63700 is a dc-dc converter for negative output voltages using buck-boost topology. It operates with an input voltage range of 2.7 V to 5.5 V and generates a negative output voltage down to –15 V. The output is controlled by a fixed-frequency, pulse-width-modulated (PWM) regulator. In normal operation mode, the converter operates at continuous conduction mode (CCM). At light loads it can enter discontinuous conduction mode (DCM).

### Power Conversion

The converter operates in a fixed-frequency, pulse-width-modulated control scheme. So, the on-time of the switches varies depending on input-to-output voltage ratio and the load. During this on-time, the inductor connected to the converter is charged with current. In the remaining time, the time period set by the fixed operating frequency, the inductor discharges into the output capacitor via the rectifier diode. Usually, at higher loads the inductor current is continuous. During light load, the inductor current of this converter can become discontinuous. In this case, the control circuit of the controller output automatically takes care of these changing conditions to always operate with an optimum control setup.

### Control

The controller circuit of the converter is based on a fixed-frequency, multiple-feedforward controller topology. Input voltage, output voltage, and voltage drop across the switch are monitored and forwarded to the regulator. Changes in the operating conditions of the converter directly affect the duty cycle.

The error amplifier compares the voltage on FB pin with GND to generate an accurate and stable output voltage. The error amplifier is internally compensated. At light loads, the converter operates in discontinuous conduction mode (DCM).

If the load will be further decreased, the energy transmitted to the output capacitor can't be absorbed by the load and would lead to an increase of the output voltage. In this case, the converter limits the output voltage increase by skipping switch pulses.

### Enable

Applying GND signal at the EN pin disables the converter, where all internal circuitry is turned off. The device now just consumes low shutdown current flowing into the VIN pin. The output load of the converter is also disconnected from the battery as described in the following paragraph. Pulling the EN pin to $V_{IN}$ enables the converter. Internal circuitry, necessary to operate the converter, is then turned on.

### Load Disconnect

The device supports complete load disconnection when the converter is disabled. The converter turns off the internal PMOS switch, thus no DC current path remains between load and input voltage source.

### Soft Start

The converter has a soft-start function. When the converter is enabled, the implemented switch current limit ramps up slowly to its nominal value. Soft start is implemented to limit the input current during start-up to avoid high peak currents at the battery which could interfere with other systems connected to the same battery.

Without soft start, uncontrolled input peak currents flow to charge up the output capacitors and to supply the load during start-up. This would cause significant voltage drops across the series resistance of the battery and its connections.

### Output Overvoltage Protection

The converter has an implemented output overvoltage protection. The output voltage is limited to –19 V in case the feedback connection from the output to the FB pin is open.

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## Undervoltage Lockout

An undervoltage lockout prevents the device from starting up and operating if the supply voltage at VIN is lower than the programmed threshold shown in the electrical characteristics table. The device automatically shuts down the converter when the supply voltage at VIN falls below this threshold. Nevertheless, parts of the control circuits remain active, which is different than device shutdown using EN inputs. The undervoltage lockout function is implemented to prevent device malfunction.

## Overtemperature Shutdown

The device automatically shuts down if the implemented internal temperature detector detects a chip temperature above the programmed threshold shown in the electrical characteristics table. It starts operating again when the chip temperature decreases. A built-in temperature hysteresis avoids undefined operation caused by ringing from overtemperature shutdown.


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## APPLICATION INFORMATION

### Design Procedure

The TPS63700 dc-dc converter is intended for systems typically powered by a single-cell Li-ion or Li-polymer battery with a terminal voltage between 2.7 V up to 4.2 V. Due to the recommended input voltage going up to 5.5 V, the device is also suitable for 3-cell alkaline, NiCd, or NiMH batteries, as well as regulated supply voltages of 3.3 V or 5 V.

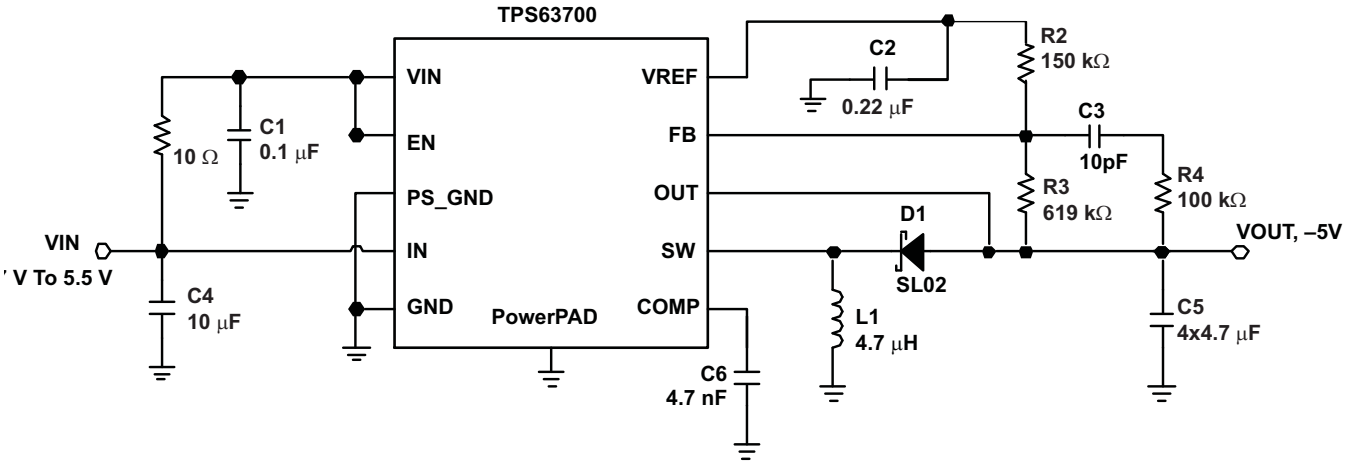



**Figure 14. Circuit for –5 Volt Output**

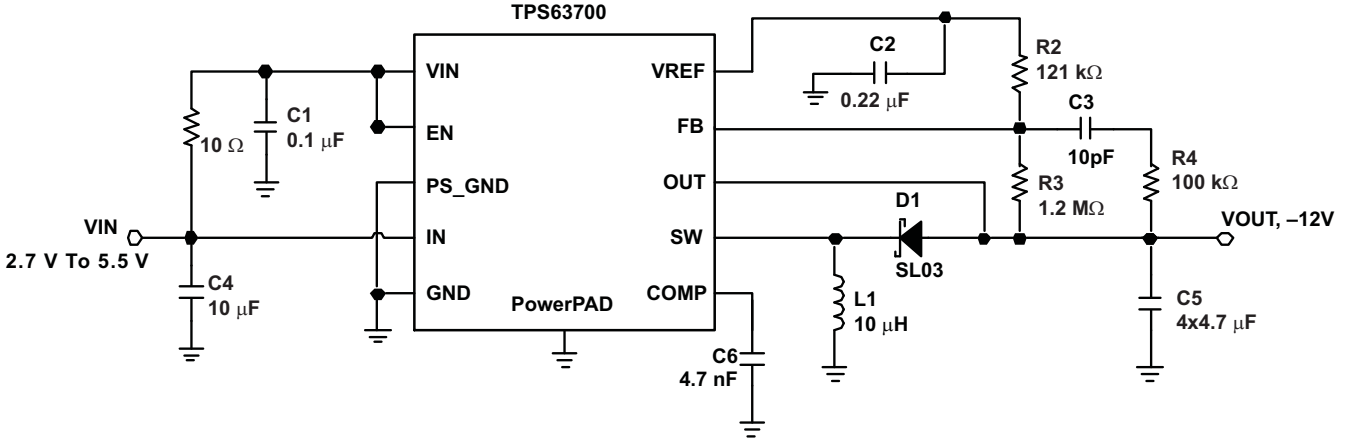



**Figure 15. Circuit for –12 Volt Output**

### Programming the Output Voltage

#### *Converter*

The output voltage of the TPS63700 converter can be adjusted with an external resistor divider connected to the FB pin. The reference point of the feedback divider is the reference voltage VREF with 1.213 V. The typical value of the voltage at the FB pin is 0 V. The minimum recommended output voltage at the converter is –15 V. The feedback divider current should be 10 µA. The voltage across R2 is 1.213 V. Based on those values, the recommended value for R2 should be 120 kΩ to 200 kΩ in order to set the divider current at the required value. The value of the resistor R3 can then be calculated using Equation 1, depending on the needed output voltage ($V_{OUT}$):

$$R3 = R2 \times \left( \frac{V_{REF} - V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

For example, if an output voltage of –5 V is needed and a resistor of 150 kΩ has been chosen for R2, a 680-kΩ resistor is needed to program the desired output voltage.

### Inductor Selection

An inductive converter normally requires two main passive components for storing energy during the conversion. An inductor and a storage capacitor at the output are required.

The average inductor current depends on the output load, the input voltage (VIN), and the output voltage VOUT. It can be estimated with Equation 2, which shows the formula for the inverting converter.

$$I_{Lavg} = \frac{V_{IN} - V_{OUT}}{V_{IN} \times 0.8} \times I_{OUT} \quad (2)$$

with:

$I_{Lavg}$= average inductor current

An important parameter for choosing the inductor is the desired current ripple in the inductor.

A ripple current value between 20% and 80% of the average inductor current can be considered as reasonable, depending on the application requirements. A smaller ripple reduces the losses in the inductor, as well as output voltage ripple and EMI. But in the same way, the inductor becomes larger and more expensive.

Keeping those parameters in mind, the possible inductor value can be calculated using Equation 3.

$$L = \frac{V_{IN} \times V_{OUT}}{\Delta I_L \times \left( V_{OUT} - V_{IN} \right) \times f} \quad (3)$$

with:

$\Delta I_L$ = peak-to-peak ripple current

f = switching frequency

L = inductor value

With the known inductor current ripple, the peak inductor value can be approximated with Equation 4. The peak current through the switch and the inductor depends also on the output load, the input voltage (VIN), and the output voltage (VOUT). To select the right inductor, it is recommended to keep the possible peak inductor current below the current-limit threshold of the power switch. For example, the current-limit threshold of the TPS63700 switch for the inverting converter is nominally 1000 mA.

$$I_{Lmax} = \frac{V_{IN} - V_{OUT}}{V_{IN} \times 0.8} \times I_{OUT} + \frac{\Delta I_L}{2} \quad (4)$$

with:

$I_{LMAX}$ = peak inductor current

With Equation 5, the inductor current ripple at a given inductor can be approximated.

$$\Delta I_L = \frac{V_{IN} \times V_{OUT}}{L \times \left( V_{OUT} - V_{IN} \right) \times f} \quad (5)$$

Care has to be taken for the possibility that load transients and losses in the circuit can lead to higher currents as estimated in Equation 4. Also, the losses caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.


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The following inductor series from different suppliers have been tested with the TPS63700 converter:

**List of Inductors**

| Output Voltage | Vendor | SUGGESTED INDUCTOR |
|---|---|---|
| –5V | TDK | VLF4012 4.7 µH |
| | | SLF6025-4.7 µH |
| –5V | Coilcraft | LPS4018 4.7 µH |
| | | LPS3015 4.7 µH |
| –12V | Sumida | CDRH5D18 10 µH |
| –12V | Coilcraft | MOS6020 10 µH |

## Capacitor Selection

### Input Capacitor

At least a 10-µF ceramic input capacitor is recommended for a good transient behavior of the regulator, and EMI behavior of the total power supply circuit.

### Output Capacitors

One of the major parameters necessary to define the capacitance value of the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 6 for the inverting converter output capacitor.

$$C_{min} = \frac{I_{OUT} \times V_{OUT}}{f_S \times \Delta V \times \left(V_{OUT} - V_{IN}\right)} \quad (6)$$

Parameter *f* is the switching frequency and *ΔV* is the maximum allowed ripple.

With a chosen ripple voltage in the range of 10 mV, a minimum capacitance of 12 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 7 .

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (7)$$

An additional ripple of 2 mV is the result of using a typical ceramic capacitor with an ESR in a 10-mΩ range. The total ripple is the sum of the ripple caused by the capacitance, and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 12 mV. Additional ripple is caused by load transients. When the load current increases rapidly, the output capacitor must provide the additional current until the inductor current has been increased by the control loop by setting a higher on-time at the main switch (duty cycle). The higher duty cycle results in longer inductor charging periods. But the rate of increase of the inductor current is also limited by the inductance itself. When the load current decreases rapidly, the output capacitor needs to store the excessive energy (stored in the inductor) until the regulator has decreased the inductor current by reducing the duty cycle. The recommendation is to use higher capacitance values, as the previous calculations show.

### Stabilizing the Control Loop

#### *Feedback Divider*

To speed up the control loop, a feedforward capacitor of 10 pF is recommended in the feedback divider, parallel to R3.

To avoid coupling noise into the control loop from the feedforward capacitor, the feedforward effect can be bandwidth-limited by adding series resistor R4. A value in the range of 100 kΩ is suitable. The higher the resistance, the lower the noise coupled into the control loop system.

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### *Compensation Capacitor*

The control loop of the converter is completely compensated internally. However the internal feedforward system requires an external capacitor. A 4.7-nF capacitor at the COMP pin of the converter is recommended.

### Layout Considerations

For all switching power supplies the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths, and for the power-ground tracks. The input and output capacitors should be placed as close as possible to the IC. The diode need to be connected closest to the SW PIN to minimize parasitic inductance. For low noise operation small bypass capacitors $C_{IN\ BP}$ and $C_{OUT\ BP}$ in the nF range can be added close to the IC.

The feedback divider should be placed as close as possible to the VREF pin of the IC. Use short traces when laying out the control ground. Figure 18 shows the layout of the EVM board.

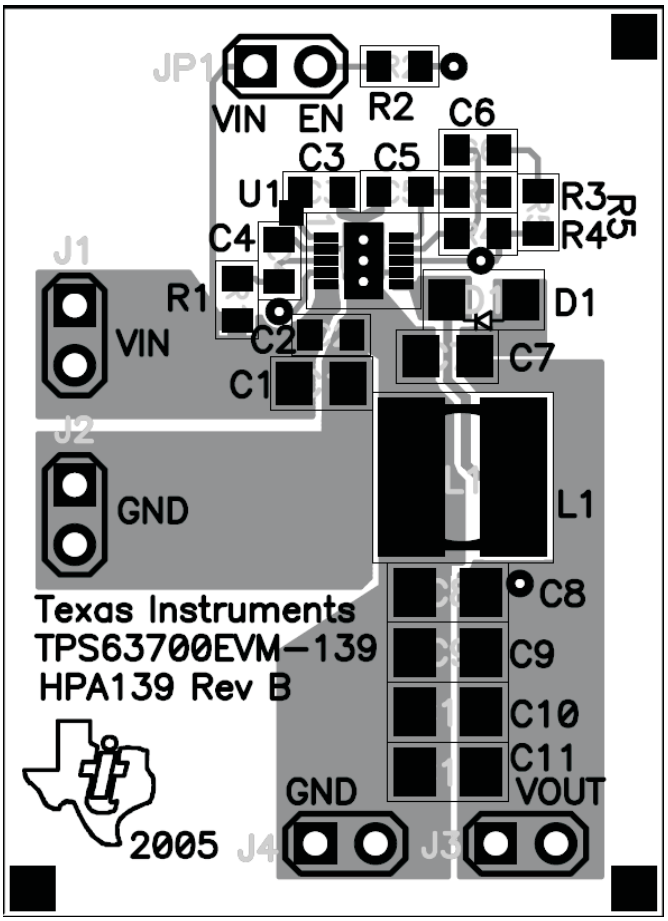



**Figure 16. Layout Considerations, Top View**


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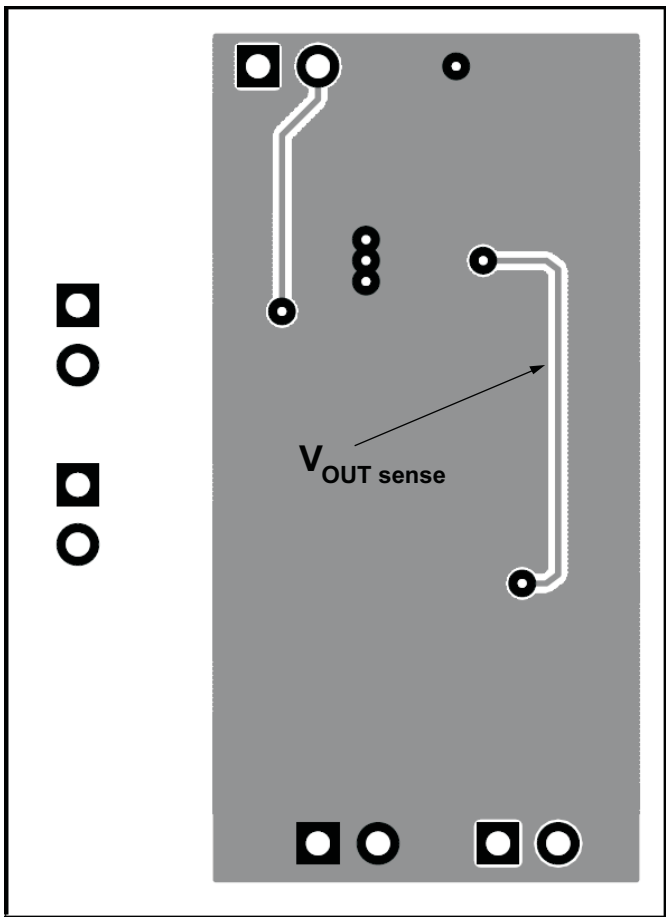



**Figure 17. Layout Considerations, Bottom View**

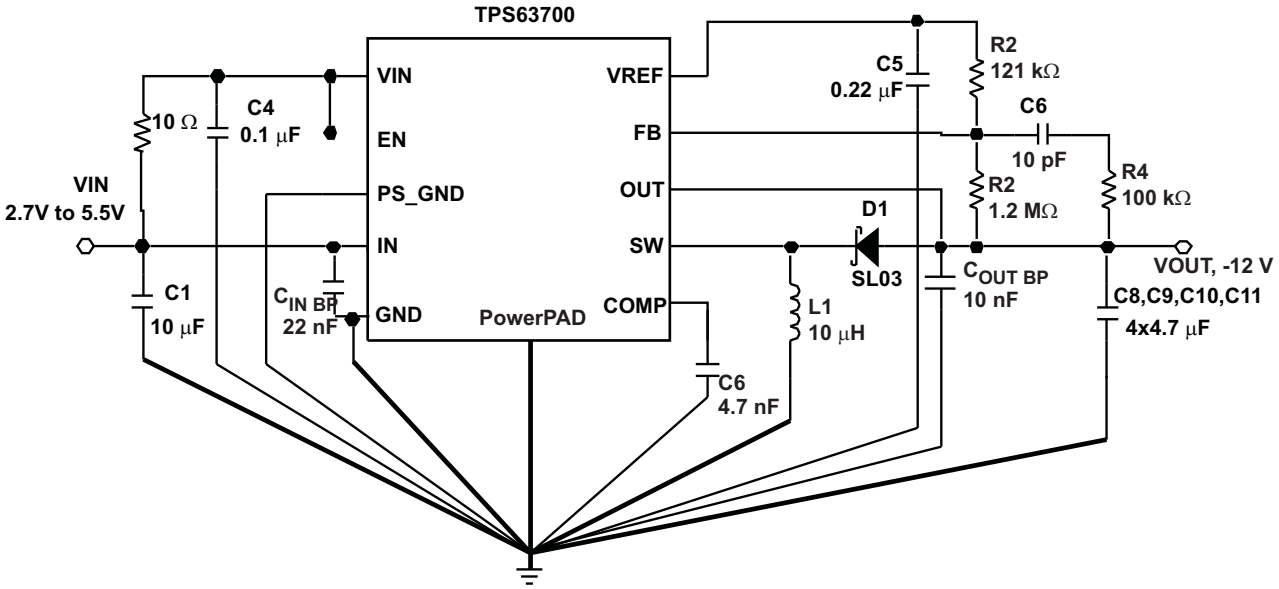



**Figure 18. Layout Circuit**

## THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues, such as thermal coupling, airflow, added heatsinks and convection surfaces, and the presence of heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow to the system

The maximum recommended junction temperature ($T_J$) of the TPS63700 device is 125°C. The thermal resistance of the 10-pin SON, 3 × 3-mm package (DRC) is $R_{JA}$ = 48.7°C/W. Specified regulator operation is ensured to a maximum ambient temperature $T_A$ of 85°C. Therefore, the maximum power dissipation is about 821 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{R_{\theta JA}} \quad (8)$$


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TPS63700DRCR | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS63700DRCRG4 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS63700DRCT | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS63700DRCTG4 | ACTIVE | SON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

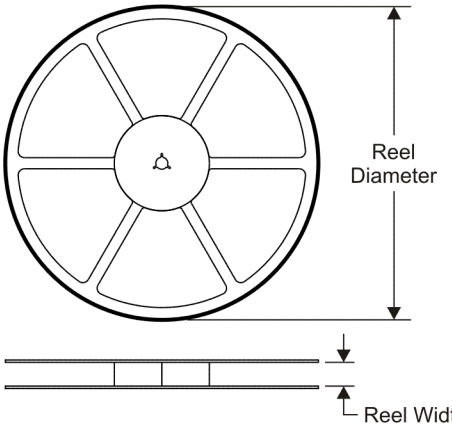
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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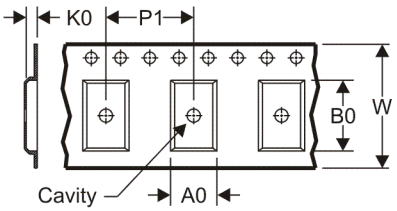
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**REEL DIMENSIONS**

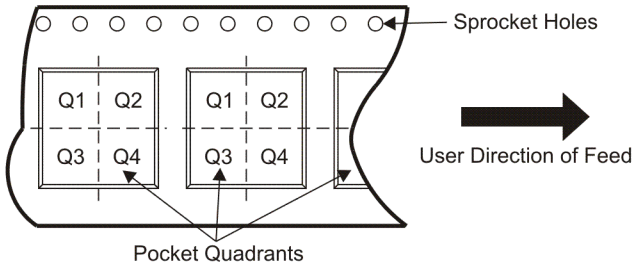



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

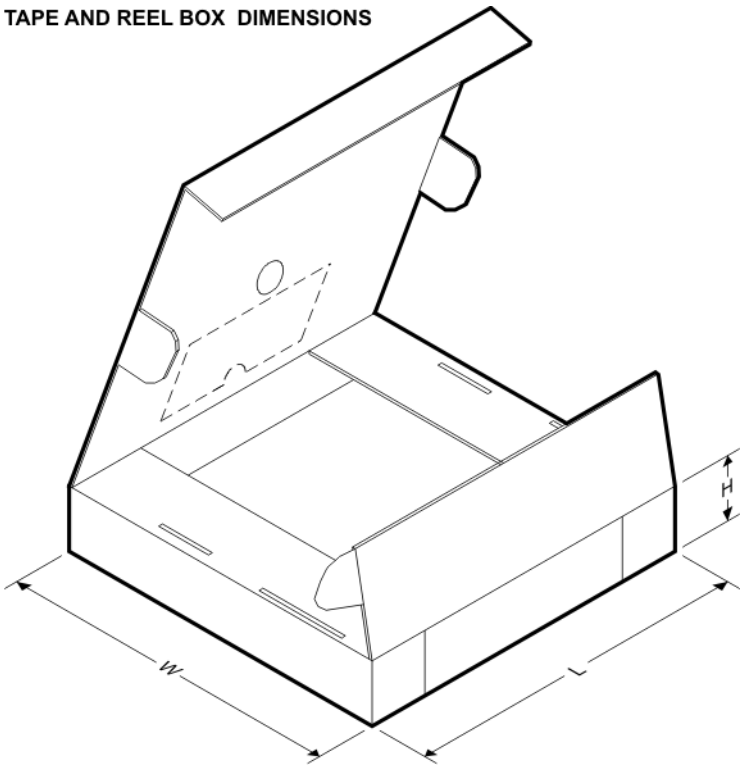
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS63700DRCR | SON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS63700DRCT | SON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

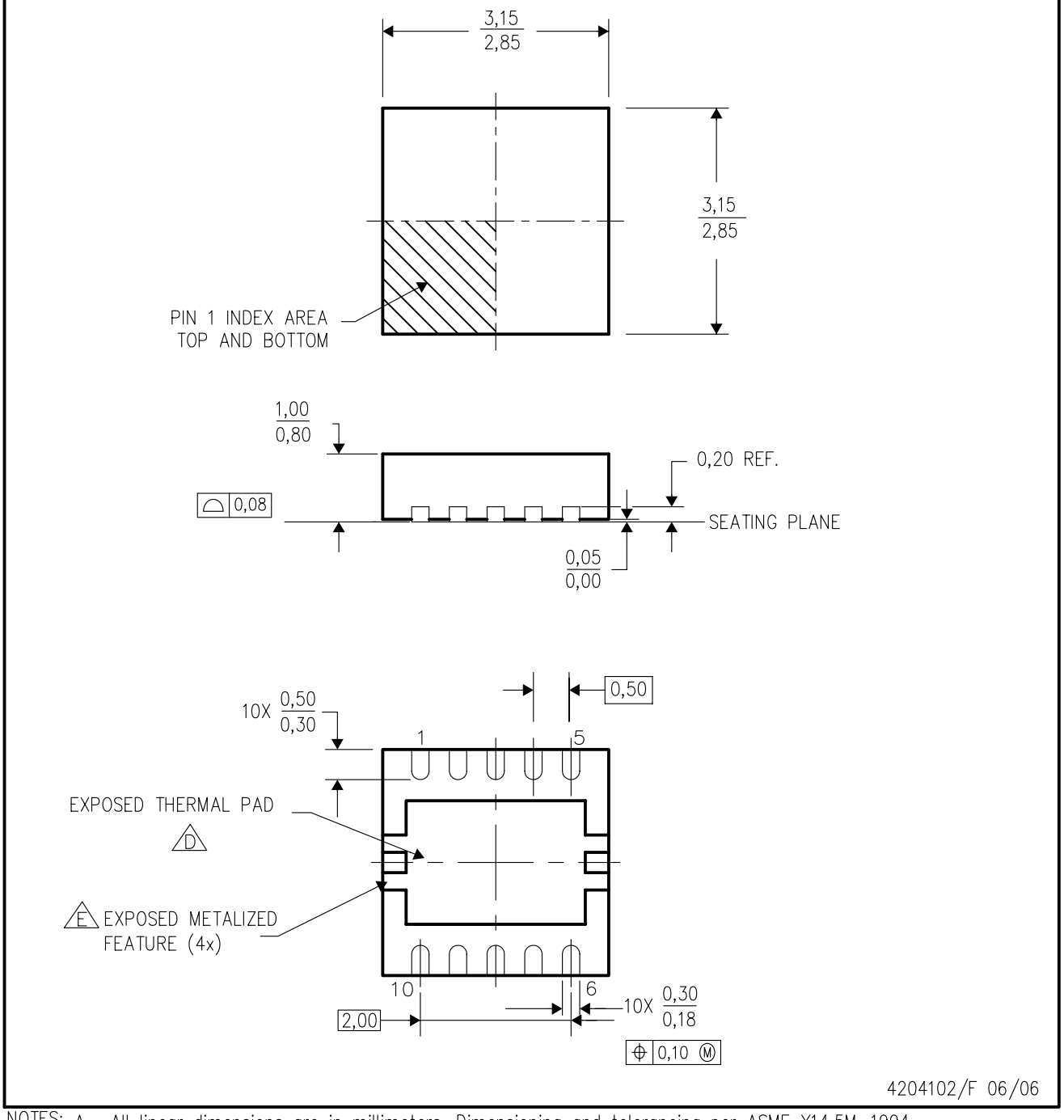
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS63700DRCR | SON | DRC | 10 | 3000 | 346.0 | 346.0 | 29.0 |
| TPS63700DRCT | SON | DRC | 10 | 250 | 190.5 | 212.7 | 31.8 |

DRC (S–PDSO–N10) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

# THERMAL PAD MECHANICAL DATA

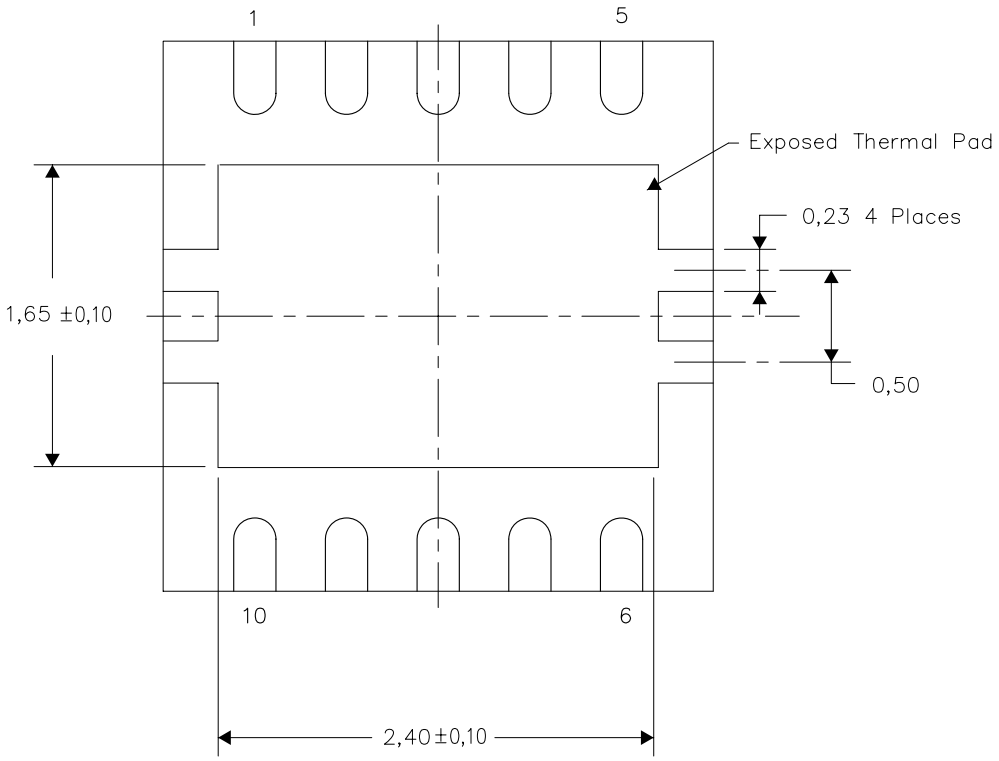
DRC (S–PVSON–N10)

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

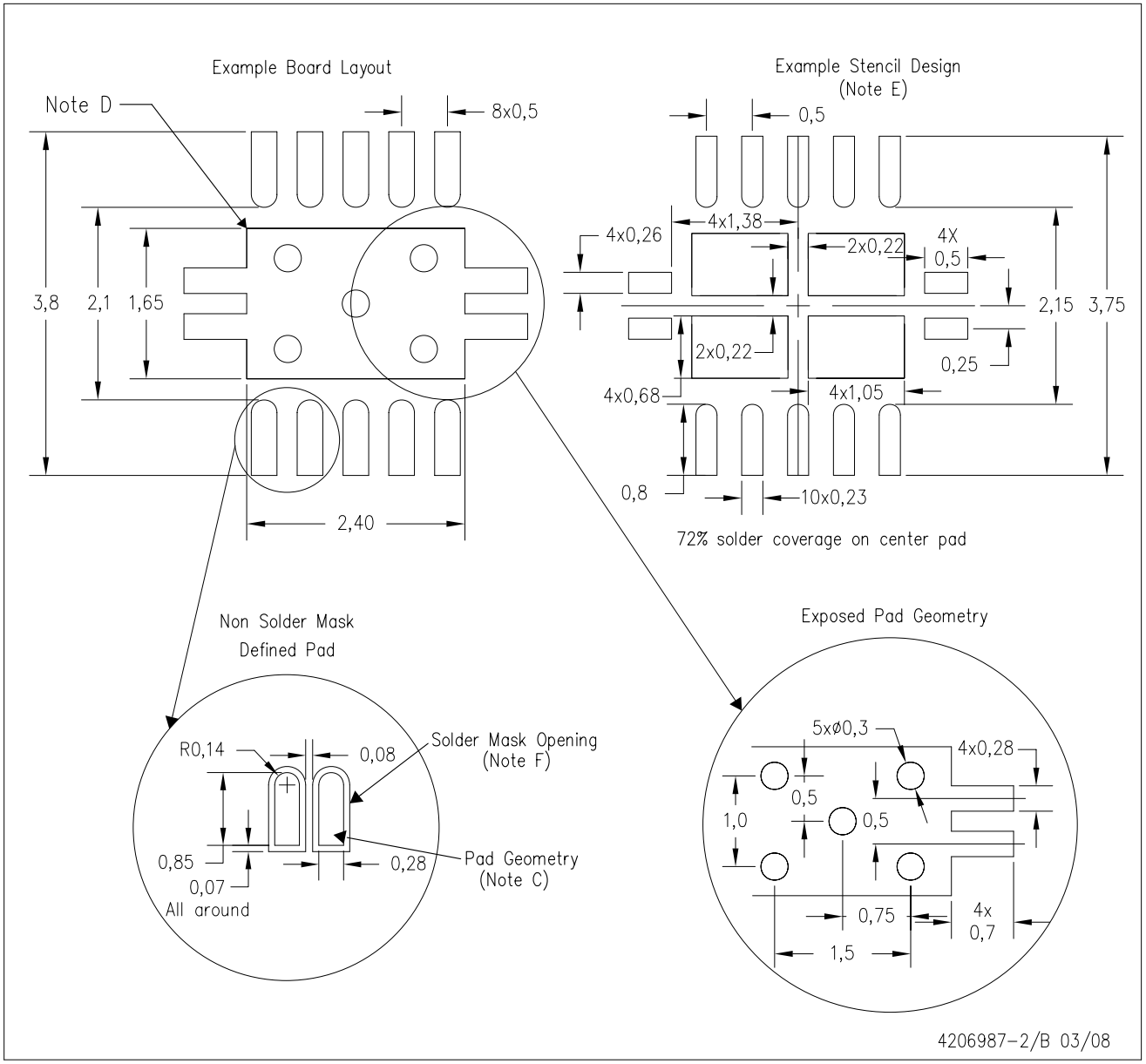



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

# DRC (S–PVSON–N10)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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