

Actual Size
(3,00 mm x 3,00 mm)



# LOW INPUT VOLTAGE, CAP FREE 150-mA LOW-DROPOUT LINEAR REGULATORS

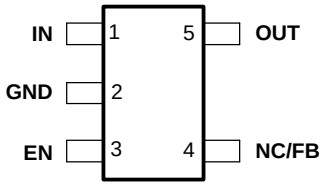
## FEATURES

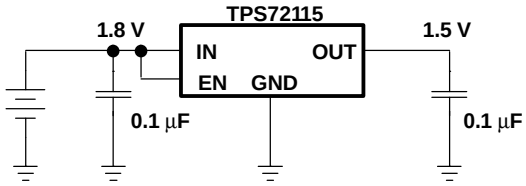
- **150-mA LDO**
- **Available in 1.5-V, 1.6-V, 1.8-V Fixed-Output and Adjustable (1.2-V to 2.5-V) Versions**
- **Low Input Voltage Requirement (Down to 1.8 V)**
- **Small Output Capacitor, 0.1-µF**
- **Dropout Voltage Typically 200 mV at 150 mA**
- **Less Than 1 µA Quiescent Current in Shutdown Mode**
- **Thermal Protection**
- **Over Current Limitation**
- **5-Pin SOT-23 (DBV) Package**

## APPLICATIONS

- **Portable Communication Devices**
- **Battery Powered Equipment**
- **PCMCIA Cards**
- **Personal Digital Assistants**
- **Modems**
- **Bar Code Scanners**
- **Backup Power Supplies**
- **SMPS Post Regulation**
- **Internet Audio**

**DBV PACKAGE**
**(TOP VIEW)**




## DESCRIPTION

The TPS721xx family of LDO regulators is available in fixed voltage options that are commonly used to power the latest DSPs and microcontrollers with an adjustable option ranging from 1.22 V to 2.5 V. These regulators can be used in a wide variety of applications ranging from portable, battery-powered equipment to PC peripherals. The family features operation over a wide range of input voltages (1.8 V to 5.5 V) and low dropout voltage (150 mV at full load). Therefore, compared to many other regulators that require 2.5-V or higher input voltages for operation, these regulators can be operated directly from two AAA batteries. Also, the typical quiescent current (ground pin current) is low, starting at 85 µA during normal operation and 1 µA in shutdown mode. These regulators can be operated very efficiently and, in a battery-powered application, help extend the longevity of the device.

Similar LDO regulators require 1-µF or larger output capacitors for stability. However, this regulator uses an internal compensation scheme that stabilizes the feedback loop over the full range of input voltages and load currents with output capacitances as low as 0.1-µF. Ceramic capacitors of this size are relatively inexpensive and available in small footprints.

This family of regulators is particularly suited as a portable power supply solution due to its minimal board space requirement and 1.8-V minimum input voltage. Being able to use two off-the-shelf AAA batteries makes system design easier and also reduces component cost. Moreover, the solution will be more efficient than if a regulator with a higher input voltage is used.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| $T_J$ | VOLTAGE | PACKAGE | PART NUMBER | | SYMBOL |
|---|---|---|---|---|---|
| -40°C to 125°C | Adjustable | SOT-23 (DBV) | TPS72101DBVT(1) | TPS72101DBVR(2) | PEKI |
| | 1.5 V | | TPS72115DBVT(1) | TPS72115DBVR(2) | PEII |
| | 1.6 V | | TPS72116DBVT(1) | TPS72116DBVR(2) | PHFI |
| | 1.8 V | | TPS72118DBVT(1) | TPS72118DBVR(2) | PEJI |

(1) The DBVT indicates tape and reel of 250 parts.
(2) The DBVR indicates tape and reel of 3000 parts.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)(2)

| | TPS72101, TPS72115, TPS72116, TPS72118 |
|---|---|
| Voltage range at IN | -0.3 V to 7 V |
| Voltage range at EN | -0.3 V to 7 V |
| Voltage on OUT, FB, NC | -0.3 V to $V_I$ + 0.3 V |
| Peak output current | Internally limited |
| ESD rating, HBM | 3 kV |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating junction temperature range, $T_J$ | -40°C to 150°C |
| Storage temperature range, $T_{stg}$ | -65°C to 150°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.All voltage values are with respect to network ground terminal.
(2) All voltage values are with respect to network ground terminal.

## PACKAGE DISSIPATION RATING

| BOARD | PACKAGE | $R_{\Theta JC}$ | $R_{\Theta JA}$ | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A \leq$ 25°C POWER RATING | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|---|---|---|
| Low-K(1) | DBV | 65.8 °C/W | 259 °C/W | 3.9 mW/°C | 386 mW | 212 mW | 154 mW |
| High-K(2) | DBV | 65.8 °C/W | 180 °C/W | 5.6 mW/°C | 555 mW | 305 mW | 222 mW |

(1) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch x 3 inch, two-layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range $V_{IN} = V_{OUT(Nom)} + 1$ V, $I_{OUT} = 1$ mA, EN = $V_{IN}$, $C_{OUT} = 1$ µF (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage (1) | | | | 1.8 | | 5.5 | V |
| $V_{OUT}$ | Output voltage range | TPS72101 | | | 1.225 | | 2.5 | V |
| $I_{OUT}$ | Continuous output current | | | | 0 | | 150 | mA |
| $T_J$ | Operating junction temperature | | | | -40 | | 125 | °C |
| $V_{OUT}$ | Output voltage | TPS72101 | 0 µA < $I_{OUT}$ < 150 mA (1) | 1.8 V ≤ $V_{OUT}$ ≤ 2.5 V | 0.97 $V_O$ | | 1.03 $V_O$ | V |
| | | TPS72115 | $T_J$ = 25°C | | | 1.5 | | |
| | | | 0 µA < $I_{OUT}$ < 150 mA | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V | 1.455 | | 1.545 | |
| | | TPS72116 | $T_J$ = 25°C | | | 1.6 | | |
| | | | 0 µA < $I_{OUT}$ < 150 mA | 2.6 V ≤ $V_{IN}$ ≤ 5.5 V | 1.552 | | 1.648 | |
| | | TPS72118 | $T_J$ = 25°C | | | 1.8 | | |
| | | | 0 µA < $I_{OUT}$ < 150 mA | 2.8 V ≤ $V_{IN}$ ≤ 5.5 V | 1.746 | | 1.854 | |
| $I_{(Q)}$ | Quiescent current (GND current) | | $T_J$ = 25°C | | | 85 | | µA |
| | | | | | | | 120 | |
| | | | $I_{OUT}$ = 150 mA | $T_J$ = 25°C | | 570 | | |
| | | | $I_{OUT}$ = 150 mA | | | | 850 | |
| | Standby current | | EN < 0.5 V | $T_J$ = 25°C | | 0.01 | | µA |
| | | | EN < 0.5 V | | | | 1 | |
| $V_n$ | Output noise voltage | TPS72115 | BW = 200 Hz to 100 kHz, $T_J$ = 25°C | $C_o$ = 1 µF | | 90 | | µV |
| $V_{ref}$ | Reference voltage | | $T_J$ = 25°C | | | 1.225 | | V |
| PSRR | Ripple rejection | | f = 100 Hz, $C_o$ = 10 µF, $I_{OUT}$ = 150 mA | $T_J$ = 25°C; See (1) | | 48 | | dB |
| | Current limit | | See (2) | | 175 | | 525 | mA |
| | Output voltage line regulation ($\Delta V_{OUT}/V_{OUT}$) (1) | | $V_O$ + 1 V < $V_{IN}$≤ 2.5 V | $T_J$= 25°C | | 0.03 | 0.09 | %/V |
| | | | | | | | 0.1 | |
| | Output voltage load regulation | TPS72118 | 0 < $I_{OUT}$ < 150 mA | $T_J$ = 25°C | | 0.5 | | mV |
| $V_{IH}$ | EN high level input | | | | 1.4 | | | V |
| $V_{IL}$ | EN low level input | | | | -0.2 | | 0.4 | |
| $I_I$ | EN input current | | EN = 0 V | | | -0.01 | | µA |
| | | | EN = IN | | | -0.01 | | |
| $V_{DO}$ | Dropout voltage (3) | TPS72118 | $I_{OUT}$ = 150 mA | $T_J$ = 25°C | | 150 | | mV |
| | | TPS72101 | $I_{OUT}$ = 150 mA | 1.2 V ≤ $V_O$ ≤ 5.2 V | | | 240 | |
| $I_n$ | Feedback input current | TPS72101 | | | | | 1 | µA |
| | Thermal shutdown temperature | | | | | 170 | | °C |
| | Thermal shutdown hysteresis | | | | | 20 | | °C |

(1) Minimum IN operating voltage is 1.8 V or $V_{OUT} + V_{DO}$, whichever is greater.
(2) Test condition includes output voltage $V_O$ = 1 V and pulse duration = 10 mS.
(3) Dropout voltage is defined as the differential voltage between $V_O$ and $V_I$ when $V_O$ drops 100 mV below the value measured with $V_{IN} = V_{OUT} + V_{DO}$.

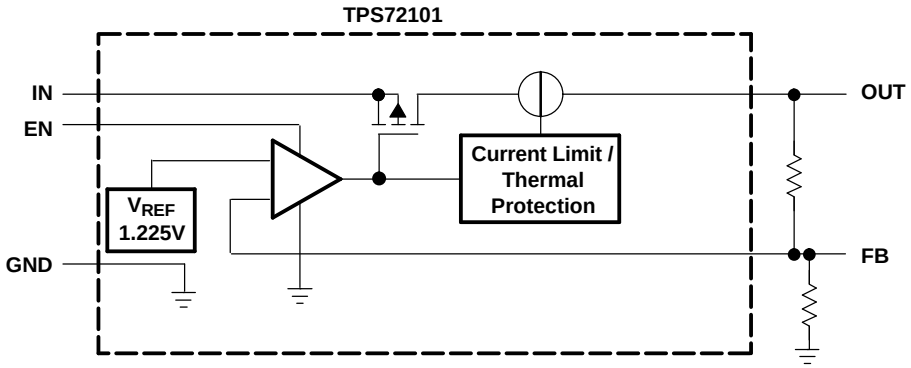
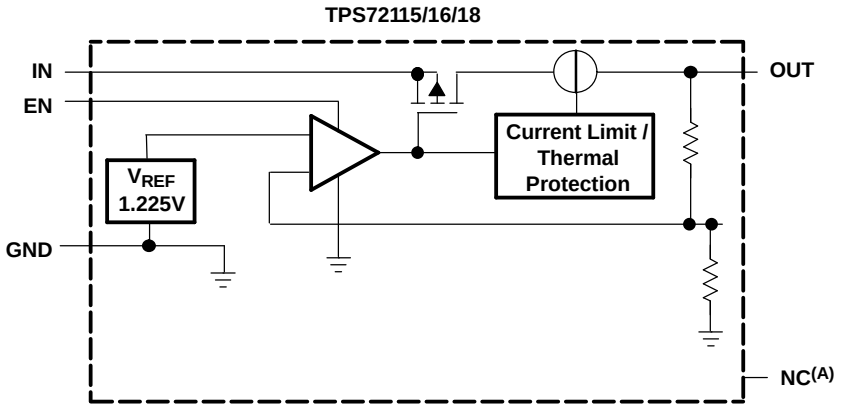



**Figure 1. FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION**




A. This pin must be left floating and not connected to GND.

**Figure 2. FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION**

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | DESCRIPTION |
|---|---|---|
| GND | 2 | Ground |
| EN | 3 | Enable input |
| IN | 1 | Input supply voltage |
| NC/FB | 4 | NC = Not connected (see (A)); FB = Feedback (adjustable option TPS72101) |
| OUT | 5 | Regulated output voltage |

## TYPICAL CHARACTERISTICS

**TPS72118**
**OUTPUT VOLTAGE**
**vs**
**OUTPUT CURRENT**

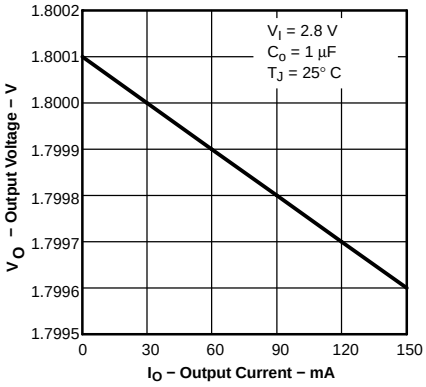



**Figure 3.**

**TPS72118**
**OUTPUT VOLTAGE**
**vs**
**JUNCTION TEMPERATURE**

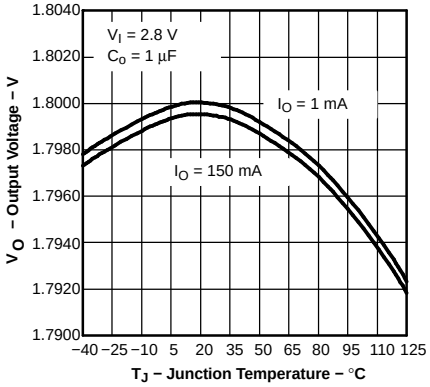



**Figure 4.**

**TPS72118**
**GROUND CURRENT**
**vs**
**JUNCTION TEMPERATURE**

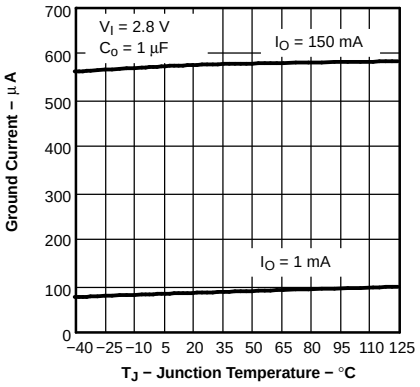



**Figure 5.**

**TPS72118**
**GROUND CURRENT**
**vs**
**OUTPUT CURRENT**

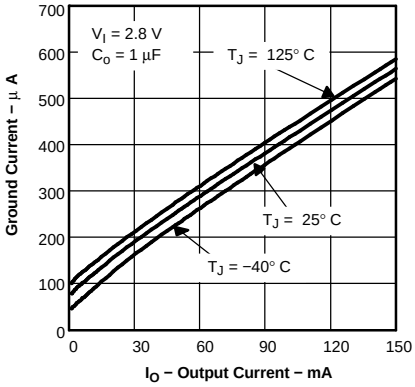



**Figure 6.**

**TPS72118**
**OUTPUT SPECTRAL NOISE DENSITY**
**vs**
**FREQUENCY**

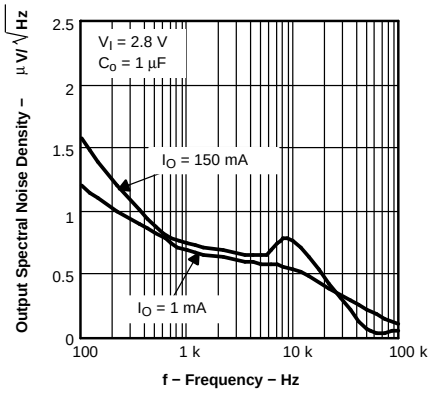



**Figure 7.**

**TPS72118**
**OUTPUT IMPEDANCE**
**vs**
**FREQUENCY**

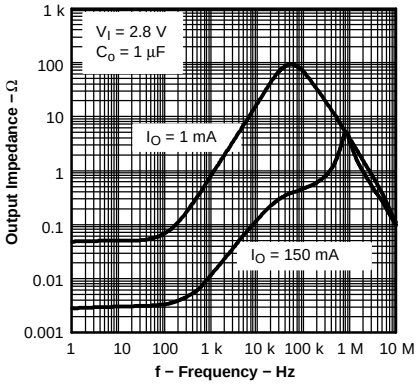



**Figure 8.**

## TYPICAL CHARACTERISTICS (continued)

**TPS72118**
**DROPOUT VOLTAGE**
**vs**
**JUNCTION TEMPERATURE**

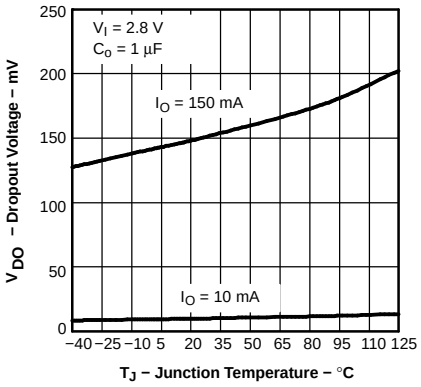



Figure 9.

**TPS72118**
**POWER SUPPLY RIPPLE REJECTION**
**vs**
**FREQUENCY**

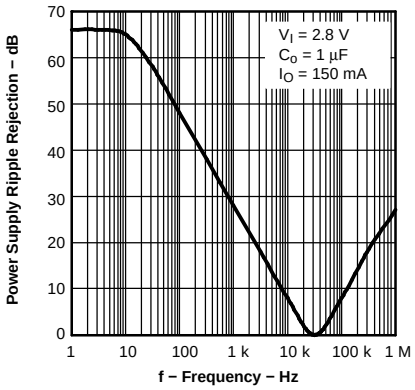



Figure 10.

**TPS72118**
**OUTPUT VOLTAGE, ENABLE VOLTAGE**
**vs**
**TIME (START-UP)**

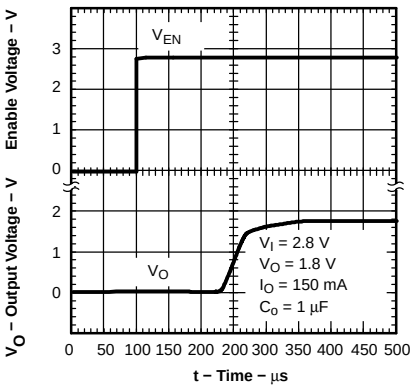



Figure 11.

**TPS72118**
**LINE TRANSIENT RESPONSE**

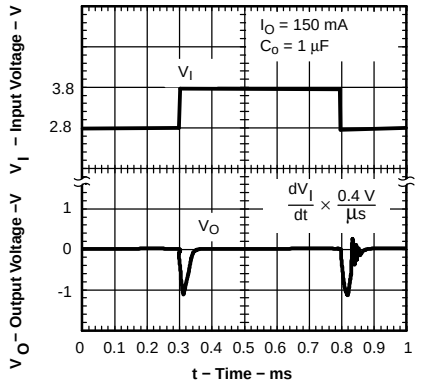



Figure 12.

**TPS72118**
**LOAD TRANSIENT RESPONSE**

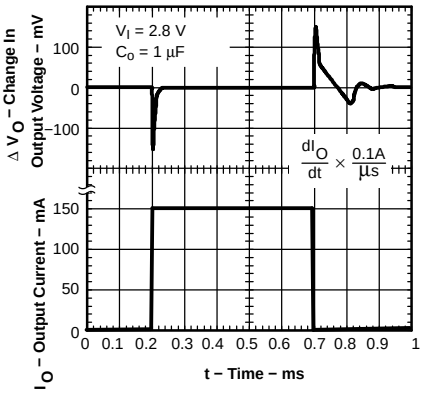



Figure 13.

**POWER UP / POWER DOWN**

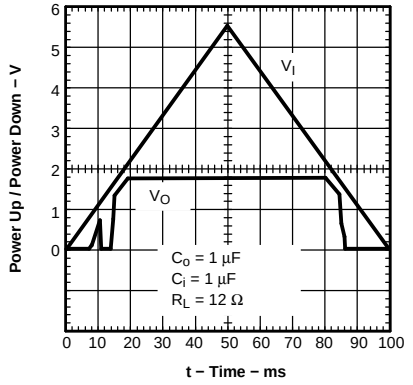



Figure 14.

**DC DROPOUT VOLTAGE**
**vs**
**OUTPUT CURRENT**

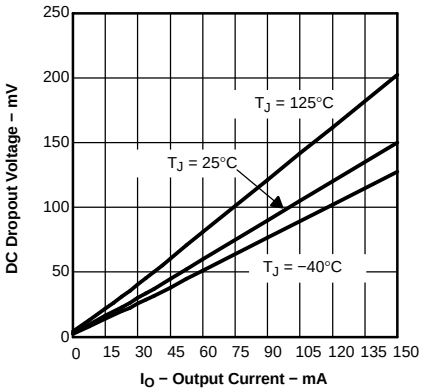



Figure 15.

**TPS72101**
**DROPOUT VOLTAGE**
**vs**
**INPUT VOLTAGE**

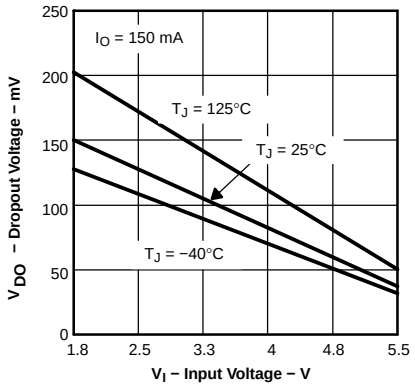



Figure 16.

**MINIMUM REQUIRED INPUT VOLTAGE**
**vs**
**OUTPUT VOLTAGE**

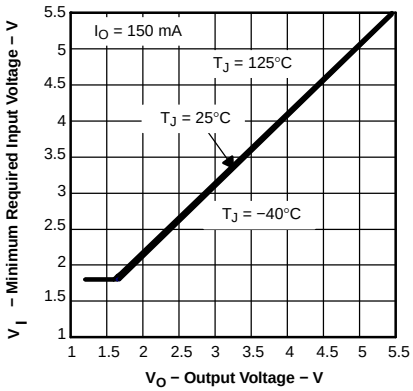



Figure 17.

## APPLICATION INFORMATION

The TPS721xx family of low-dropout (LDO) regulators functions with a very low input voltage (>1.8 V). The dropout voltage is typically 150 mV at full load. Typical quiescent current (ground pin current) is only 85 µA and drops to 1 µA in the shutdown mode.

### DEVICE OPERATION

The TPS721xx family can be operated at low input voltages due to low voltage circuit design techniques and a PMOS pass element that exhibits low dropout.

A logic low on the enable input, EN, shuts off the output and reduces the supply current to less than 1 µA. EN may be tied to $V_{IN}$ in applications where the shutdown feature is not used.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 170°C. Recovery is automatic when the junction temperature drops approximately 20°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

A typical application circuit is shown in Figure 18.

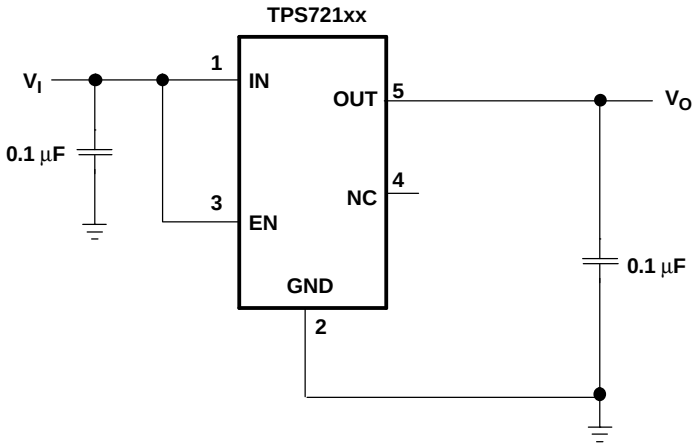



**Figure 18. Typical Application Circuit**

### DUAL SUPPLY APPLICATION

In portable, battery-powered electronics, separate power rails for the DSP or microcontroller core voltage, $V_{(CORE)}$, and I/O peripherals ($V_{IO}$) are usually necessary. The TPS721xx family of LDO linear regulators is ideal for providing $V_{(CORE)}$ for the DSP or microcontroller. As shown in Figure 19, two AAA batteries provide an input voltage to a boost converter and the TPS72115 LDO linear regulator. The batteries combine input voltage ranges from 3.0 V down to 1.8 V near the end of their useful lives. Therefore, a boost converter is necessary to provide the typical 3.3 V needed for $V_{IO}$, and the TPS72115 linear regulator provides a regulated $V_{(CORE)}$ voltage, which in this example is 1.5 V. Although there is no explicit circuitry to perform power-up sequencing of first $V_{(CORE)}$ then $V_{IO}$, the output of the linear regulator reaches its regulated voltage much faster (< 400 µs) than the output of any switching type boost converter due to the inherent slow start up of those types of converters. Assuming a boost converter with minimum $V_I$ of 1.8 V is appropriately chosen, this power supply solution can be used over the entire life of the two off-the-shelf AAA batteries. Thus, this solution is very efficient and the design time and overall cost of the solution is minimized.

## APPLICATION INFORMATION (continued)

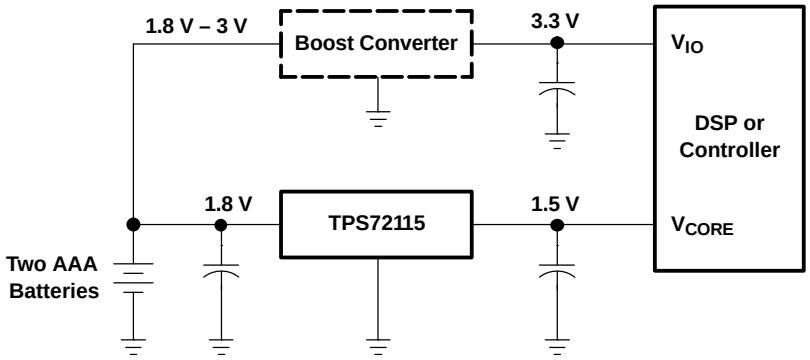



**Figure 19. Dual Supply Application Circuit**

## EXTERNAL CAPACITOR REQUIREMENTS

A 0.1-µF ceramic bypass capacitor is required on both the input and output for stability. Larger capacitors improve transient response, noise rejection, and ripple rejection. A higher value electrolytic input capacitor may be necessary if large, fast rise time load transient are anticipated, and/or there is significant input resistance from the device to the input power supply.

## POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable without damaging the device is 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, $P_D$, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 1 :

$$P_{D(max)} + \frac{T_J max \times T_A}{R_{\theta JA}} \quad (1)$$

Where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package; see the package dissipation rating table.
- $T_A$ is the ambient temperature.

The regulator dissipation is calculated using Equation 2:

$$P_D \quad \left(V_I + V_O\right) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible.

## PROGRAMMING THE TPS72101 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS72101 adjustable regulator is programmed using an external resistor divider as shown in Figure 20. The output voltage is calculated using Equation 3:

$$V_O \quad V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

Where:

- $V_{ref}$ = 1.225 V typ (the internal reference voltage)

## APPLICATION INFORMATION (continued)

Resistors R1 and R2 should be chosen for approximately 10-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided, as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 10 µA and then calculate R1 using Equation 4:

$$R1 \quad \left(\frac{V_O}{V_{ref}} + 1\right) \times R2 \tag{4}$$

Where:

- $V_{ref}$ = 1.225 V.

**OUTPUT VOLTAGE PROGRAMMING GUIDE**

| OUTPUT VOLTAGE (V) | DIVIDER RESISTANCE (kΩ)[1] | |
|---|---|---|
| | R1 | R2 |
| 2.5 | 127 | 121 |

Note (1): 1% values shown.

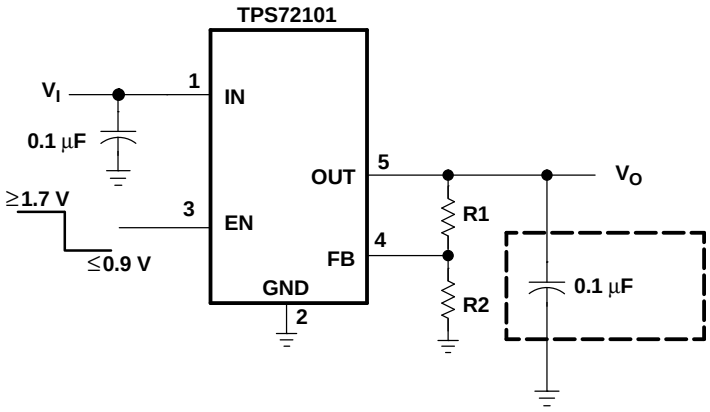



**Figure 20. TPS72101 Adjustable LDO Regulator Programming**

## REGULATOR PROTECTION

The TPS721xx pass element has a built-in back diode that safely conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS721xx also features internal current limiting and thermal protection. During normal operation, the TPS721xx limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 170°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 150°C, regulator operation resumes.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TPS72101DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72101DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72101DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72101DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72115DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72115DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72115DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72115DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72116DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72116DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72116DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72116DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72118DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72118DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72118DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS72118DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

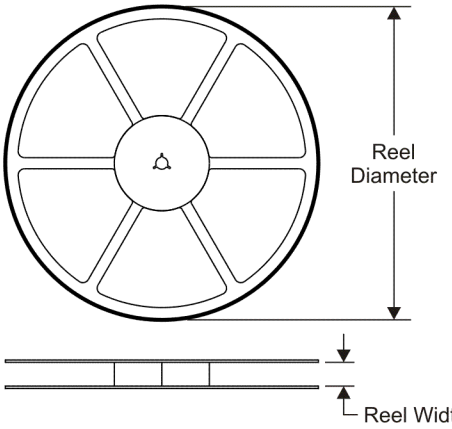
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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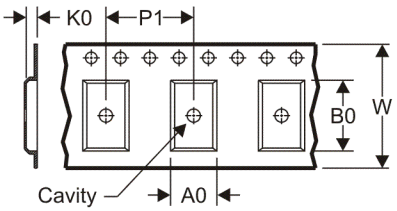
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

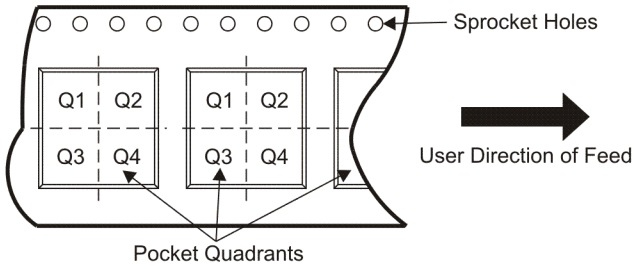



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

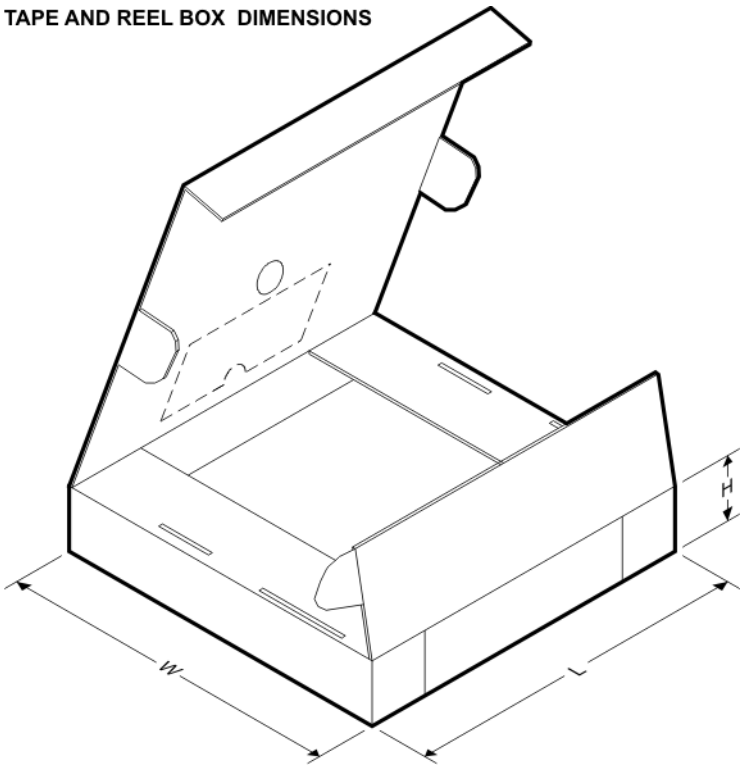
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS72101DBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.0 | 3.0 | 3.0 | 1.0 | 4.0 | 8.0 | Q3 |
| TPS72101DBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.0 | 3.0 | 3.0 | 1.0 | 4.0 | 8.0 | Q3 |
| TPS72115DBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.0 | 3.0 | 3.0 | 1.0 | 4.0 | 8.0 | Q3 |
| TPS72115DBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.0 | 3.0 | 3.0 | 1.0 | 4.0 | 8.0 | Q3 |
| TPS72116DBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.0 | 3.0 | 3.0 | 1.0 | 4.0 | 8.0 | Q3 |
| TPS72116DBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.0 | 3.0 | 3.0 | 1.0 | 4.0 | 8.0 | Q3 |
| TPS72118DBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.0 | 3.0 | 3.0 | 1.0 | 4.0 | 8.0 | Q3 |
| TPS72118DBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.0 | 3.0 | 3.0 | 1.0 | 4.0 | 8.0 | Q3 |

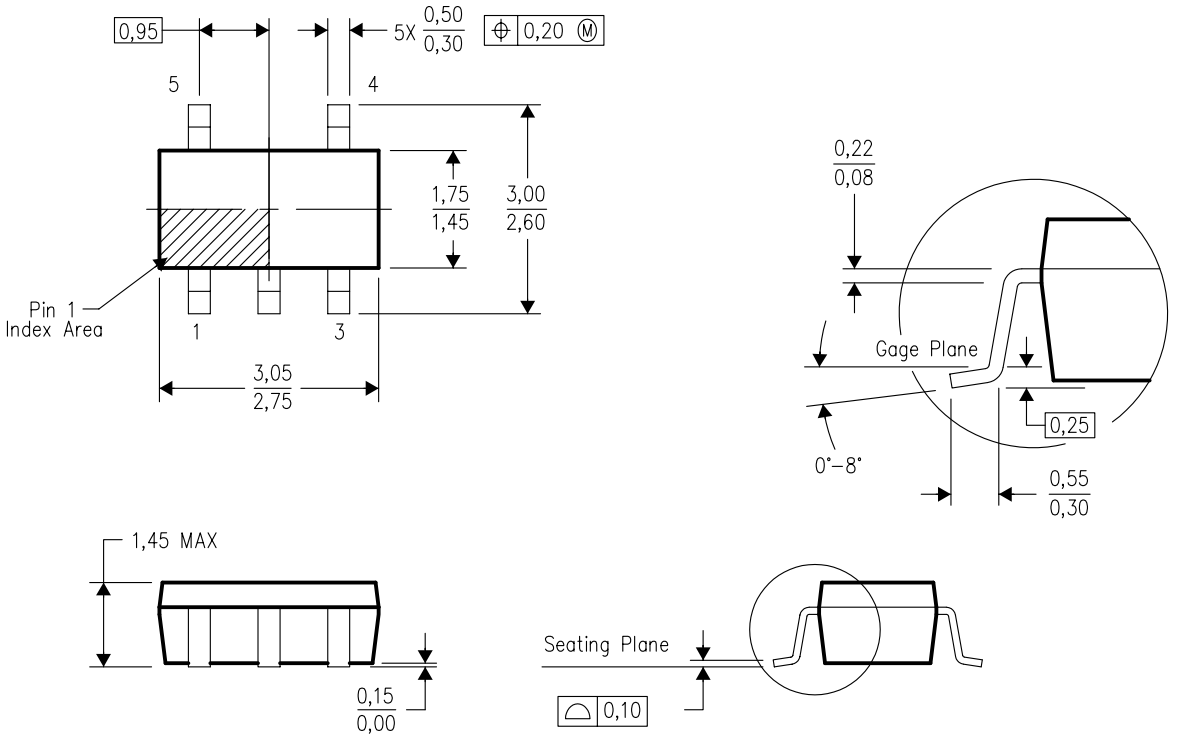
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS72101DBVR | SOT-23 | DBV | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TPS72101DBVT | SOT-23 | DBV | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TPS72115DBVR | SOT-23 | DBV | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TPS72115DBVT | SOT-23 | DBV | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TPS72116DBVR | SOT-23 | DBV | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TPS72116DBVT | SOT-23 | DBV | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TPS72118DBVR | SOT-23 | DBV | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TPS72118DBVT | SOT-23 | DBV | 5 | 250 | 195.0 | 200.0 | 45.0 |

## DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

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