TPS6104x Low-Power DC-DC Boost Converter in SOT-23 and WSON Packages

1 Features

- 1.8-V to 6-V Input Voltage Range
- Adjustable Output Voltage Range up to 28 V
- 400-mA (TPS61040) and 250-mA (TPS61041) Internal Switch Current
- Up to 1-MHz Switching Frequency
- 28-µA Typical No-Load Quiescent Current
- 1-µA Typical Shutdown Current
- Internal Soft Start
- Available in SOT23-5, TSOT23-5, and 2-mm × 2-mm × 0.8-mm WSON Packages

2 Applications

- LCD Bias Supply
- White-LED Supply for LCD Backlights
- Digital Still Camera
- PDAs, Organizers, and Handheld PCs
- Cellular Phones
- Internet Audio Players
- Standard 3.3-V or 5-V to 12-V Conversion

3 Description

The TPS6104x is a high-frequency boost converter dedicated for small to medium LCD bias supply and white LED backlight supplies. The device is ideal to generate output voltages up to 28 V from a dual-cell NiMH/NiCd or a single-cell Li-Ion battery. The part can also be used to generate standard 3.3-V or 5-V to 12-V power conversions.

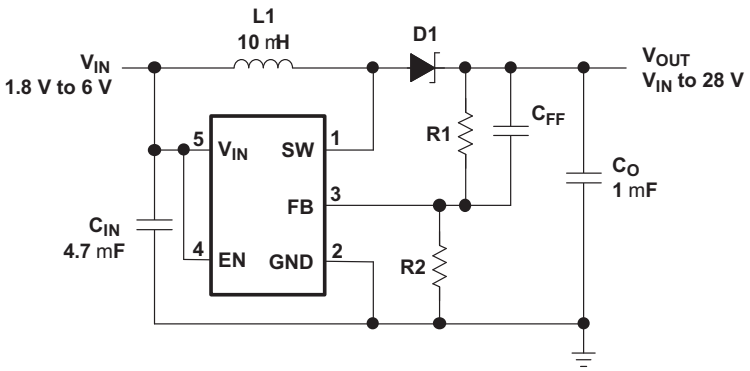
The TPS6104x operates with a switching frequency up to 1 MHz. This frequency allows the use of small external components using ceramic as well as tantalum output capacitors. Together with the thin WSON package, the TPS6104x gives a very small overall solution size. The TPS61040 device has an internal 400-mA switch current limit, while the TPS61041 device has a 250-mA switch current limit, offering lower output voltage ripple and allows the use of a smaller form factor inductor for lower power applications. The low quiescent current (typically 28 µA) together with an optimized control scheme, allows device operation at very high efficiencies over the entire load current range.

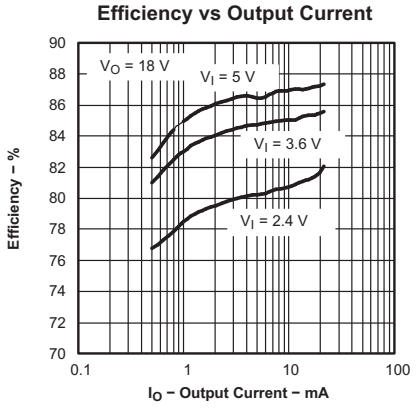
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61040	SOT-23 (5)	2.90 mm × 1.60 mm
	SOT (5)	2.90 mm ×1.60 mm
	WSON (6)	2.00 mm × 2.00 mm
TPS61041	SOT-23 (5)	2.90 mm ×1.60 mm
	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application Schematic





An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

Changes from Revision G (December 2014) to Revision H **Page**

- Added 500 µs/div label to X-axis of Figure 15. ... 15

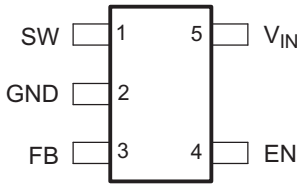
Changes from Revision F (December 2010) to Revision G **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

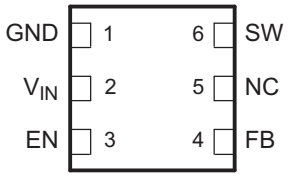
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6 Pin Configuration and Functions

DDC Package, DBV Package
5 Pins
Top View



DRV Package
6 Pins
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DDC, DBV NO.	DRV NO.		
EN	4	3	I	This is the enable pin of the device. Pulling this pin to ground forces the device into shutdown mode reducing the supply current to less than 1 µA. This pin should not be left floating and needs to be terminated.
FB	3	4	I	This is the feedback pin of the device. Connect this pin to the external voltage divider to program the desired output voltage.
GND	2	1	–	Ground
NC	–	5	–	No connection
SW	1	6	I	Connect the inductor and the Schottky diode to this pin. This is the switch pin and is connected to the drain of the internal power MOSFET.
V_{IN}	5	2	I	Supply voltage pin

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltages on pin V_{IN} (2)	–0.3	7	V
Voltages on pins EN, FB (2)	–0.3	V_{IN} + 0.3	V
Switch voltage on pin SW (2)	30	30	V
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±YYY V may actually have higher performance.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	1.8		6	V
V_{OUT}	Output voltage range			28	V
L	Inductor (1)	2.2	10		µH
f	Switching frequency (1)			1	MHz
C_{IN}	Input capacitor (1)		4.7		µF
C_{OUT}	Output capacitor (1)	1			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See application section for further information.

7.4 Thermal Information

THERMAL METRIC (1)		TPS61040			TPS61041		UNIT
		DBV	DDC	DRV	DBV	DRV	
		5 PINS	5 PINS	6 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.2	214.7	83.0	205.2	83.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	118.3	38.5	57.1	118.3	57.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.8	35.4	52.9	34.8	52.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.2	0.4	2.4	12.2	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.9	34.8	53.4	33.9	53.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	26.9	—	26.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

V_{IN} = 2.4 V, EN = V_{IN}, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		1.8		6	V
I_Q	Operating quiescent current	I_{OUT} = 0 mA, not switching, V_{FB} = 1.3 V		28	50	µA
I_{SD}	Shutdown current	EN = GND		0.1	1	µA
V_{UVLO}	Undervoltage lockout threshold			1.5	1.7	V
ENABLE						
V_{IH}	EN high level input voltage		1.3			V
V_{IL}	EN low level input voltage				0.4	V
I_I	EN input leakage current	EN = GND or V_{IN}		0.1	1	µA
POWER SWITCH AND CURRENT LIMIT						
Vsw	Maximum switch voltage				30	V
t_{off}	Minimum off time		250	400	550	ns
t_{on}	Maximum on time		4	6	7.5	µs
$R_{DS(on)}$	MOSFET on-resistance	V_{IN} = 2.4 V; I_{SW} = 200 mA; TPS61040		600	1000	mΩ
$R_{DS(on)}$	MOSFET on-resistance	V_{IN} = 2.4 V; I_{SW} = 200 mA; TPS61041		750	1250	mΩ
	MOSFET leakage current	V_{SW} = 28 V		1	10	µA
I_{LIM}	MOSFET current limit	TPS61040	350	400	450	mA
I_{LIM}	MOSFET current limit	TPS61041	215	250	285	mA
OUTPUT						
V_{OUT}	Adjustable output voltage range		V_{IN}		28	V
V_{ref}	Internal voltage reference			1.233		V
I_{FB}	Feedback input bias current	V_{FB} = 1.3 V			1	µA
V_{FB}	Feedback trip point voltage	1.8 V ≤ V_{IN} ≤ 6 V	1.208	1.233	1.258	V
	Line regulation (1)	1.8 V ≤ V_{IN} ≤ 6 V; V_{OUT} = 18 V; I_{load} = 10 mA; C_{FF} = not connected		0.05		%/V
	Load regulation (1)	V_{IN} = 2.4 V; V_{OUT} = 18 V; 0 mA ≤ I_{OUT} ≤ 30 mA		0.15		%/mA

(1) The line and load regulation depend on the external component selection. See the application section for further information.

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7.6 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
η	Efficiency	vs Load current	Figure 1, Figure 2, Figure 3
		vs Input voltage	Figure 4
I_Q	Quiescent current	vs Input voltage and temperature	Figure 5
V_{FB}	Feedback voltage	vs Temperature	Figure 6
I_{SW}	Switch current limit	vs Temperature	Figure 7
I_{CL}	Switch current limit	vs Supply voltage, TPS61041	Figure 8
		vs Supply voltage, TPS61040	Figure 9
$R_{DS(on)}$	$R_{DS(on)}$	vs Temperature	Figure 10
		vs Supply voltage	Figure 11
	Line transient response		Figure 13
	Load transient response		Figure 14
	Start-up behavior		Figure 15

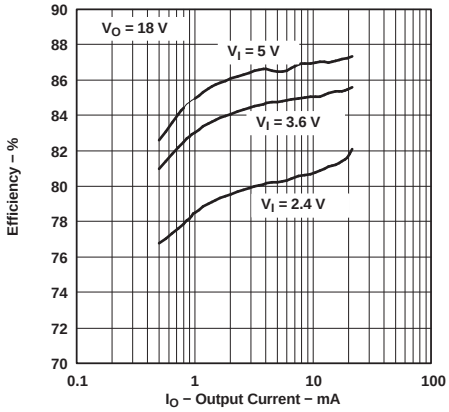


Figure 1. Efficiency vs Output Current

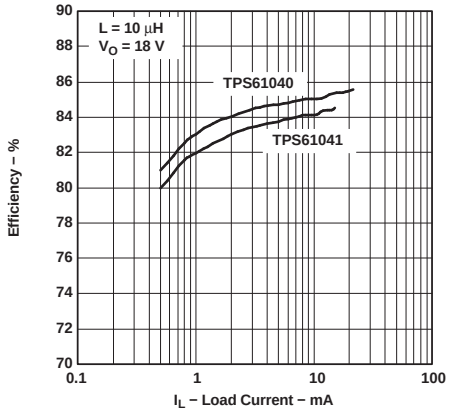


Figure 2. Efficiency vs Load Current

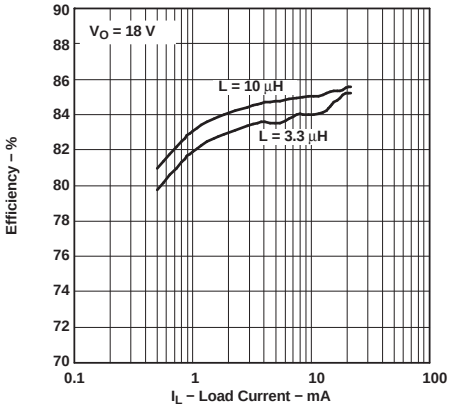


Figure 3. Efficiency vs Load Current

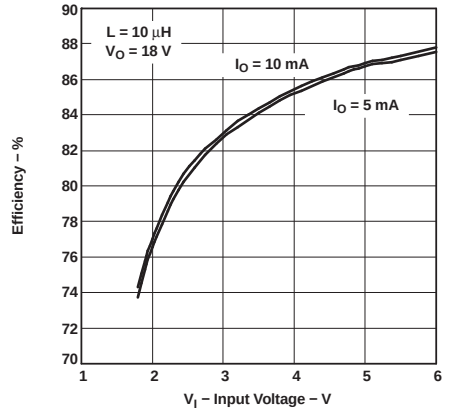


Figure 4. Efficiency vs Input Voltage

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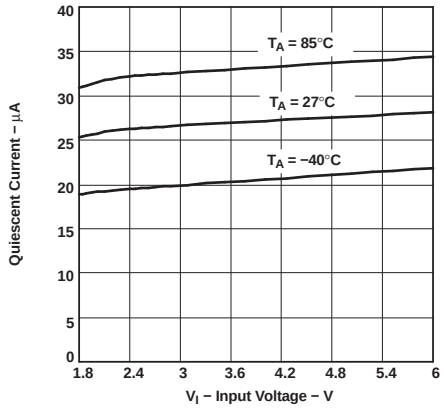


Figure 5. TPS61040 Quiescent Current vs Input Voltage

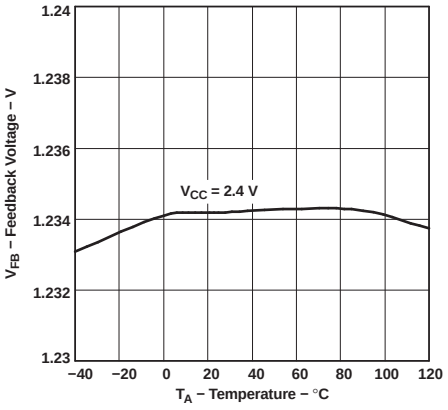


Figure 6. Feedback Voltage vs Free-Air Temperature

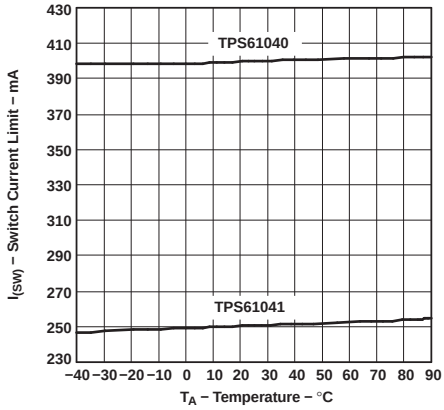


Figure 7. TPS6104x Switch Current Limit vs Free-Air Temperature

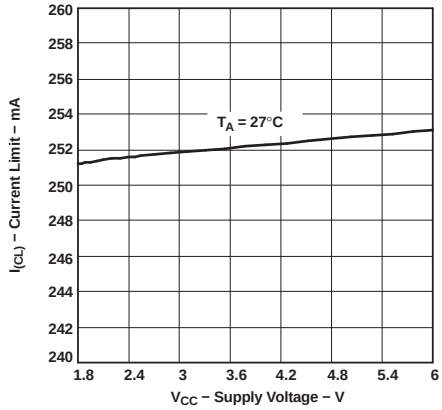


Figure 8. TPS61041 Current Limit vs Supply Voltage

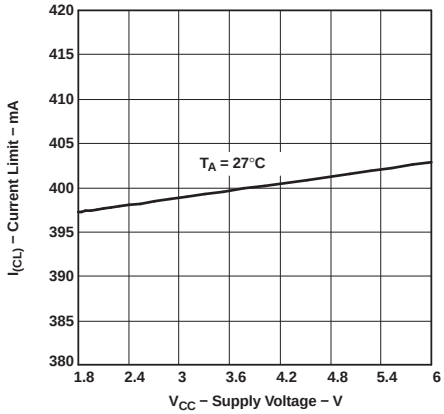


Figure 9. TPS61040 Current Limit vs Supply Voltage

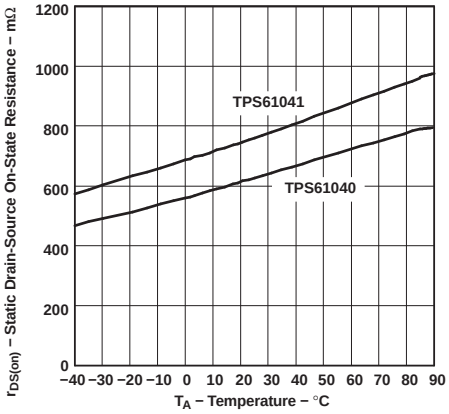


Figure 10. TPS6104x Static Drain-Source On-State Resistance vs Free-Air Temperature

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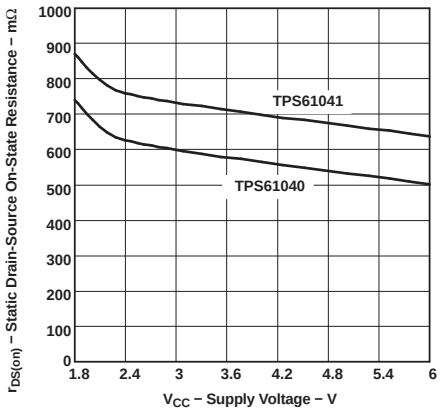


Figure 11. TPS6104x Static Drain-Source On-State Resistance vs Supply Voltage

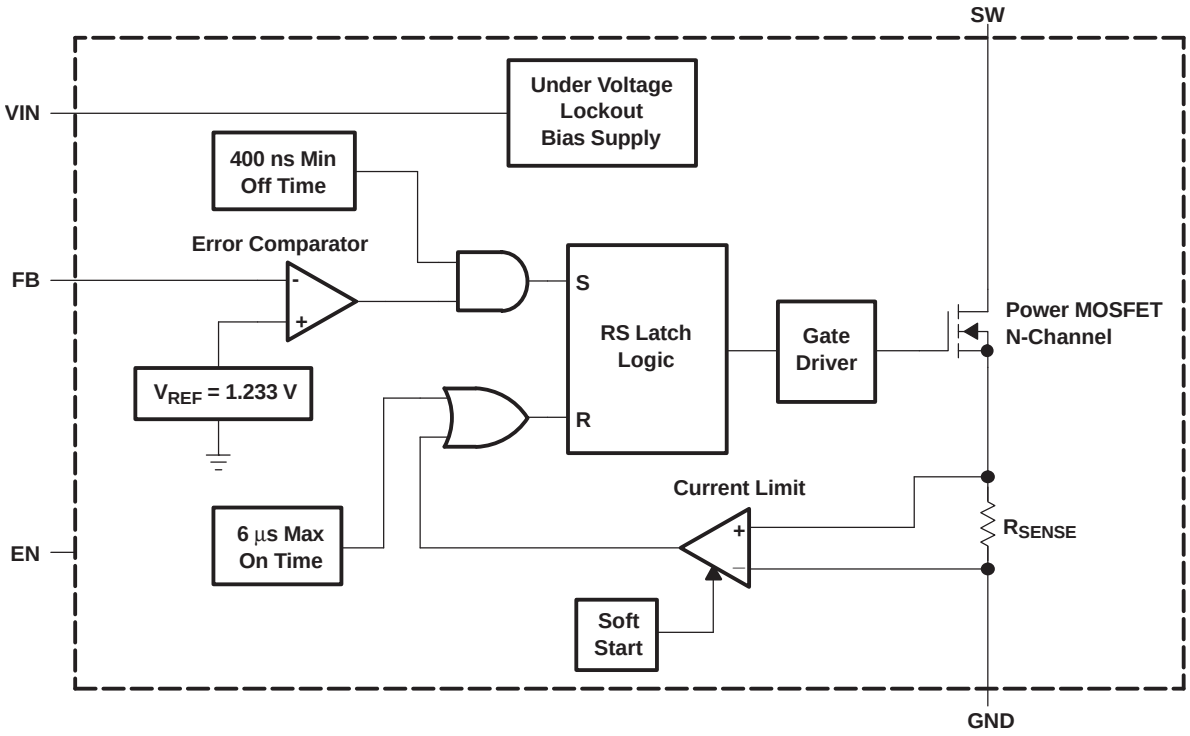
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8 Detailed Description

8.1 Overview

The TPS6104x is a high-frequency boost converter dedicated for small to medium LCD bias supply and white LED backlight supplies. The device is ideal to generate output voltages up to 28 V from a dual-cell NiMH/NiCd or a single cell device Li-Ion battery.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Peak Current Control

The internal switch turns on until the inductor current reaches the typical dc current limit (I_{LIM}) of 400 mA (TPS61040) or 250 mA (TPS61041). Due to the internal propagation delay of typical 100 ns, the actual current exceeds the dc current limit threshold by a small amount. The typical peak current limit can be calculated:

$$I_{peak(typ)} = I_{LIM} + \frac{V_{IN}}{L} \times 100\ ns$$

$$I_{peak(typ)} = 400\ mA + \frac{V_{IN}}{L} \times 100\ ns \text{ for the TPS61040}$$

$$I_{peak(typ)} = 250\ mA + \frac{V_{IN}}{L} \times 100\ ns \text{ for the TPS61041} \quad (1)$$

The higher the input voltage and the lower the inductor value, the greater the peak.

By selecting the TPS6104x, it is possible to tailor the design to the specific application current limit requirements. A lower current limit supports applications requiring lower output power and allows the use of an inductor with a lower current rating and a smaller form factor. A lower current limit usually has a lower output voltage ripple as well.

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Feature Description (continued)

8.3.2 Soft Start

All inductive step-up converters exhibit high inrush current during start-up if no special precaution is made. This can cause voltage drops at the input rail during start up and may result in an unwanted or early system shut down.

The TPS6104x limits this inrush current by increasing the current limit in two steps starting from $\frac{I_{LIM}}{4}$ for 256 cycles to $\frac{I_{LIM}}{2}$ for the next 256 cycles, and then full current limit (see Figure 15).

8.3.3 Enable

Pulling the enable (EN) to ground shuts down the device reducing the shutdown current to 1 µA (typical). Because there is a conductive path from the input to the output through the inductor and Schottky diode, the output voltage is equal to the input voltage during shutdown. The enable pin needs to be terminated and should not be left floating. Using a small external transistor disconnects the input from the output during shutdown as shown in Figure 17.

8.3.4 Undervoltage Lockout

An undervoltage lockout prevents misoperation of the device at input voltages below typical 1.5 V. When the input voltage is below the undervoltage threshold, the main switch is turned off.

8.3.5 Thermal Shutdown

An internal thermal shutdown is implemented and turns off the internal MOSFETs when the typical junction temperature of 168°C is exceeded. The thermal shutdown has a hysteresis of typically 25°C. This data is based on statistical means and is not tested during the regular mass production of the IC.

8.4 Device Functional Modes

8.4.1 Operation

The TPS6104x operates with an input voltage range of 1.8 V to 6 V and can generate output voltages up to 28 V. The device operates in a pulse-frequency-modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range, and with a switching frequency up to 1 MHz, the device enables the use of very small external components.

The converter monitors the output voltage, and as soon as the feedback voltage falls below the reference voltage of typically 1.233 V, the internal switch turns on and the current ramps up. The switch turns off as soon as the inductor current reaches the internally set peak current of typically 400 mA (TPS61040) or 250 mA (TPS61041). See *Peak Current Control* for more information. The second criteria that turns off the switch is the maximum on-time of 6 µs (typical). This is just to limit the maximum on-time of the converter to cover for extreme conditions. As the switch is turned off the external Schottky diode is forward biased delivering the current to the output. The switch remains off for a minimum of 400 ns (typical), or until the feedback voltage drops below the reference voltage again. Using this PFM peak current control scheme the converter operates in discontinuous conduction mode (DCM) where the switching frequency depends on the output current, which results in very high efficiency over the entire load current range. This regulation scheme is inherently stable, allowing a wider selection range for the inductor and output capacitor.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6104x is designed for output voltages up to 28 V with an input voltage range of 1.8 V to 6 V and a switch peak current limit of 400 mA (250 mA for the TPS61041). The device operates in a pulse-frequency-modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range, and with a switching frequency up to 1 MHz, the device enables the use of very small external components. The following section provides a step-by-step design approach for configuring the TPS61040 as a voltage regulating boost converter for LCD bias power supply, as shown in Figure 12.

9.2 Typical Application

The following section provides a step-by-step design approach for configuring the TPS611040 as a voltage regulating boost converter for LCD bias supply, as shown in Figure 12.

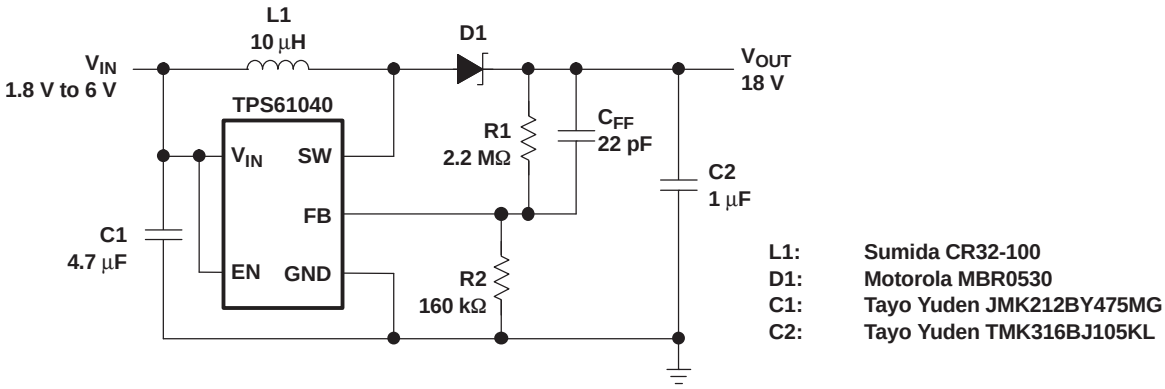


Figure 12. LCD Bias Supply

9.2.1 Design Requirements

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage	1.8 V to 6 V
Output Voltage	18 V
Output Current	10 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection, Maximum Load Current

Because the PFM peak current control scheme is inherently stable, the inductor value does not affect the stability of the regulator. The selection of the inductor together with the nominal load current, input and output voltage of the application determines the switching frequency of the converter. Depending on the application, inductor values from 2.2 µH to 47 µH are recommended. The maximum inductor value is determined by the maximum on time of the switch, typically 6 µs. The peak current limit of 400 mA/250 mA (typically) should be reached within this 6-µs period for proper operation.

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The inductor value determines the maximum switching frequency of the converter. Therefore, select the inductor value that ensures the maximum switching frequency at the converter maximum load current is not exceeded. The maximum switching frequency is calculated by the following formula:

$$fS_{max} = \frac{V_{IN(min)} \times (V_{OUT} - V_{IN})}{I_P \times L \times V_{OUT}} \quad (2)$$

where

- I_P = Peak current as described in *Peak Current Control*
- L = Selected inductor value
- $V_{IN(min)}$ = The highest switching frequency occurs at the minimum input voltage

If the selected inductor value does not exceed the maximum switching frequency of the converter, the next step is to calculate the switching frequency at the nominal load current using the following formula:

$$fS(I_{load}) = \frac{2 \times I_{load} \times (V_{OUT} - V_{IN} + Vd)}{I_P^2 \times L} \quad (3)$$

where

- I_P = Peak current as described in *Peak Current Control*
- L = Selected inductor value
- I_{load} = Nominal load current
- Vd = Rectifier diode forward voltage (typically 0.3 V)

A smaller inductor value gives a higher converter switching frequency, but lowers the efficiency.

The inductor value has less effect on the maximum available load current and is only of secondary order. The best way to calculate the maximum available load current under certain operating conditions is to estimate the expected converter efficiency at the maximum load current. This number can be taken out of the efficiency graphs shown in Figure 1 through Figure 4. The maximum load current can then be estimated as follows:

$$I_{load\ max} = \eta \frac{I_P^2 \times L \times fS_{max}}{2 \times (V_{OUT} - V_{IN})} \quad (4)$$

where

- I_P = Peak current as described in *Peak Current Control*
- L = Selected inductor value
- fS_{max} = Maximum switching frequency as calculated previously
- η = Expected converter efficiency. Typically 70% to 85%

The maximum load current of the converter is the current at the operation point where the converter starts to enter the continuous conduction mode. Usually the converter should always operate in discontinuous conduction mode.

Last, the selected inductor should have a saturation current that meets the maximum peak current of the converter (as calculated in *Peak Current Control*). Use the maximum value for I_{LIM} for this calculation.

Another important inductor parameter is the dc resistance. The lower the dc resistance, the higher the efficiency of the converter. See Table 3 and the typical applications for the inductor selection.

Table 3. Recommended Inductor for Typical LCD Bias Supply (see Figure 23)

DEVICE	INDUCTOR VALUE	COMPONENT SUPPLIER	COMMENTS
TPS61040	10 µH	Sumida CR32-100	High efficiency
	10 µH	Sumida CDRH3D16-100	High efficiency
	10 µH	Murata LQH4C100K04	High efficiency
	4.7 µH	Sumida CDRH3D16-4R7	Small solution size
	4.7 µH	Murata LQH3C4R7M24	Small solution size

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Table 3. Recommended Inductor for Typical LCD Bias Supply (see Figure 23) (continued)

DEVICE	INDUCTOR VALUE	COMPONENT SUPPLIER	COMMENTS
TPS61041	10 µH	Murata LQH3C100K24	High efficiency Small solution size

9.2.2.2 Setting the Output Voltage

The output voltage is calculated as:

$$V_{OUT} = 1.233\ V \times \left(1 + \frac{R1}{R2}\right) \quad (5)$$

For battery-powered applications, a high-impedance voltage divider should be used with a typical value for R2 of ≤200 kΩ and a maximum value for R1 of 2.2 MΩ. Smaller values might be used to reduce the noise sensitivity of the feedback pin.

A feedforward capacitor across the upper feedback resistor R1 is required to provide sufficient overdrive for the error comparator. Without a feedforward capacitor, or one whose value is too small, the TPS6104x shows *double pulses* or a pulse burst instead of single pulses at the switch node (SW), causing higher output voltage ripple. If this higher output voltage ripple is acceptable, the feedforward capacitor can be left out.

The lower the switching frequency of the converter, the larger the feedforward capacitor value required. A good starting point is to use a 10-pF feedforward capacitor. As a first estimation, the required value for the feedforward capacitor at the operation point can also be calculated using the following formula:

$$C_{FF} = \frac{1}{2 \times \pi \times \frac{fS}{20} \times R1} \quad (6)$$

where

- R1 = Upper resistor of voltage divider
- fS = Switching frequency of the converter at the nominal load current (See *Inductor Selection, Maximum Load Current* for calculating the switching frequency)
- C_{FF} = Choose a value that comes closest to the result of the calculation

The larger the feedforward capacitor the worse the line regulation of the device. Therefore, when concern for line regulation is paramount, the selected feedforward capacitor should be as small as possible. See the following section for more information about line and load regulation.

9.2.2.3 Line and Load Regulation

The line regulation of the TPS6104x depends on the voltage ripple on the feedback pin. Usually a 50 mV peak-to-peak voltage ripple on the feedback pin FB gives good results.

Some applications require a very tight line regulation and can only allow a small change in output voltage over a certain input voltage range. If no feedforward capacitor C_{FF} is used across the upper resistor of the voltage feedback divider, the device has the best line regulation. Without the feedforward capacitor the output voltage ripple is higher because the TPS6104x shows output voltage bursts instead of single pulses on the switch pin (SW), increasing the output voltage ripple. Increasing the output capacitor value reduces the output voltage ripple.

If a larger output capacitor value is not an option, a feedforward capacitor C_{FF} can be used as described in the previous section. The use of a feedforward capacitor increases the amount of voltage ripple present on the feedback pin (FB). The greater the voltage ripple on the feedback pin (≥50 mV), the worse the line regulation. There are two ways to improve the line regulation further:

1. Use a smaller inductor value to increase the switching frequency which will lower the output voltage ripple, as well as the voltage ripple on the feedback pin.
2. Add a small capacitor from the feedback pin (FB) to ground to reduce the voltage ripple on the feedback pin down to 50 mV again. As a starting point, the same capacitor value as selected for the feedforward capacitor C_{FF} can be used.

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9.2.2.4 Output Capacitor Selection

For best output voltage filtering, a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value but tantalum capacitors can be used as well, depending on the application.

Assuming the converter does not show double pulses or pulse bursts on the switch node (SW), the output voltage ripple can be calculated as:

$$\Delta V_{out} = \frac{I_{out}}{C_{out}} \times \left(\frac{1}{fS(Iout)} - \frac{I_P \times L}{Vout + Vd - Vin} \right) + I_P \times ESR \quad (7)$$

where

- I_P = Peak current as described in *Peak Current Control*
- L = Selected inductor value
- I_{out} = Nominal load current
- fS (I_{out}) = Switching frequency at the nominal load current as calculated previously
- Vd = Rectifier diode forward voltage (typically 0.3 V)
- C_{out} = Selected output capacitor
- ESR = Output capacitor ESR value

See Table 4 and the *Typical Application* for choosing the output capacitor.

Table 4. Recommended Input and Output Capacitors

DEVICE	CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER(1)	COMMENTS
TPS6104x	4.7 µF/X5R/0805	6.3 V	Tayo Yuden JMK212BY475MG	C_{IN}/C_{OUT}
	10 µF/X5R/0805	6.3 V	Tayo Yuden JMK212BJ106MG	C_{IN}/C_{OUT}
	1 µF/X7R/1206	25 V	Tayo Yuden TMK316BJ105KL	C_{OUT}
	1 µF/X5R/1206	35 V	Tayo Yuden GMK316BJ105KL	C_{OUT}
	4.7 µF/X5R/1210	25 V	Tayo Yuden TMK325BJ475MG	C_{OUT}

(1) See Third-Party Products disclaimer.

9.2.2.5 Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 4.7-µF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased. See Table 4 and typical applications for input capacitor recommendations.

9.2.2.6 Diode Selection

To achieve high efficiency a Schottky diode should be used. The current rating of the diode should meet the peak current rating of the converter as it is calculated in *Peak Current Control*. Use the maximum value for I_{LIM} for this calculation. See Table 5 and the typical applications for the selection of the Schottky diode.

Table 5. Recommended Schottky Diode for Typical LCD Bias Supply (see Figure 23)

DEVICE	REVERSE VOLTAGE	COMPONENT SUPPLIER(1)	COMMENTS
TPS6104x	30 V	ON Semiconductor MBR0530	
	20 V	ON Semiconductor MBR0520	
	20 V	ON Semiconductor MBRM120L	High efficiency
	30 V	Toshiba CRS02	

(1) See Third-Party Products disclaimer.

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9.2.3 Application Curves

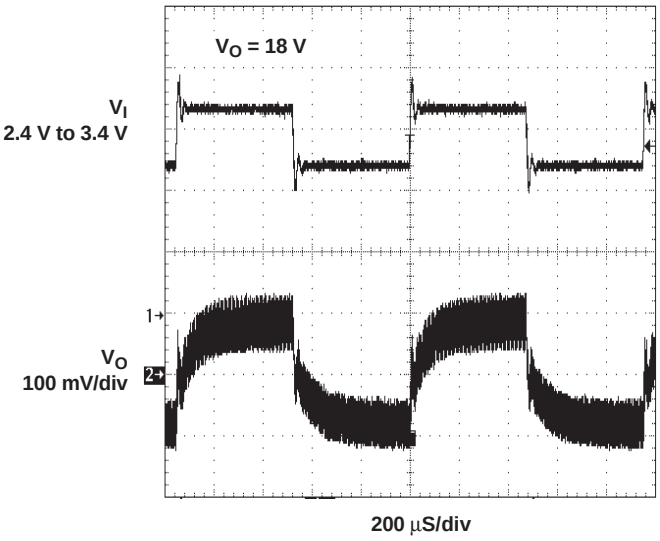


Figure 13. Line Transient Response

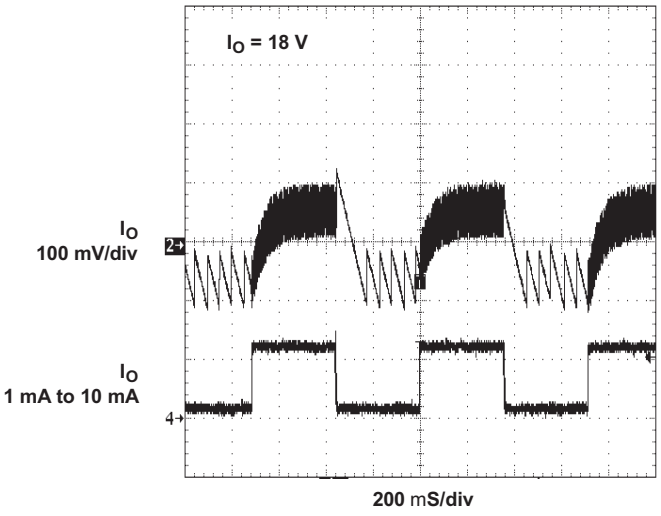


Figure 14. Load Transient Response

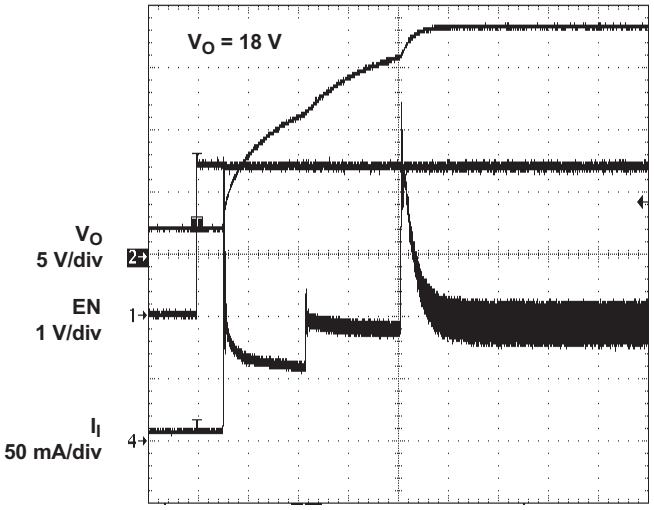


Figure 15. Start-Up Behavior

9.3 System Examples

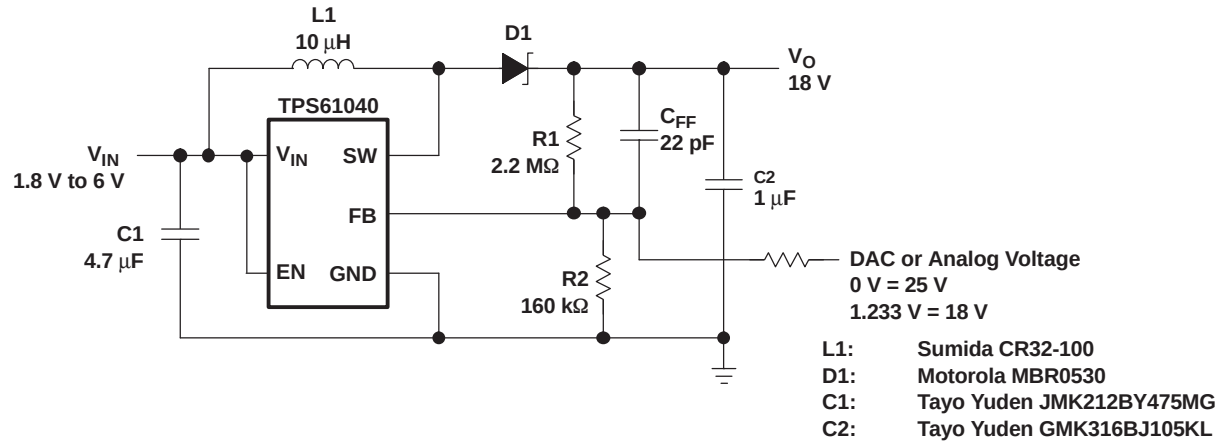


Figure 16. LCD Bias Supply With Adjustable Output Voltage

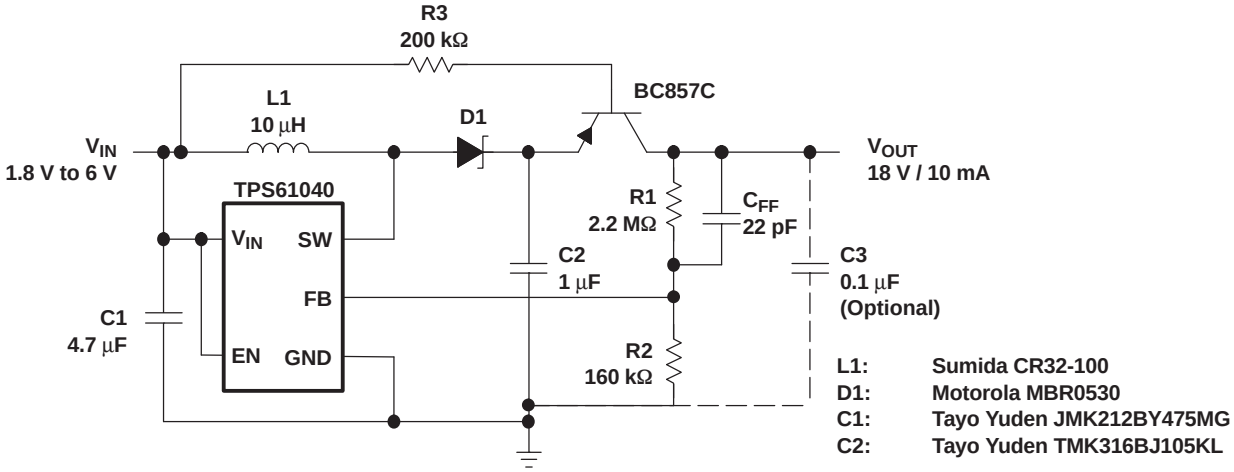


Figure 17. LCD Bias Supply With Load Disconnect

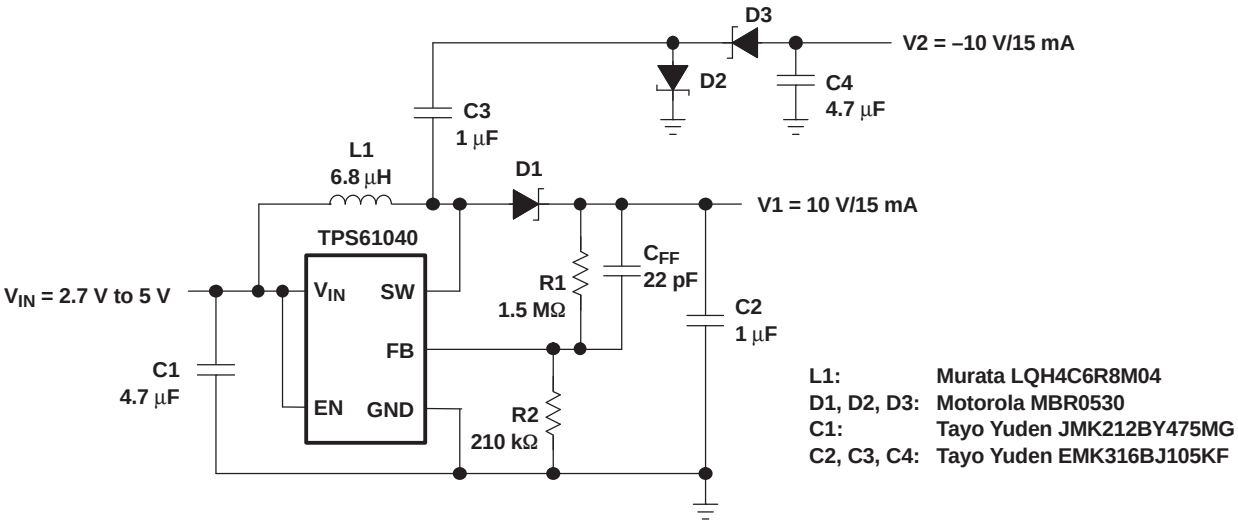


Figure 18. Positive and Negative Output LCD Bias Supply

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System Examples (continued)

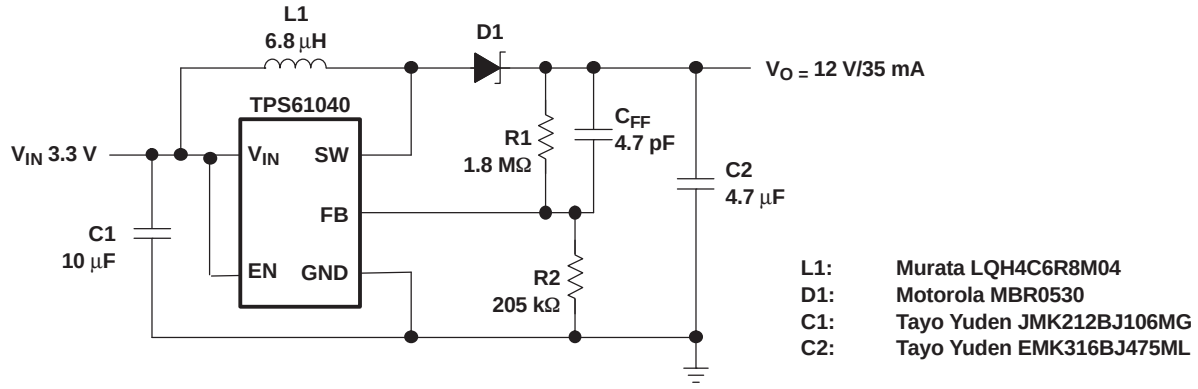


Figure 19. Standard 3.3-V to 12-V Supply

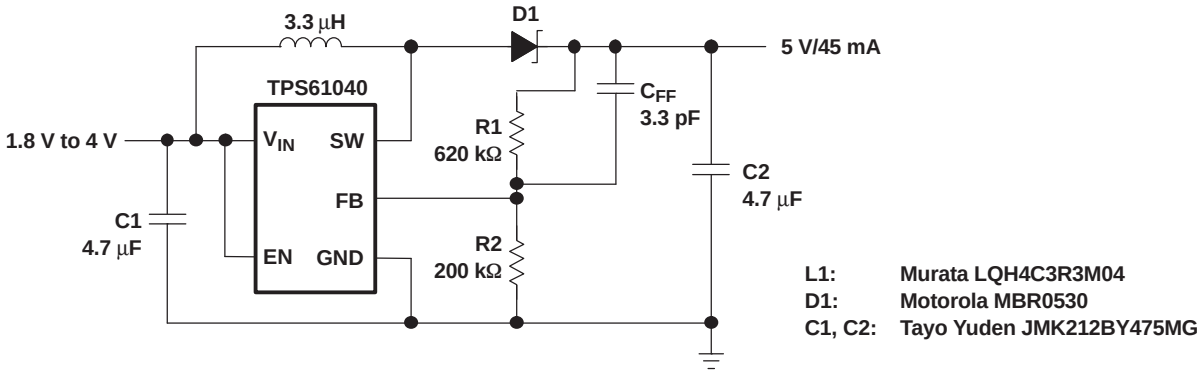


Figure 20. Dual Battery Cell to 5-V/50-mA Conversion
Efficiency Approximately Equals 84% at V_{IN} = 2.4 V to Vo = 5 V/45 mA

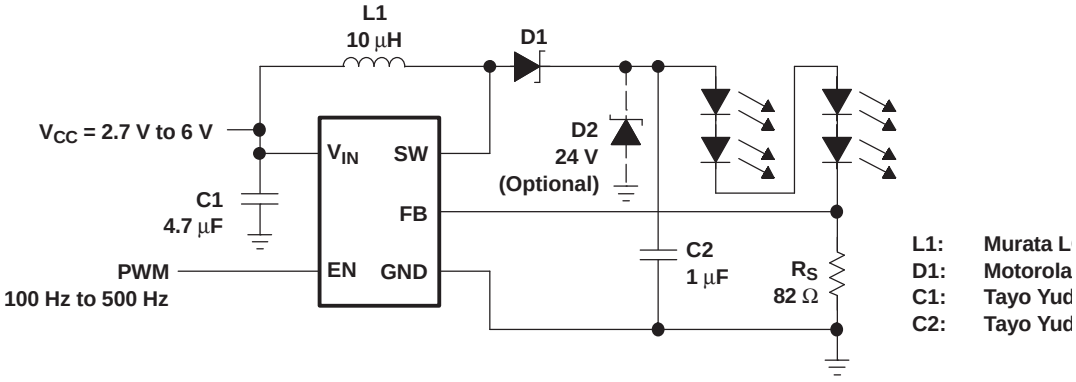
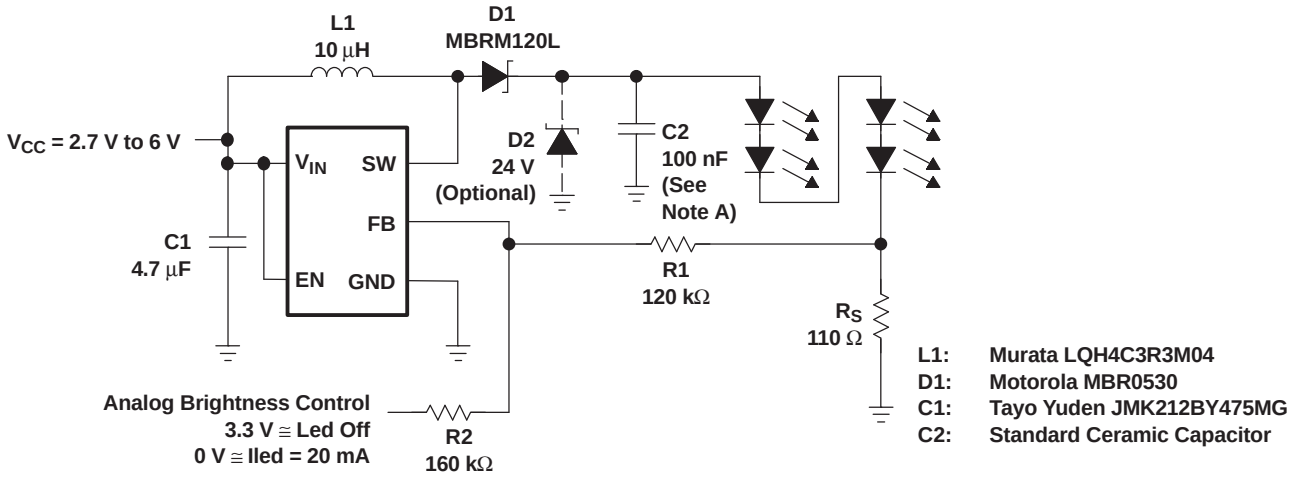


Figure 21. White LED Supply With Adjustable Brightness Control
Using a PWM Signal on the Enable Pin, Efficiency Approximately Equals 86% at V_{IN} = 3 V, I_{LED} = 15 mA

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System Examples (continued)



A. A smaller output capacitor value for C2 causes a larger LED ripple.

Figure 22. White LED Supply With Adjustable Brightness Control Using an Analog Signal on the Feedback Pin

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10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8 V and 6 V. The output current of the input power supply must be rated according to the supply voltage, output voltage and output current of TPS6104x.

11 Layout

11.1 Layout Guidelines

Typical for all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

The input capacitor should be placed as close as possible to the input pin for good input voltage filtering. The inductor and diode should be placed as close as possible to the switch pin to minimize the noise coupling into other circuits. Because the feedback pin and network is a high-impedance circuit, the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

Wide traces should be used for connections in bold as shown in Figure 23. A star ground connection or ground plane minimizes ground shifts and noise.

11.2 Layout Example

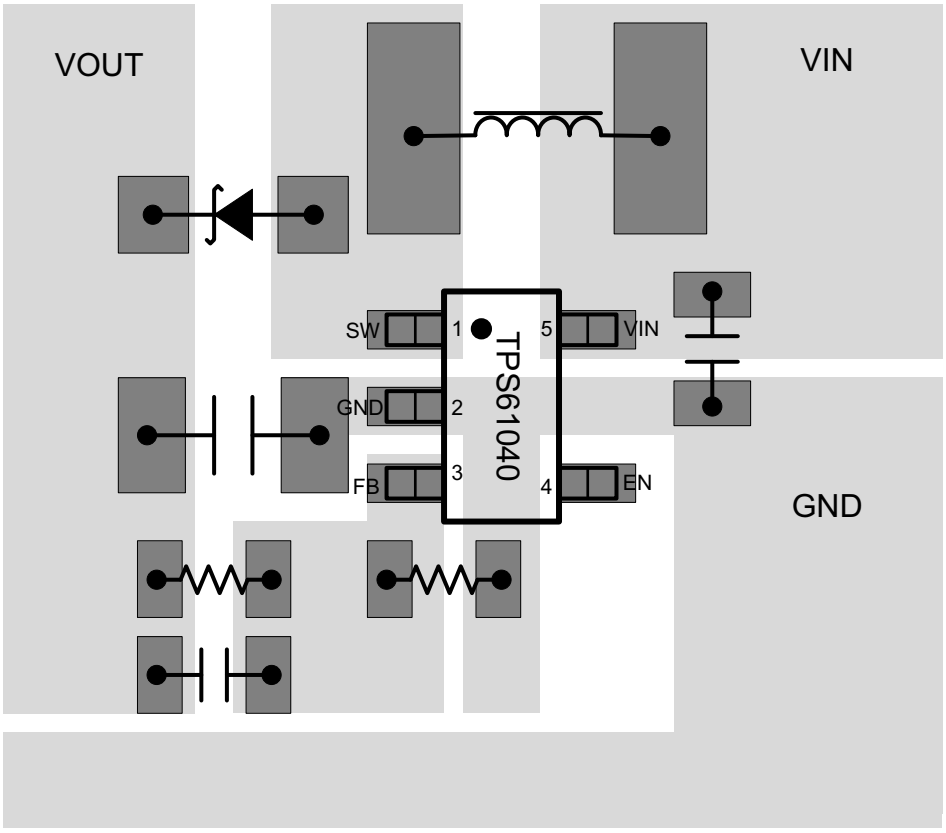


Figure 23. Layout Diagram

12 Device and Documentation Support

12.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61041	Click here	Click here	Click here	Click here	Click here
TPS61040	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61040DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHOI	Samples
TPS61040DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHOI	Samples
TPS61040DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QXK	Samples
TPS61040DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QXK	Samples
TPS61040DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCL	Samples
TPS61040DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCL	Samples
TPS61040DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CCL	Samples
TPS61041DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHPI	Samples
TPS61041DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHPI	Samples
TPS61041DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CAW	Samples
TPS61041DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CAW	Samples
TPS61041DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CAW	Samples
TPS61041DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CAW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS61040, TPS61041 :

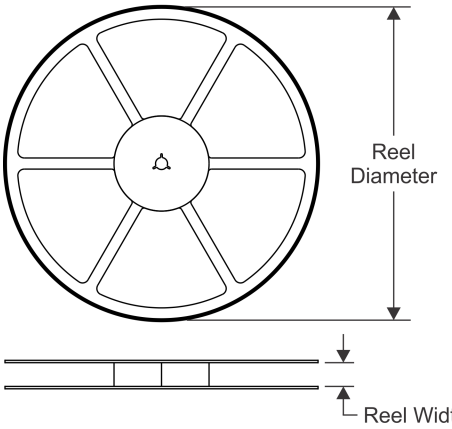
- Automotive: TPS61040-Q1, TPS61041-Q1

NOTE: Qualified Version Definitions:

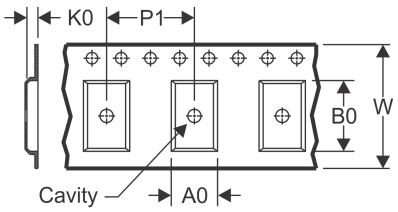
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

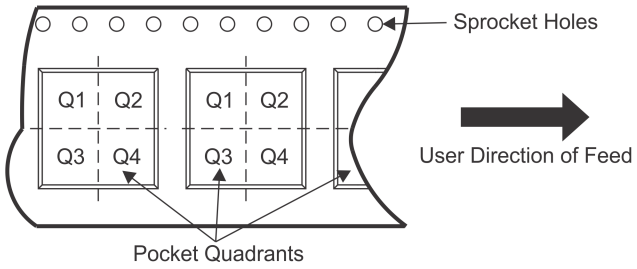


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

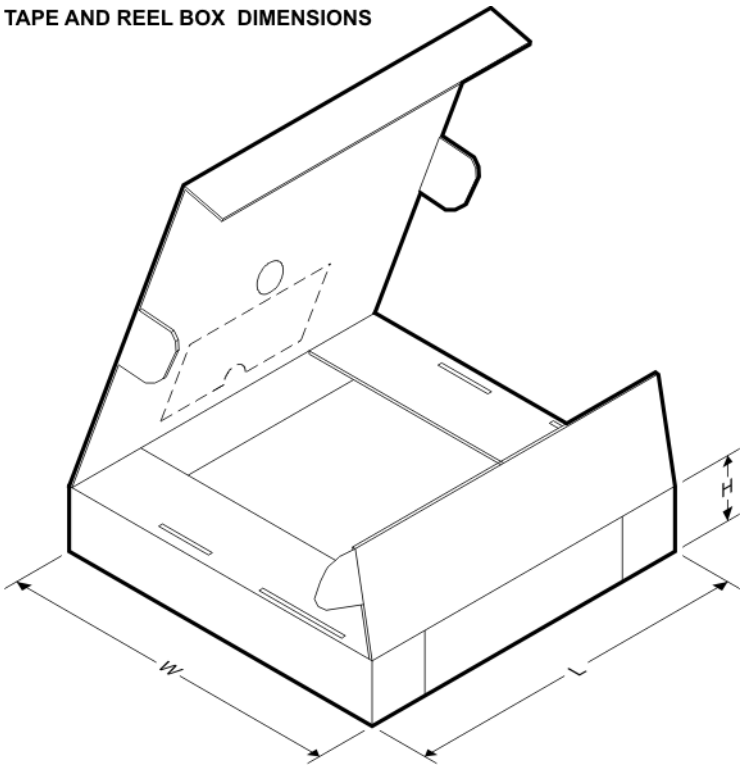
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61040DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS61040DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS61040DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS61040DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS61040DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS61040DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS61041DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS61041DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS61041DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

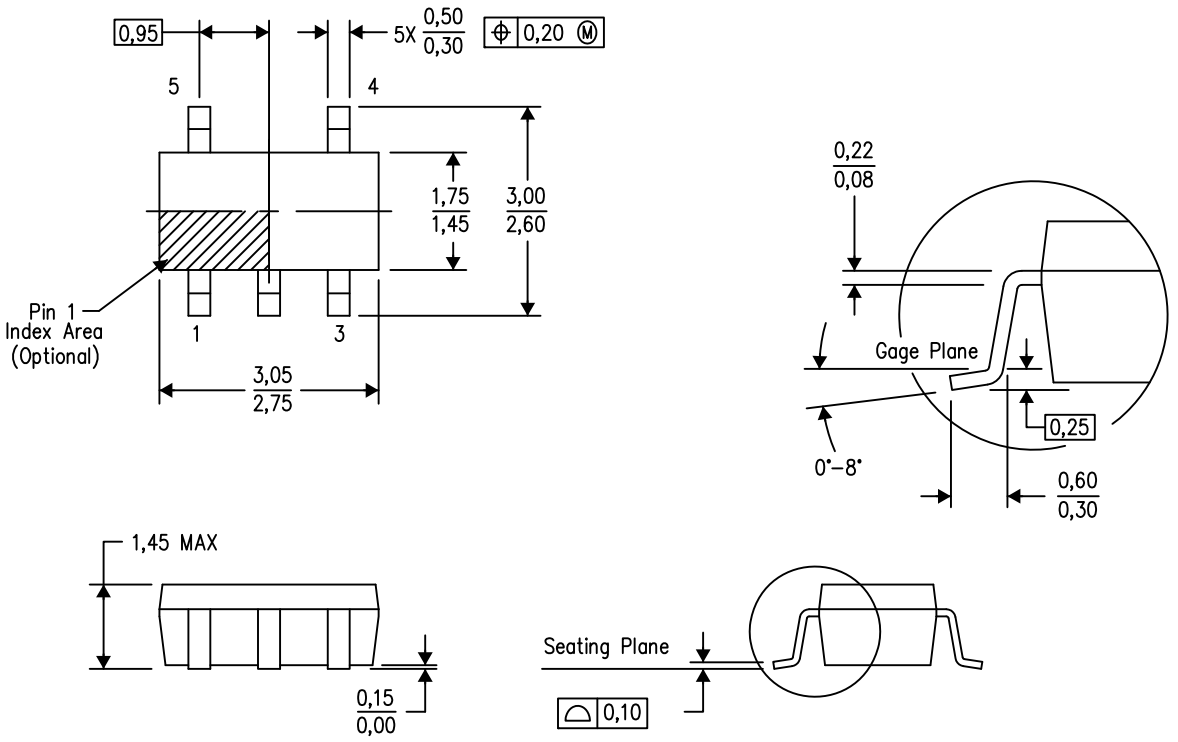
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61040DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS61040DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS61040DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS61040DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS61040DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS61040DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS61041DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS61041DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS61041DRVR	SON	DRV	6	3000	203.0	203.0	35.0

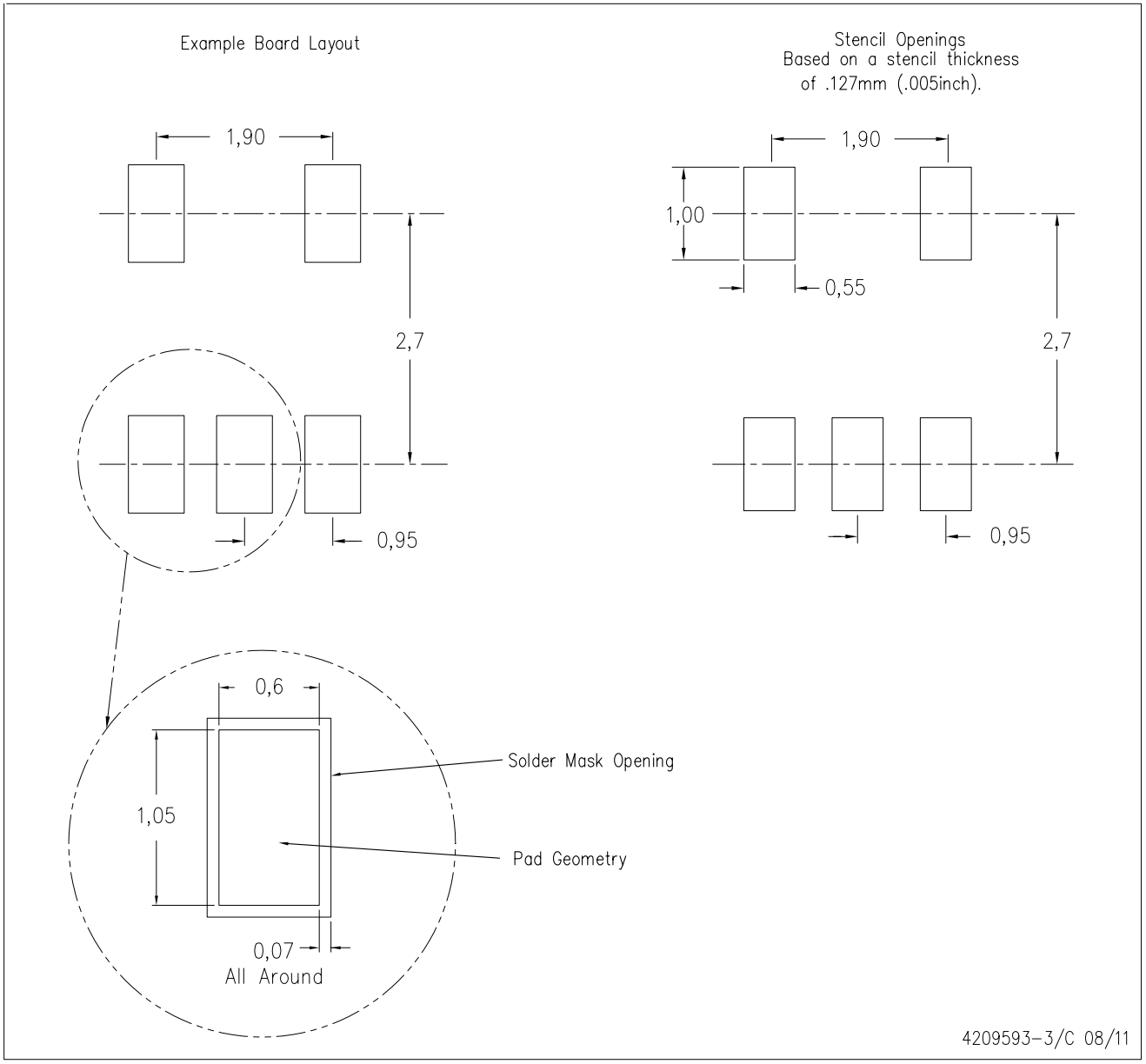
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

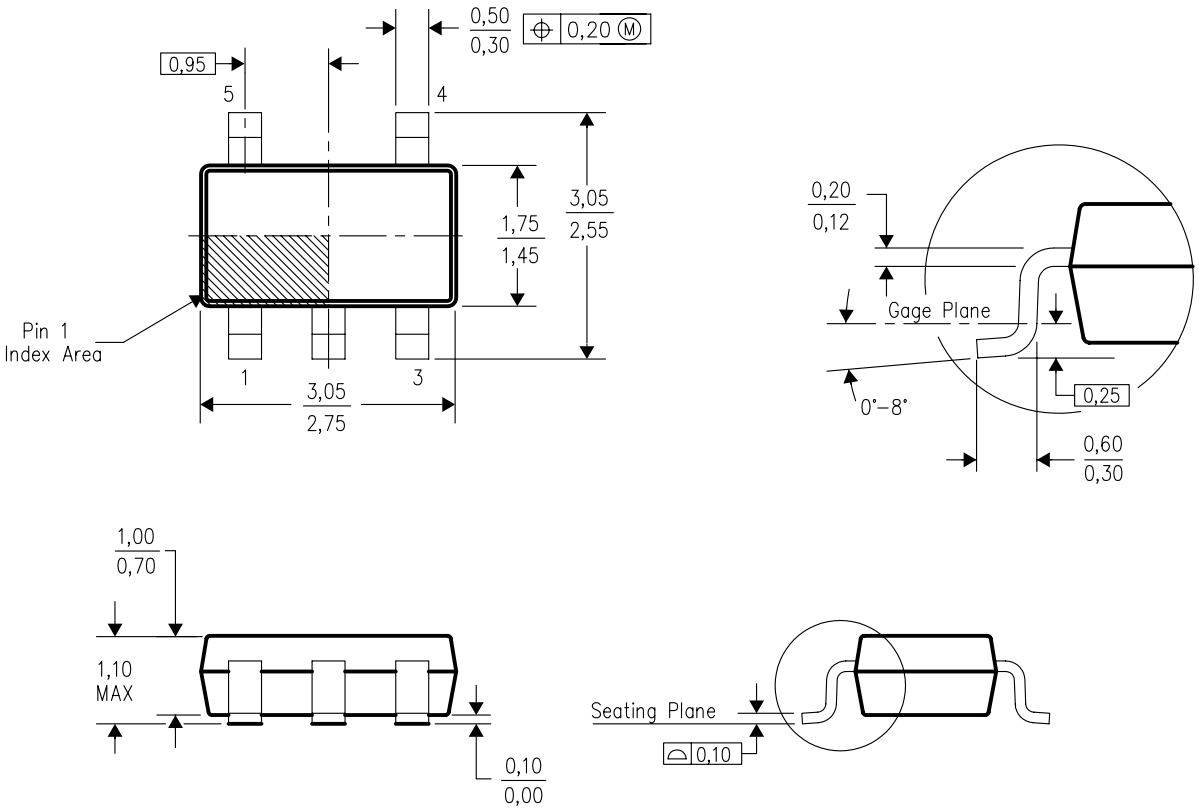
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

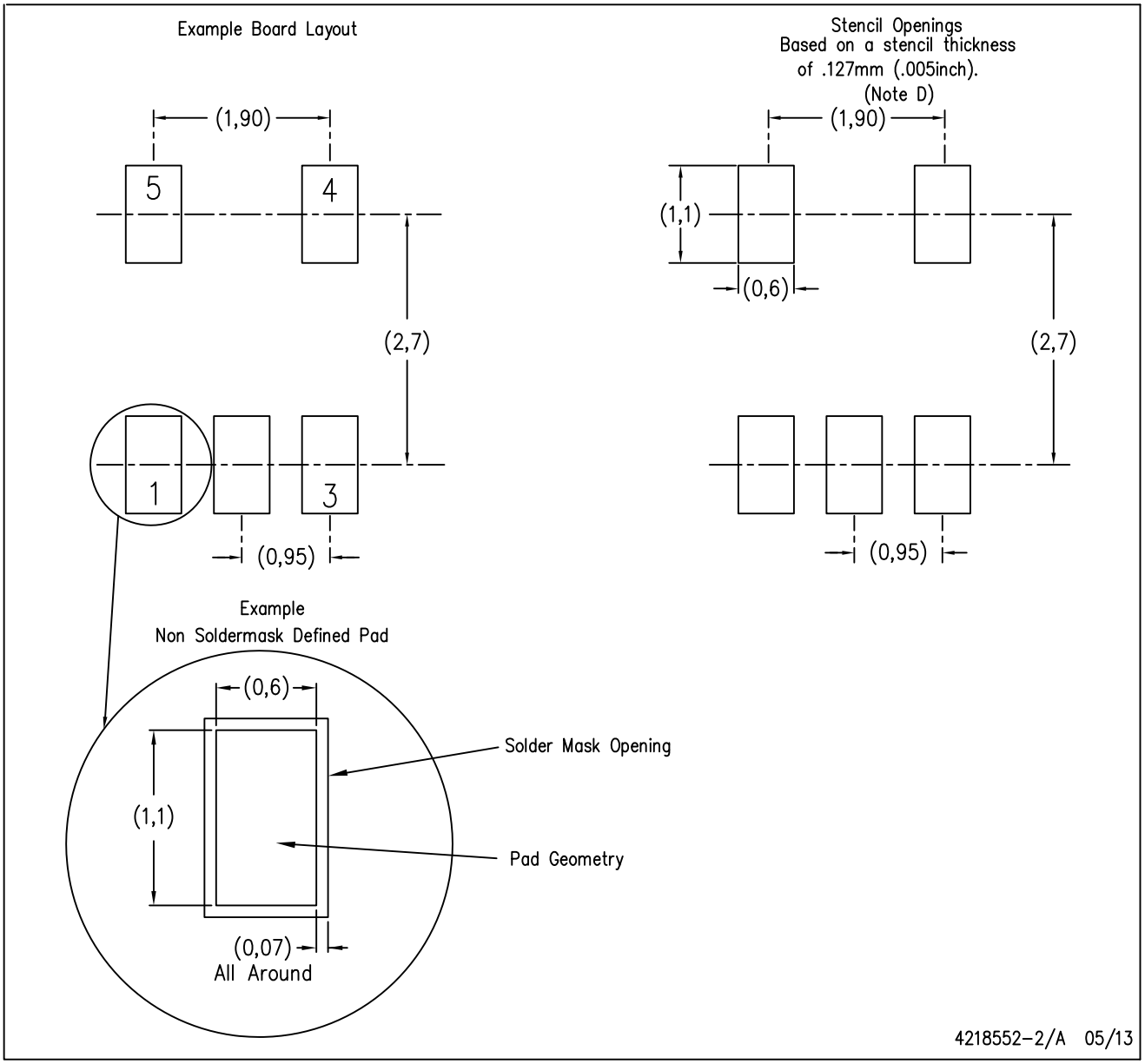
DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



4204403–2/E 06/05

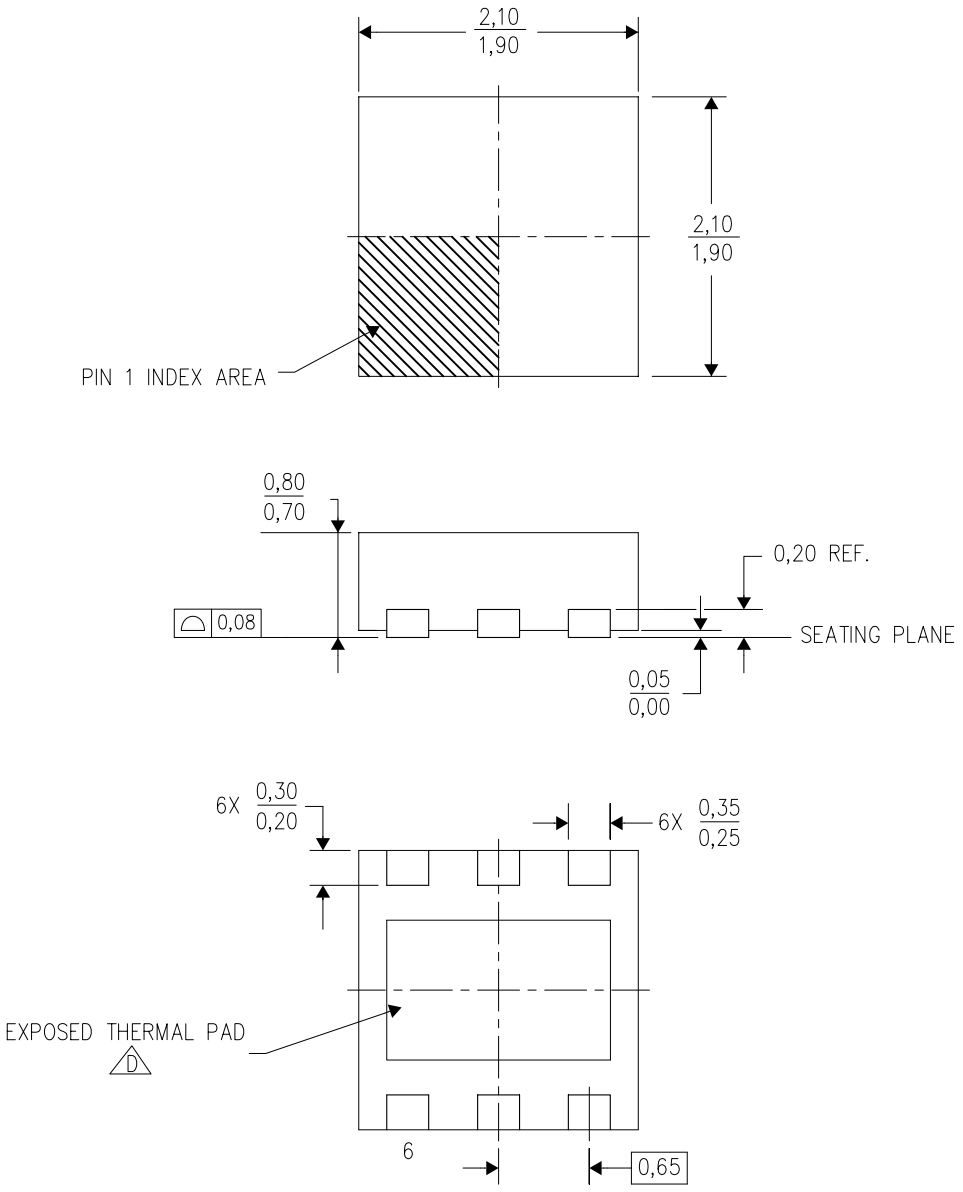
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

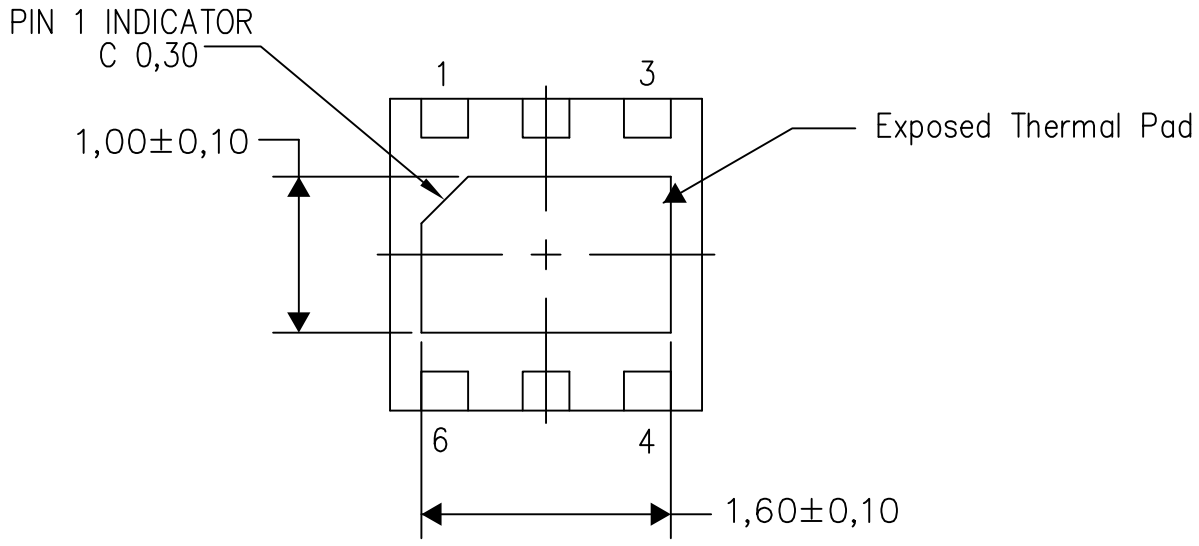
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



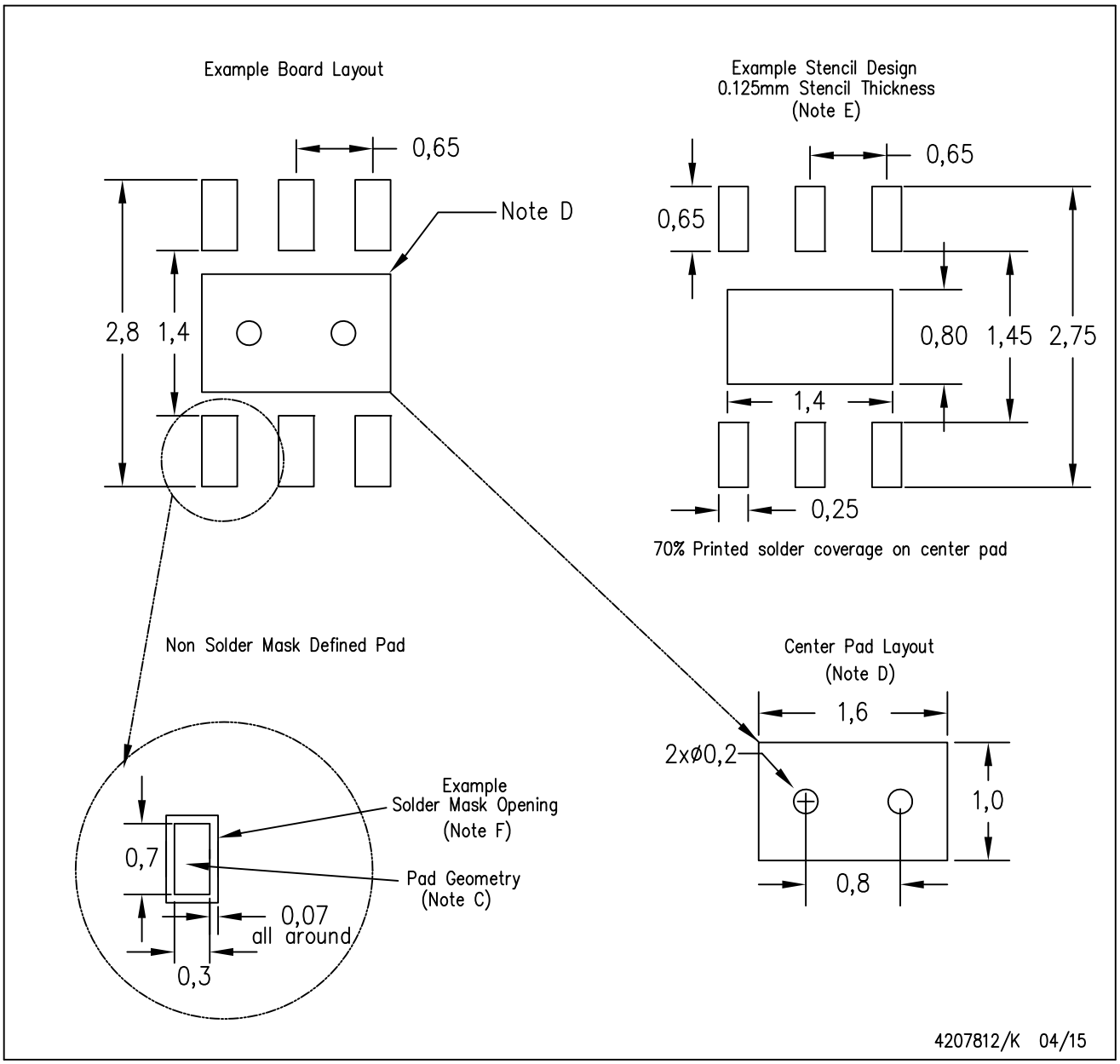
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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