# CURRENT-LIMITED POWER-DISTRIBUTION SWITCH

**Check for Samples: TPS2068-Q1**

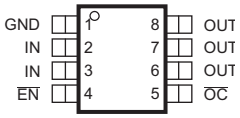
## FEATURES

- **Qualified for Automotive Applications**
- **70-mΩ High-Side MOSFET**
- **1.5-A Continuous Current**
- **Thermal and Short-Circuit Protection**
- **Accurate Current Limit (1.6 A Min, 2.6 A Max)**
- **Operating Range: 2.7 V to 5.5 V**
- **0.6-ms Typical Rise Time**
- **Undervoltage Lockout**
- **Deglitched Fault Report ($\overline{OC}$)**
- **No $\overline{OC}$ Glitch During Power Up**
- **1-µA Maximum Standby Supply Current**
- **Reverse Current Blocking**
- **UL Listed – File No. E169910**
- **CB Certified**

## APPLICATIONS

- **Heavy Capacitive Loads**
- **Short-Circuit Protections**

**DGN PACKAGE**
**(TOP VIEW)**




## DESCRIPTION

The TPS2068 power-distribution switches are intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates 70-mΩ N-channel MOSFET power switches for power-distribution systems that require single or dual power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OC}$) logic output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. Current limit is typically 2.1 A.

**GENERAL SWITCH CATALOG**

| 33 mΩ, Single | 80 mΩ, Single | 80 mΩ, Dual | 80 mΩ, Dual | 80 mΩ, Triple | 80 mΩ, Quad | 80 mΩ, Quad |
|---|---|---|---|---|---|---|
| TPS201xA 0.2 A to 2 A | TPS2014 600 mA | TPS2042B 500 mA | TPS2080 500 mA | TPS2043B 500 mA | TPS2044B 500 mA | TPS2085 500 mA |
| TPS202x 0.2 A to 2 A | TPS2015 1 A | TPS2052B 500 mA | TPS2081 500 mA | TPS2053B 500 mA | TPS2054B 500 mA | TPS2086 500 mA |
| TPS203x 0.2 A to 2 A | TPS2041B 500 mA | TPS2046B 250 mA | TPS2082 500 mA | TPS2047B 250 mA | TPS2048A 250 mA | TPS2087 500 mA |
| | TPS2051B 500 mA | TPS2056 250 mA | TPS2090 250 mA | TPS2057A 250 mA | TPS2058 250 mA | TPS2095 250 mA |
| | TPS2045A 250 mA | TPS2062 1 A | TPS2091 250 mA | TPS2063 1 A | | TPS2096 250 mA |
| | TPS2049 100 mA | TPS2066 1 A | TPS2092 250 mA | TPS2067 1 A | | TPS2097 250 mA |
| | TPS2055A 250 mA | TPS2060 1.5 A | | | | |
| | TPS2061 1 A | TPS2064 1.5 A | | | | |
| | TPS2065 1 A | | | | | |
| | TPS2068 1.5 A | | | | | |
| | TPS2069 1.5 A | | | | | |

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE (2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | MSOP – DGN | Reel of 2500 | TPS2068IDGNRQ1 | PSQQ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | | |
|---|---|---|---|
| $V_I$ | Input voltage range, $V_{I(IN)}$ | | –0.3 V to 6 V |
| | Input voltage range, $V_{I(\overline{EN})}$ | | –0.3 V to 6 V |
| | Voltage range, $V_{I(\overline{OC})}$ | | –0.3 V to 6 V |
| $V_O$ | Output voltage range, $V_{O(OUT)}$ | | –0.3 V to 6 V |
| $I_O$ | Continuous output current , $I_{O(OUT)}$ | | Internally limited |
| | Continuous total power dissipation | | See Dissipation Rating Table |
| $T_J$ | Operating virtual-junction temperature range | | –40°C to 105°C |
| $T_{stg}$ | Storage temperature range | | –65°C to150°C |
| ESD | Electrostatic discharge protection | Human-body model (HBM) | 1500 V |
| | | Machine model (MM) | 50 V |
| | | Charged-device model (CDM) | 1000 V |

(1) Stresses beyond those listed under *absolute maximum ratings*may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATING RATING TABLE(1)

| PACKAGE | $T_A$ < 25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|
| DGN-8(2) | 1370 mW | 17 mW/°C | 600 mW | 342 mW |

(1) Heatsink the PowerPad™per the recommendations of SLMA002. PCB used for recommendations per appendix A4.
(2) See *Recommended Operating Conditions* Table for PowerPad connection guidelines to meet qualifying conditions for CB Certificate.

## RECOMMENDED OPERATING CONDITIONS(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_I$ | Input voltage, $V_{I(IN)}$ | 2.7 | 5.5 | V |
| | Input voltage, $V_{I(\overline{EN})}$ | 0 | 5.5 | V |
| $I_O$ | Continuous output current, $I_{O(OUT)}$ | 0 | 1.5 | A |
| $T_J$ | Operating virtual-junction temperature | –40 | 105 | °C |

(1) The thermal pad must be connected externally to GND pin to meet qualifying conditions for CB Certificate (DGN package only).


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## ELECTRICAL CHARACTERISTICS

–40°C ≤ $T_J$ ≤ 105° $V_{I(IN)}$ = 5.5 V, $I_O$ = 1 A, $V_{I(\overline{EN})}$ = 0 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS (1) | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | | |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 5-V operation and 3.3-V operation | $V_{I(IN)}$ = 5 V or 3.3 V, $I_O$ = 1.5 A | | | | 70 | 150 | mΩ |
| | Static drain-source on-state resistance, 2.7-V operation | $V_{I(IN)}$ = 2.7 V, $I_O$ = 1.5 A | | | | 75 | 150 | mΩ |
| $t_r$ | Rise time, output (2) | $V_{I(IN)}$ = 5.5 V | $C_L$ = 1 µF, $R_L$ = 5 Ω | $T_J$ =25°C | | 0.6 | 1.5 | ms |
| | | $V_{I(IN)}$ = 2.7 V | | | | 0.4 | 1 | |
| $t_f$ | Fall time, output (2) | $V_{I(IN)}$ = 5.5 V | | | 0.05 | | 0.5 | |
| | | $V_{I(IN)}$ = 2.7 V | | | 0.05 | | 0.5 | |
| **ENABLE INPUT $\overline{EN}$** | | | | | | | | |
| $V_{IH}$ | High-level input voltage | 2.7 V < $V_{I(IN)}$ < 5.5 V | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | 2.7 V < $V_{I(IN)}$ < 5.5 V | | | | | 0.8 | |
| $I_I$ | Input current | $V_{I(\overline{EN})}$ = 0 V or 5.5 V | | | -0.5 | | 0.5 | µA |
| $t_{on}$ | Turn-on time (2) | $C_L$ = 100 µF, $R_L$ = 5 Ω | | | | | 3 | ms |
| $t_{off}$ | Turn-off time (2) | $C_L$ = 100 µF, $R_L$ = 5 Ω | | | | | 10 | |
| **CURRENT LIMIT** | | | | | | | | |
| $I_{OS}$ | Short-circuit output current | $V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short-circuit | | | 1.6 | 2.1 | 2.6 | A |
| $I_{OC_TRIP}$ | Overcurrent trip threshold (2) | $V_{I(IN)}$ = 5 V, Current ramp (≤ 100 A/s) on OUT | | | 2.3 | 2.85 | 3.4 | A |
| $I_{OS}$ (3) | Short-circuit output current (2) | $V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short-circuit, current measured at $V_{I(IN)}$ | | | 3.2 | 4.2 | 5.2 | A |
| $I_{OL}$ | Supply current, low-level output | No load on OUT, $V_{I(\overline{EN})}$ = 5.5 V | | $T_J$ = 25°C | | 0.5 | 1 | µA |
| | | | | Over $T_J$ range | | 0.5 | 5 | |
| $I_{OH}$ | Supply current, high-level output | No load on OUT, $V_{I(\overline{EN})}$ = 0 V | | $T_J$ = 25°C | | 43 | 60 | µA |
| | | | | Over $T_J$ range | | 43 | 70 | |
| $I_{lkg}$ | Leakage current | OUT connected to ground, $V_{I(\overline{EN})}$ = 5.5 V | | | | 1 | | µA |
| | Reverse leakage current | $V_{I(OUT)}$ = 5.5 V, IN = ground | | $T_J$ = 25°C | | 0.2 | | µA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | | | |
| | Low-level input voltage, IN | | | | 2 | | 2.5 | V |
| | Hysteresis, IN | $T_J$ = 25°C | | | | 75 | | mV |
| **OVERCURRENT $\overline{OC}$** | | | | | | | | |
| $V_{OL(\overline{OC})}$ | Output low voltage | $I_{O(\overline{OC})}$ = 5 mA | | | | | 0.4 | V |
| | Off-state current | $V_{O(\overline{OC})}$ = 5 V or 3.3 V | | | | | 1 | µA |
| | $\overline{OC}$ deglitch (2) | $\overline{OC}$ assertion or deassertion | | | 4 | 8 | 15 | ms |
| **THERMAL SHUTDOWN (4)** | | | | | | | | |
| | Thermal shutdown threshold (2) | | | | 135 | | | °C |
| | Recovery from thermal shutdown (2) | | | | 125 | | | °C |
| | Hysteresis | | | | | 10 | | °C |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Specified by design
(3) This configuration has not been tested for UL certification.
(4) The thermal shutdown only reacts under overcurrent conditions.

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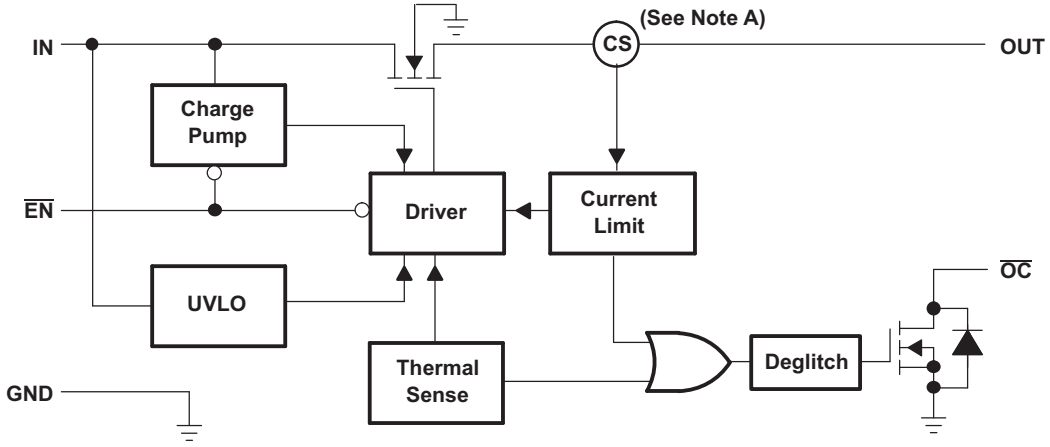
# DEVICE INFORMATION

## Terminal Functions

| NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| $\overline{EN}$ | 4 | I | Enable input, logic low turns on power switch |
| GND | 1 | | Ground |
| IN | 2,3 | I | Input voltage |
| $\overline{OC}$ | 5 | O | Overcurrent, open-drain output, active-low |
| OUT | 6, 7,8 | O | Power-switch output |
| Thermal pad | | | Connect to GND(1) |

(1) See the *Recommended Operating Conditions* Table for PowerPad connection guidelines to meet qualifying conditions for CB Certificate (DGN package only).

## Functional Block Diagram




A. Current sense.


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## PARAMETER MEASUREMENT INFORMATION

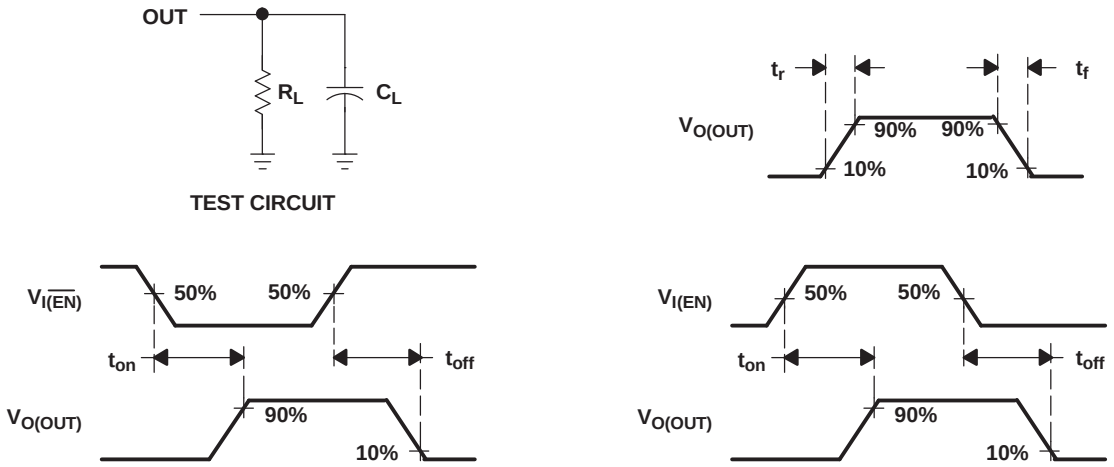
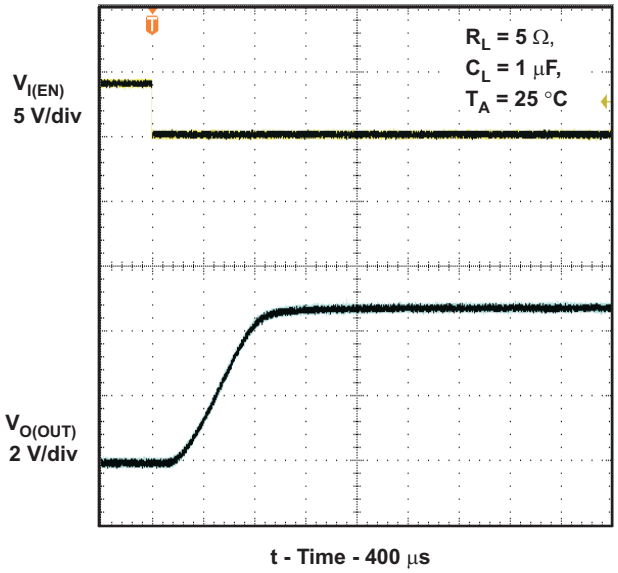
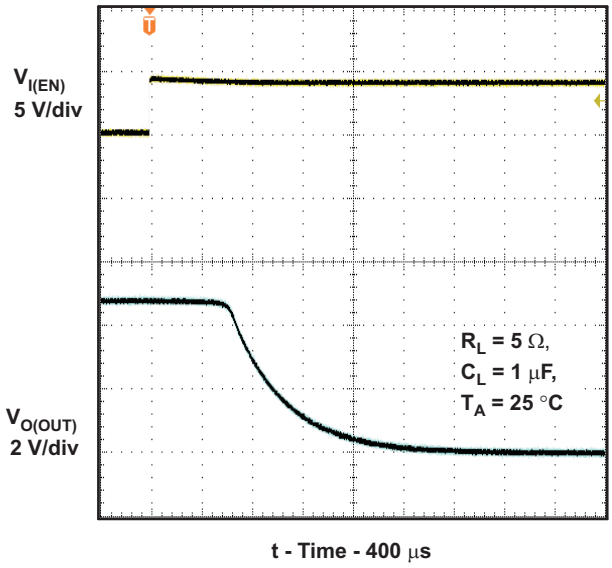
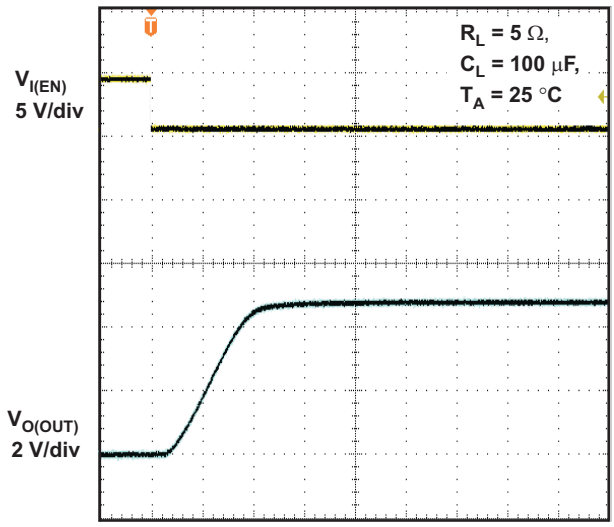


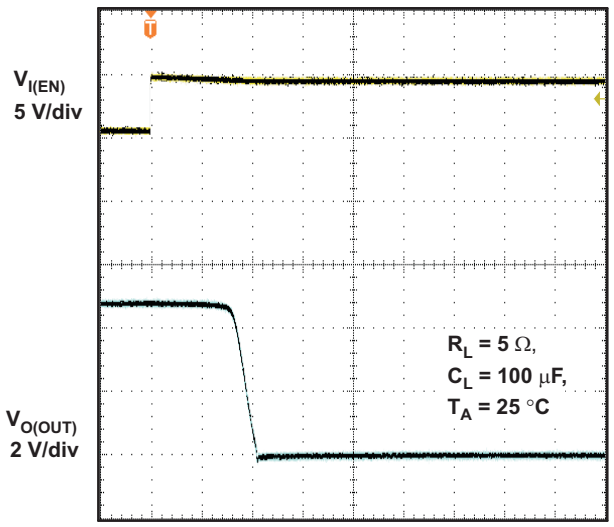

**Figure 1. Test Circuit and Voltage Waveforms**

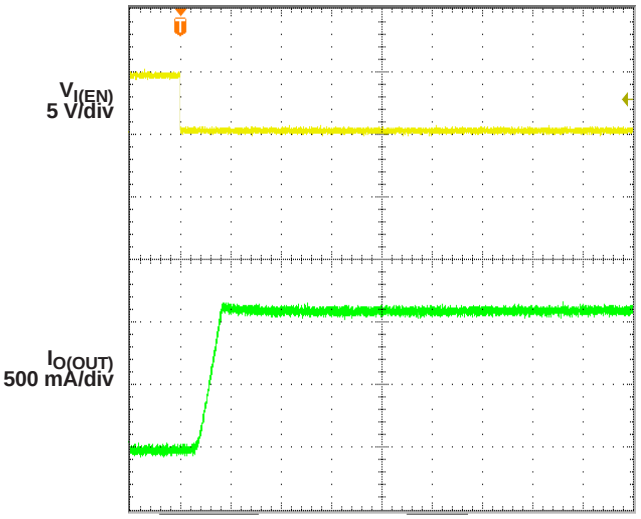


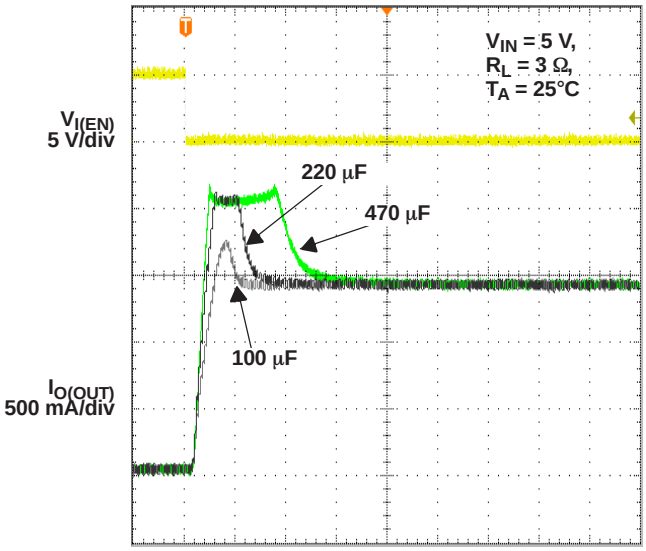



## PARAMETER MEASUREMENT INFORMATION (continued)



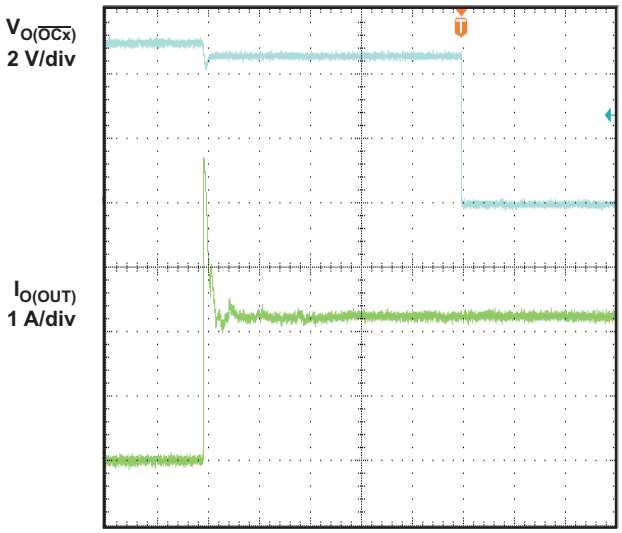





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## PARAMETER MEASUREMENT INFORMATION (continued)



## TYPICAL CHARACTERISTICS

**TURNON TIME vs INPUT VOLTAGE**

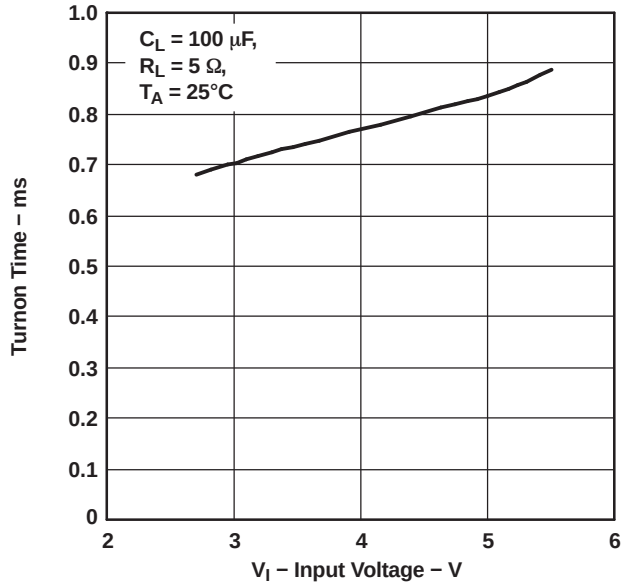



Figure 9.

**TURNOFF TIME vs INPUT VOLTAGE**

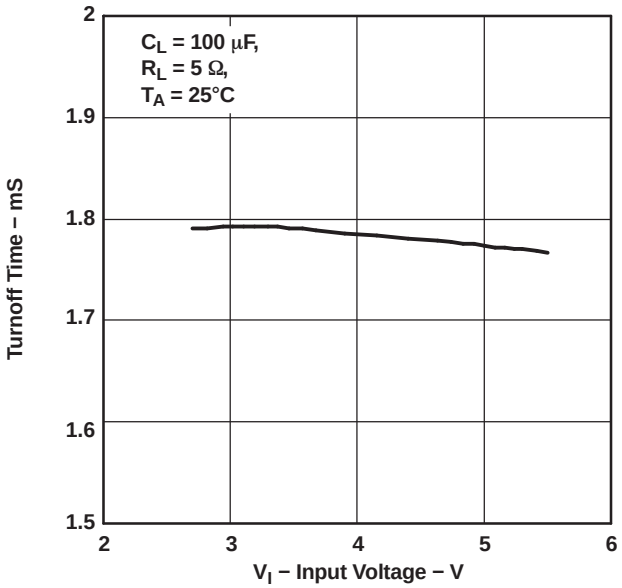



Figure 10.

**RISE TIME vs INPUT VOLTAGE**

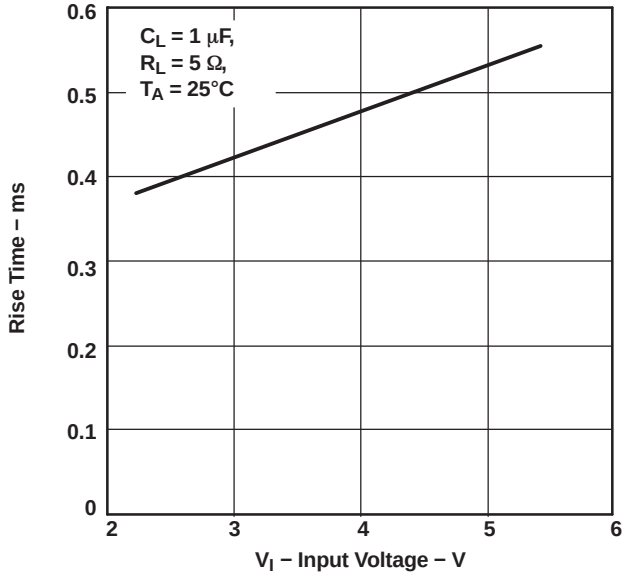



Figure 11.

**FALL TIME vs INPUT VOLTAGE**

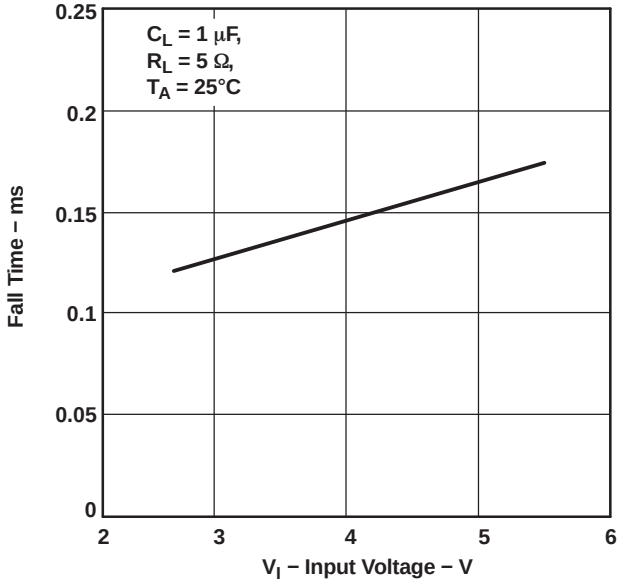



Figure 12.


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## TYPICAL CHARACTERISTICS (continued)

**SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE**

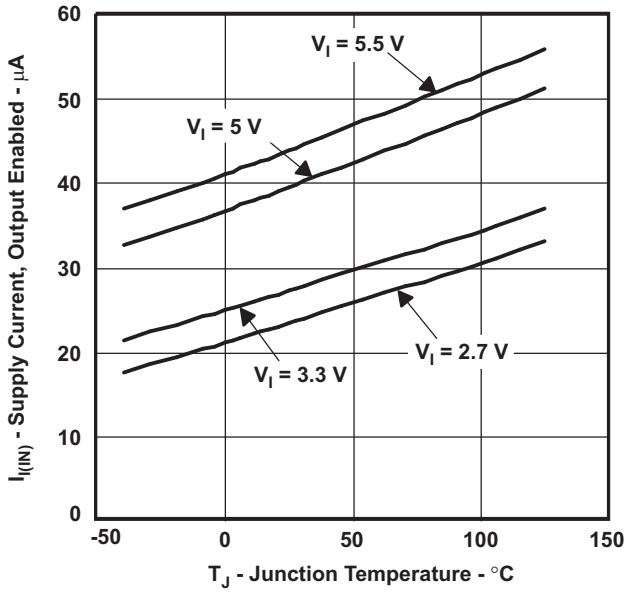



Figure 13.

**SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE**

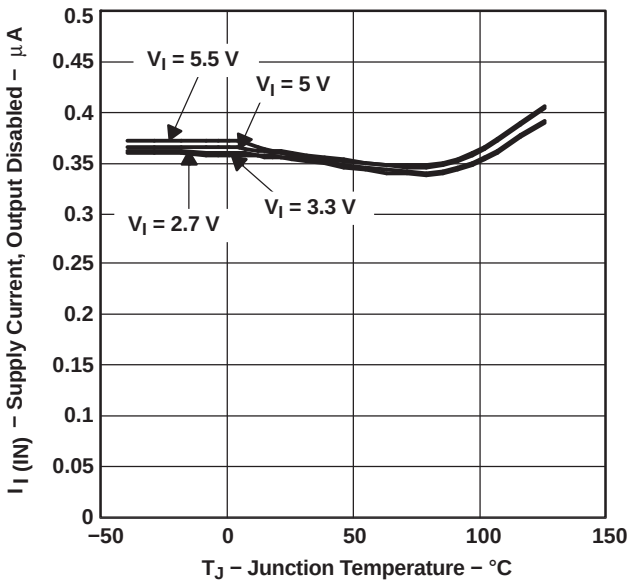



Figure 14.

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE**

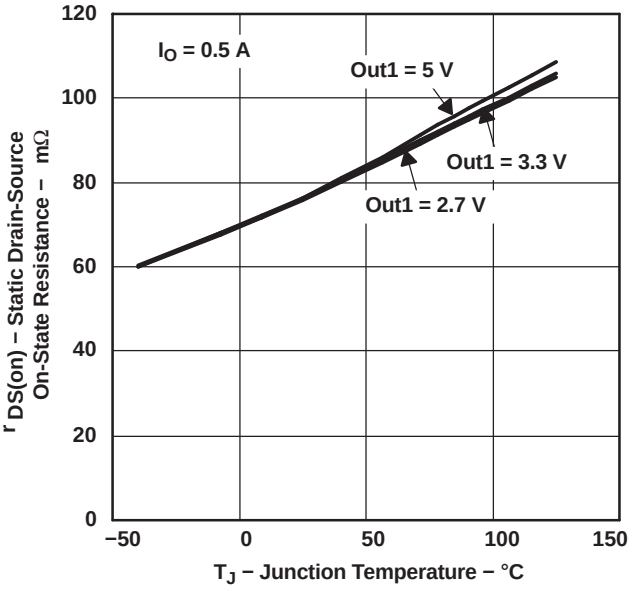



Figure 15.

**SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE**

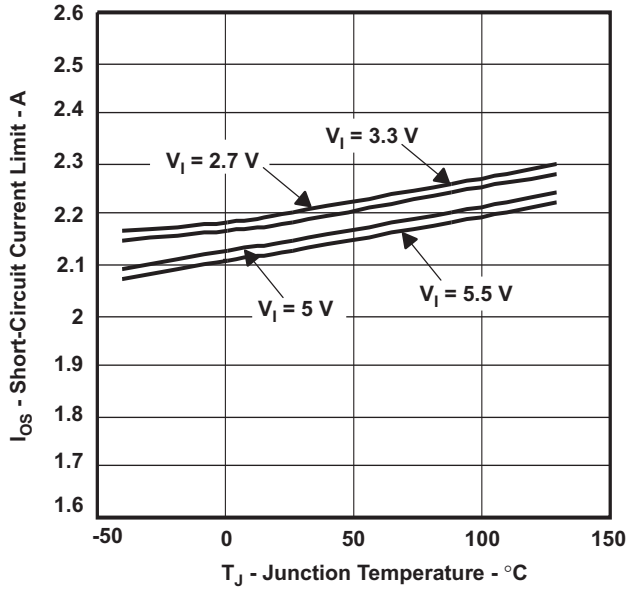



Figure 16.

## TYPICAL CHARACTERISTICS (continued)

**UNDERVOLTAGE LOCKOUT vs JUNCTION TEMPERATURE**

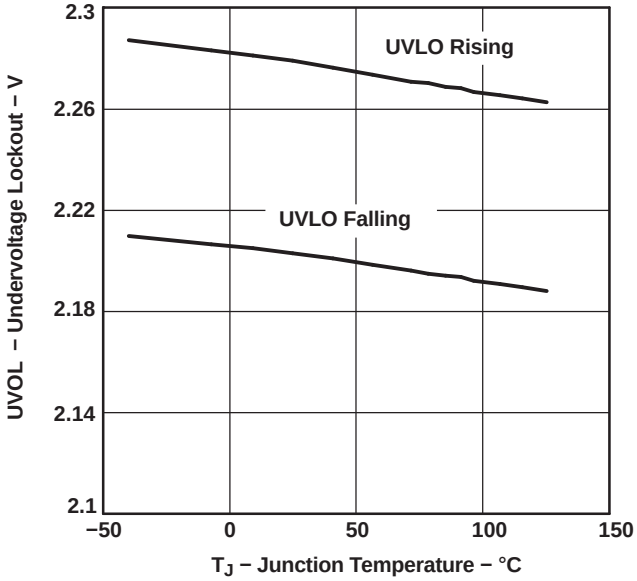



Figure 17.

**CURRENT-LIMIT RESPONSE vs PEAK CURRENT**

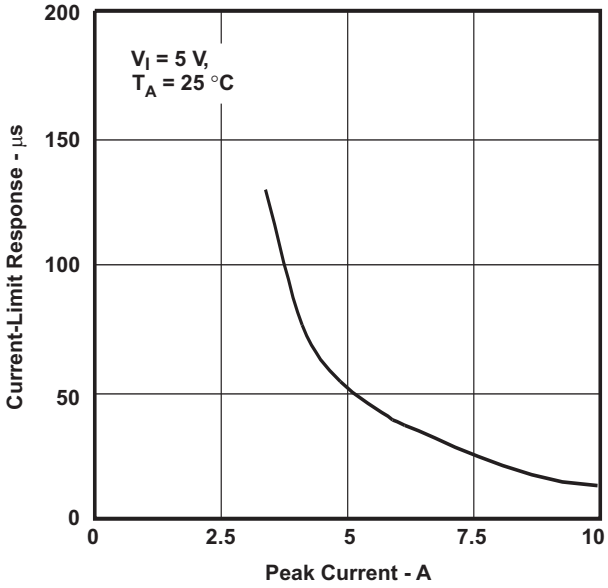



Figure 18.


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## APPLICATION INFORMATION

### Power-Supply Considerations

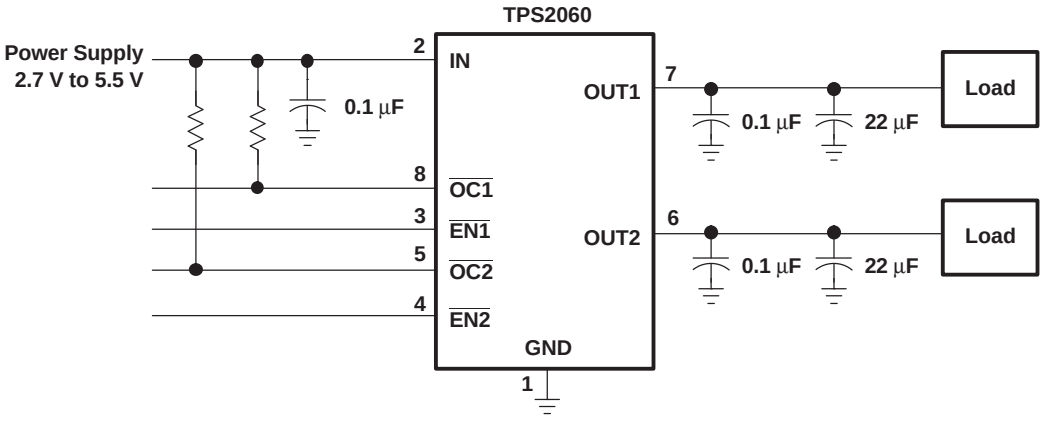



**Figure 19. Typical Application**

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

### Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS2068 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react (see Figure 8).After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS2068 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

### $\overline{\text{OC}}$ Response

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{\text{OC}}$ occurs due to the 10-ms deglitch circuit. The TPS2068 is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{\text{OC}}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

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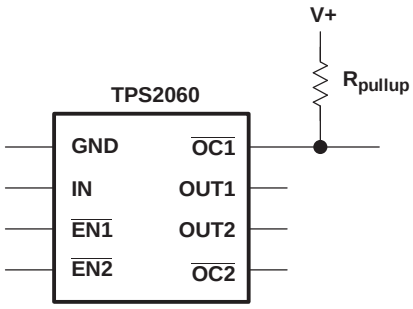



**Figure 20. Typical Circuit for the $\overline{OC}$ Pin**

## Power Dissipation and Junction Temperature

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistance of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 15. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$= Ambient temperature °C
$R_{\theta JA}$ = Thermal resistance
$P_D$ = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

## Thermal Protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS2068 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OC}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## Undervoltage Lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.


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## Universal Serial Bus (USB) Applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

SPHs and BPHs distribute data and power to downstream functions. The TPS2068 has higher current capability than required by one USB port; so, it can be used on the host side and supplies power to multiple downstream ports or functions.

## Host/Self-Powered and Bus-Powered Hubs

Hosts and SPHs have a local power supply that powers the embedded functions and the downstream ports (see Figure 21). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

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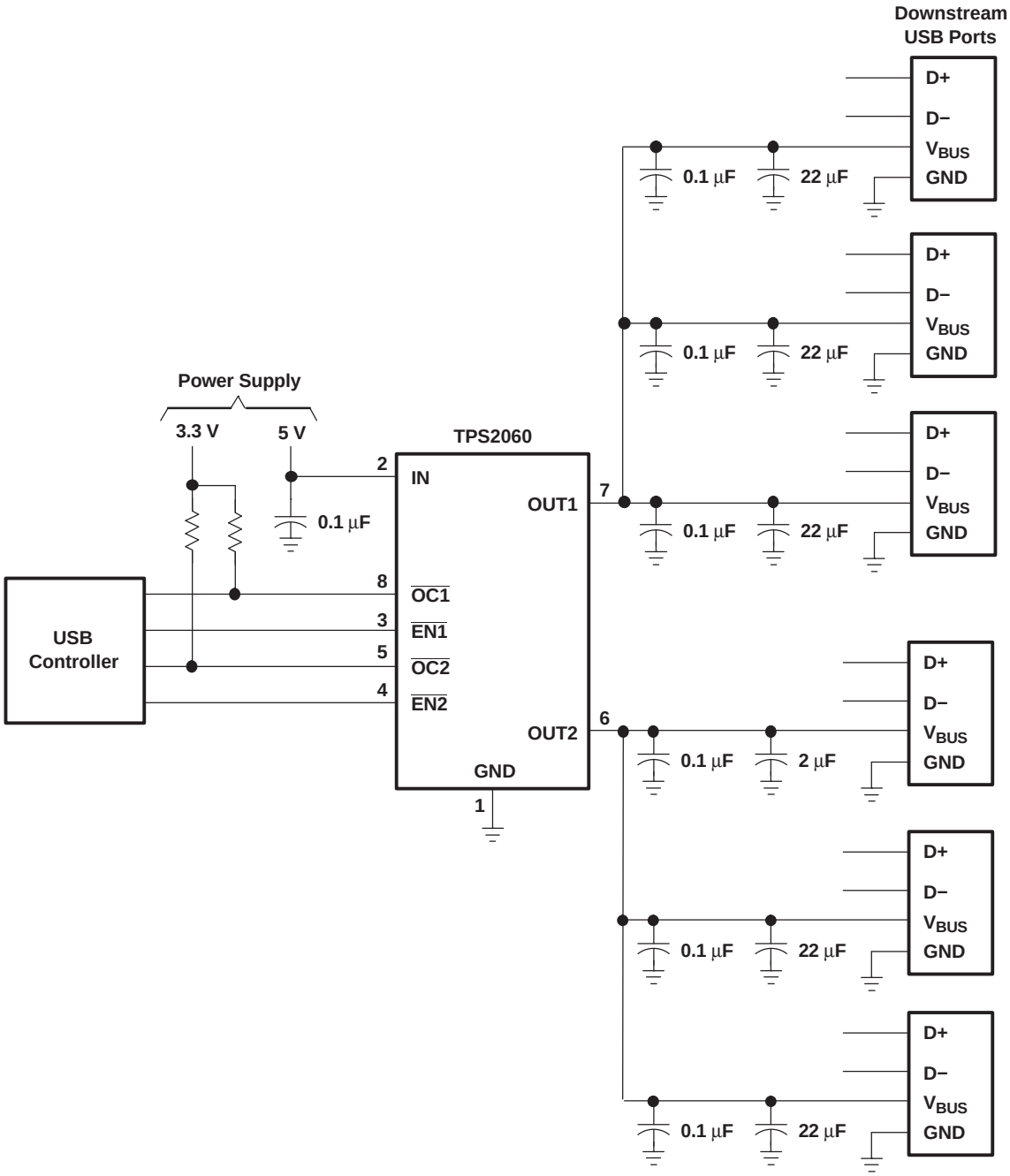



**Figure 21. Typical Six-Port USB Host/Self-Powered Hub**

BPHs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.


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## Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 22). With TPS2068, the internal functions could draw more than 500 mA, which fits the needs of some applications such as motor driving circuits.

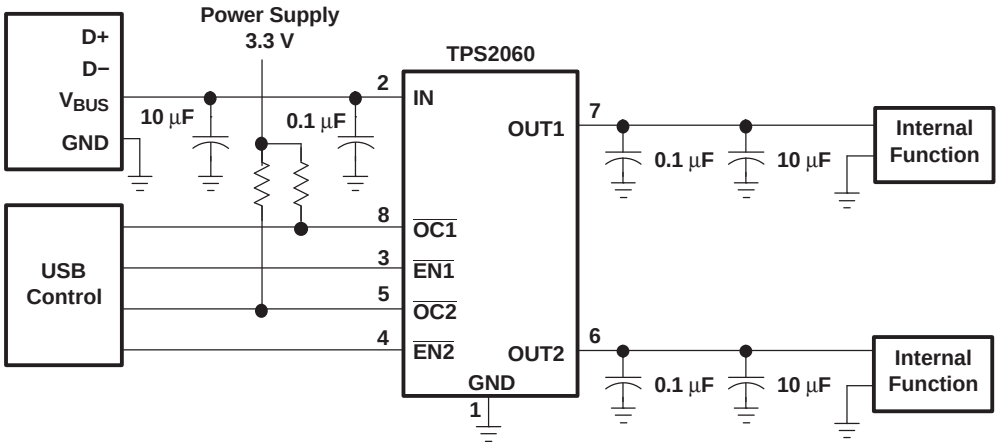



**Figure 22. High-Power Bus-Powered Function**

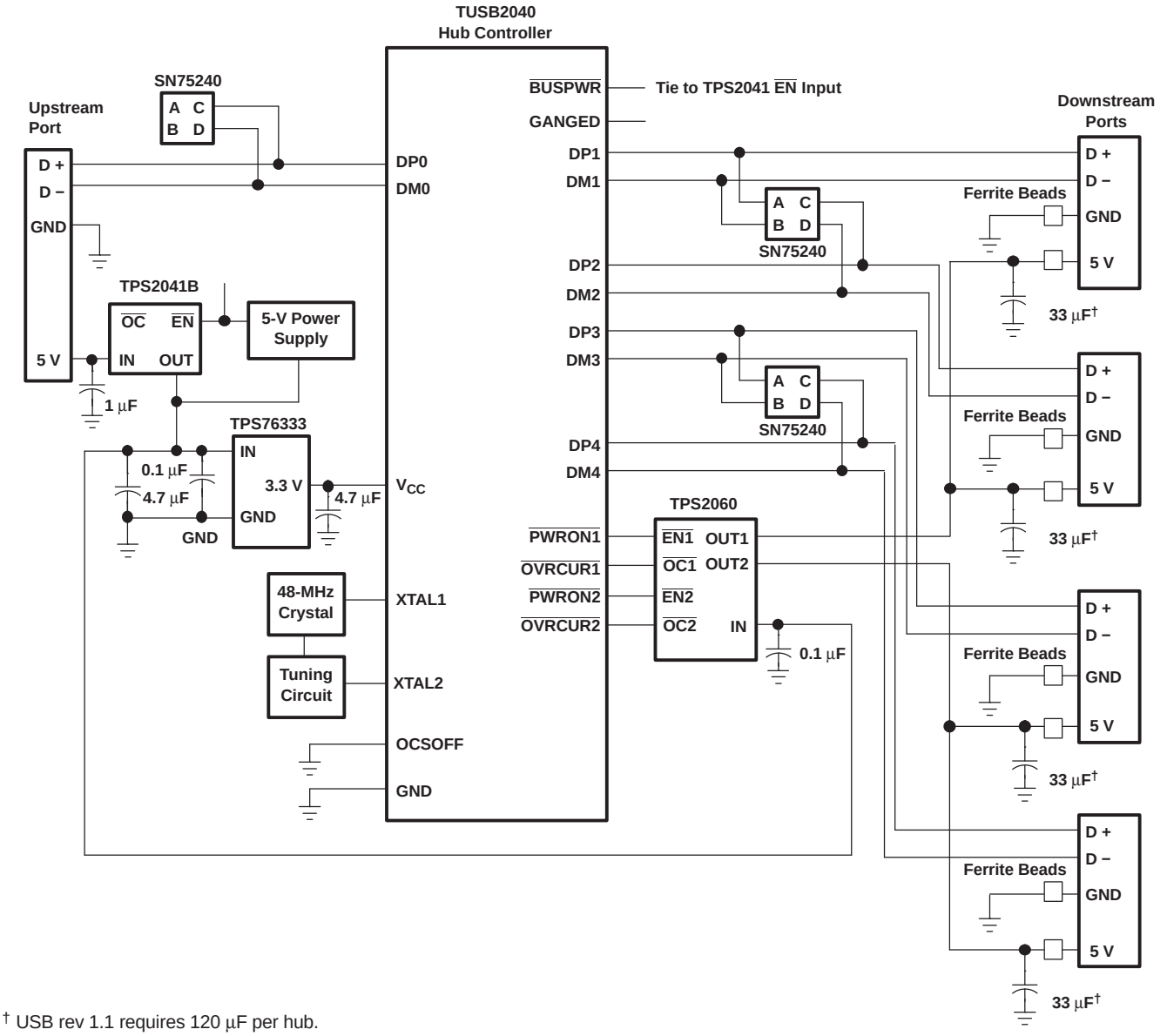
## USB Power-Distribution Requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB $V_{BUS}$
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2068 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 23).

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† USB rev 1.1 requires 120 µF per hub.

**Figure 23. Hybrid Self / Bus-Powered Hub Implementation**

## Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2068, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2068 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.


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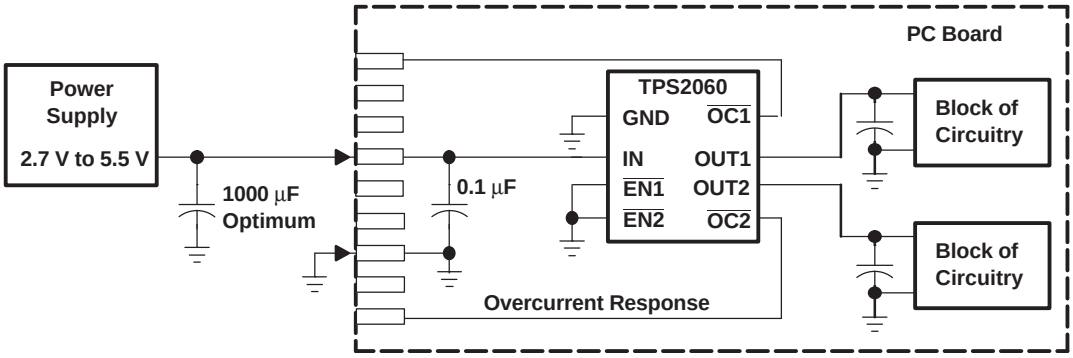



**Figure 24. Typical Hot-Plug Implementation**

By placing the TPS2068 between the $V_{CC}$ input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

## DETAILED DESCRIPTION

### Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 1.5 A.

### Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

### Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

### Enable ($\overline{EN}$)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA when a logic high is present on $\overline{EN}$. A logic zero input on $\overline{EN}$ restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

### Overcurrent ($\overline{OC}$)

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{OC}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{OC}$ is asserted instantaneously.

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## Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

## Thermal Sense

The TPS2068 implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{OC}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2068IDGNRQ1 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PSQQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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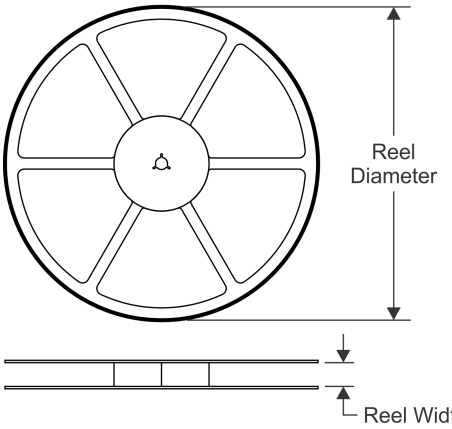
- Catalog: TPS2068

NOTE: Qualified Version Definitions:

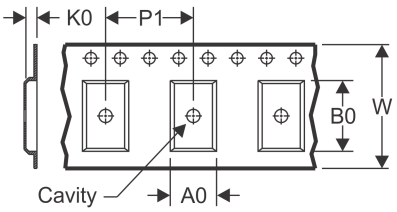
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

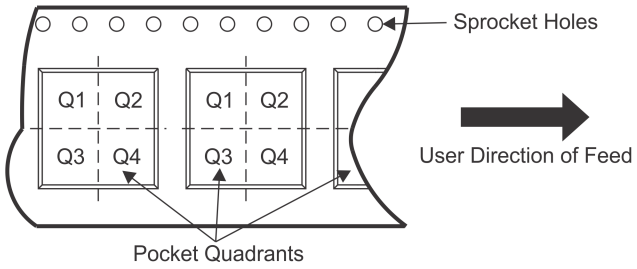



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

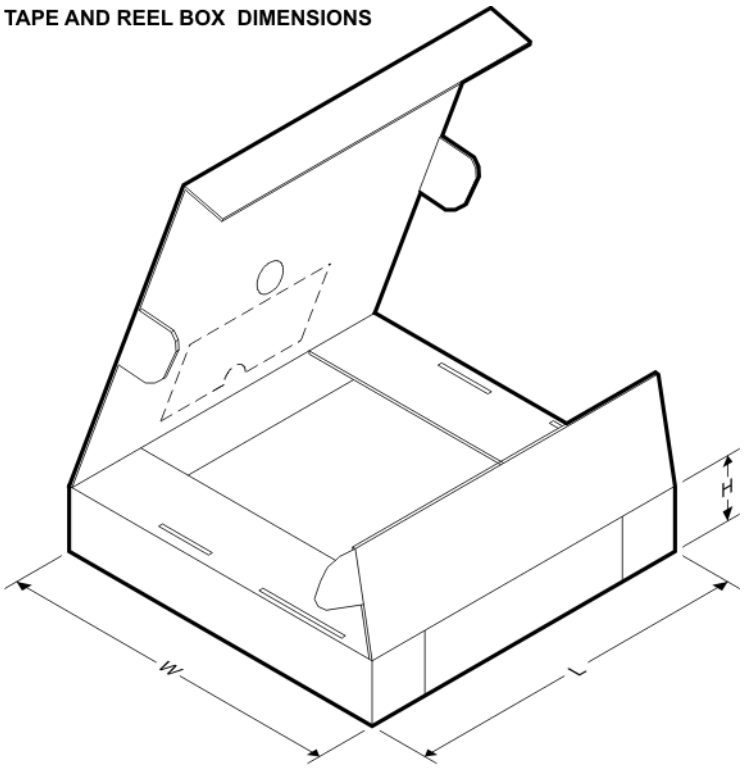
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2068IDGNRQ1 | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |

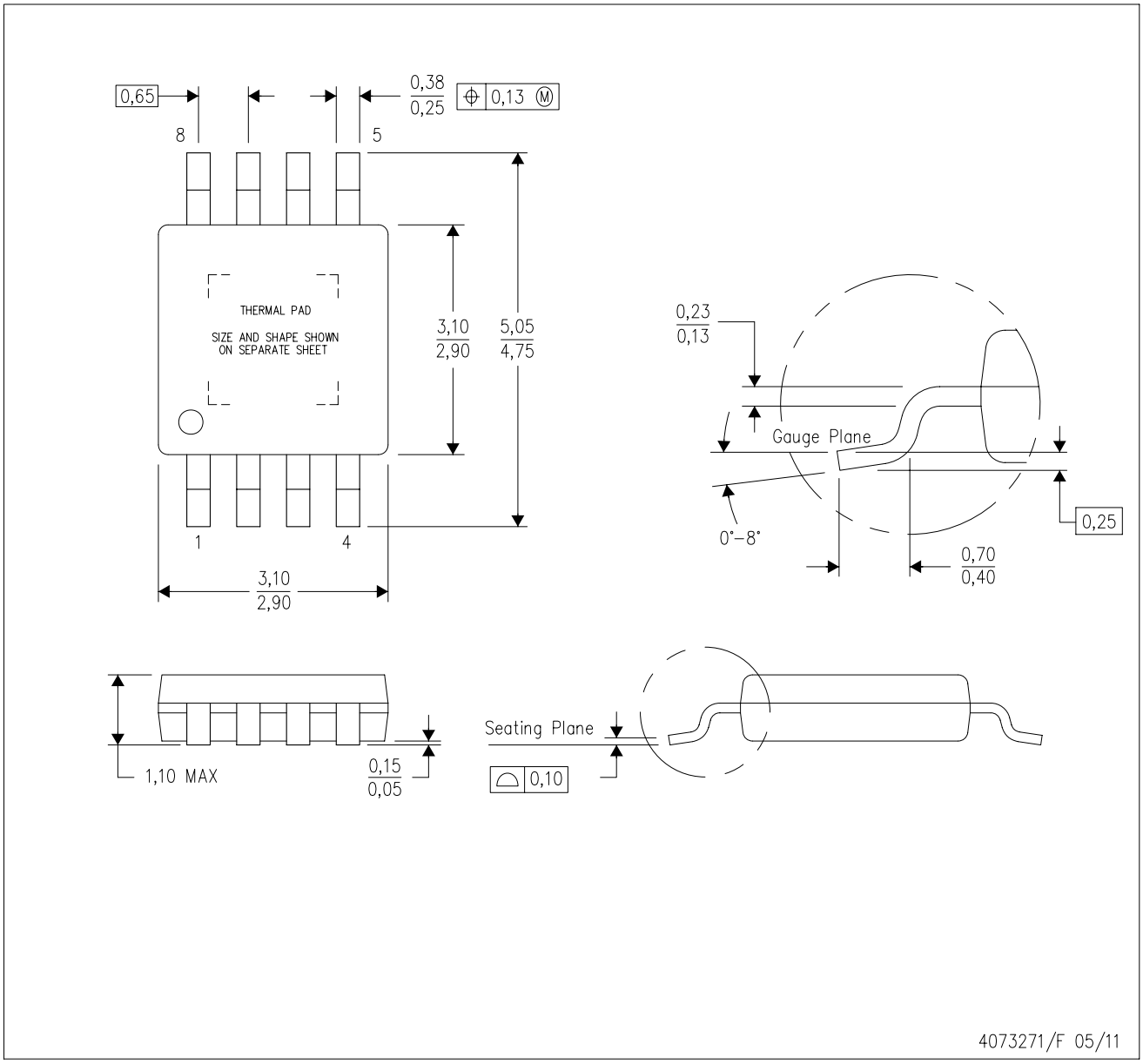
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS2068IDGNRQ1 | MSOP-PowerPAD | DGN | 8 | 2500 | 370.0 | 355.0 | 55.0 |

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

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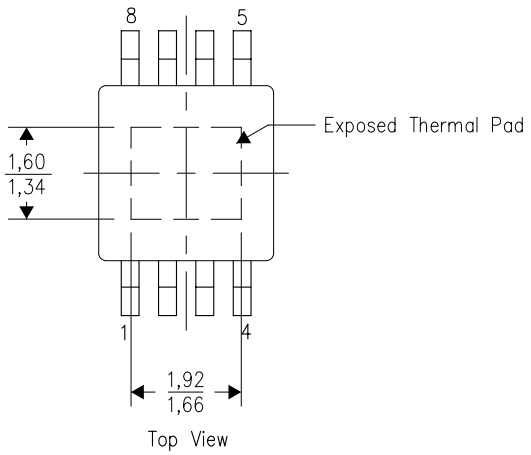
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Exposed Thermal Pad Dimensions

4206323–4/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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