FAIRCHILD SEMICONDUCTOR®

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# FSQ0370RNA, FSQ0370RLA
# Green Mode Fairchild Power Switch (FPS™)

## Features

- Internal Avalanche Rugged 700V SenseFET
- Consumes Only 0.8W at 230$V_{AC}$ & 0.5W Load with Burst-Mode Operation
- Precision Fixed Operating Frequency: 100kHz
- Internal Startup Circuit and Built-in Soft-Start
- Pulse-by-Pulse Current Limiting, Auto-Restart Mode
- Over-Voltage Protection (OVP), Overload Protection (OLP), Internal Thermal Shutdown Function (TSD)
- Under-Voltage Lockout (UVLO)
- Low Operating Current: 3mA
- Adjustable Peak Current Limit

## Applications

- Auxiliary Power Supply for PC and Server
- SMPS for VCR, SVR, STB, DVD, and DVCD Player
- Printer, Facsimile, and Scanner
- Adapter for Camcorder

## Description

The FSQ0370 consists of an integrated Current Mode Pulse Width Modulator (PWM) and an avalanche rugged 700V SenseFET. It is specifically designed for high-performance offline Switched Mode Power Supplies (SMPS) with minimal external components. The integrated PWM controller features include: a fixed-frequency generating oscillator, Under-Voltage Lockout (UVLO) protection, Leading-Edge Blanking (LEB), an optimized gate turn-on / turn-off driver, Thermal Shutdown (TSD) protection, and temperature-compensated precision current sources for loop compensation and fault protection circuitry.

Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSQ0370 reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform that is well suited for the design of cost-effective flyback converters, such as in PC auxiliary power supplies.

## Related Application Notes

- *AN-4134 — Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)*
- *AN-4137 — Design Guidelines for Offline Flyback Converters Using Fairchild Power Switch (FPS™)*
- *AN-4141 — Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*
- *AN-4147 — Design Guidelines for RCD Snubber of Flyback Converters*

## Ordering Information

| Part Number | Package | Marking Code | $BV_{DSS}$ | $f_{OSC}$ | $R_{DS(ON)(MAX)}$ |
|---|---|---|---|---|---|
| FSQ0370RNA | 8-Lead, Dual Inline Package (DIP) | Q0370RA | 700V | 100KHz | 4.75Ω |
| FSQ0370RLA | 8-Lead, LSOP | | | | |

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## Application Circuit

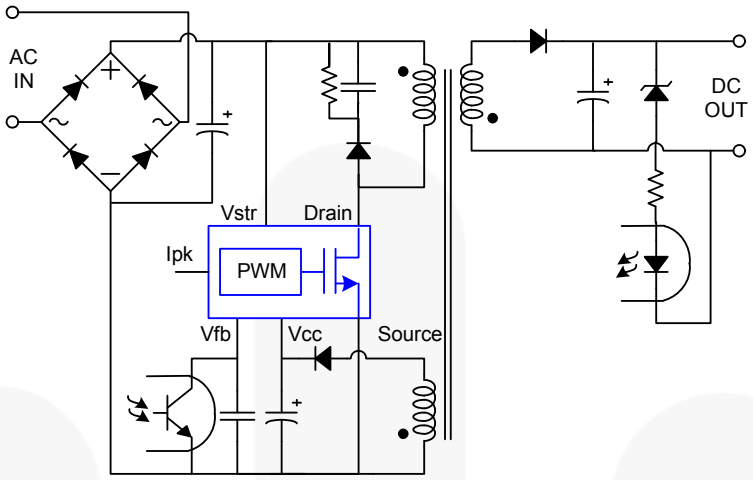



**Figure 1. Typical Flyback Application**

**Table 1. Output Power Table[1]**

| Product | 230V$_{AC}$ ±15%[2] | | 85-265V$_{AC}$ | |
|---|---|---|---|---|
| | Adapter[3] | Open Frame[4] | Adapter[3] | Open Frame[4] |
| FSQ0370RNA | 20W | 27W | 13W | 19W |
| FSQ0370RLA | | | | |

**Notes:**
1. The maximum output power can be limited by junction temperature.
2. 230V$_{AC}$ or 100/115V$_{AC}$ with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50°C ambient.
4. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sink at 50°C ambient.

## Internal Block Diagram

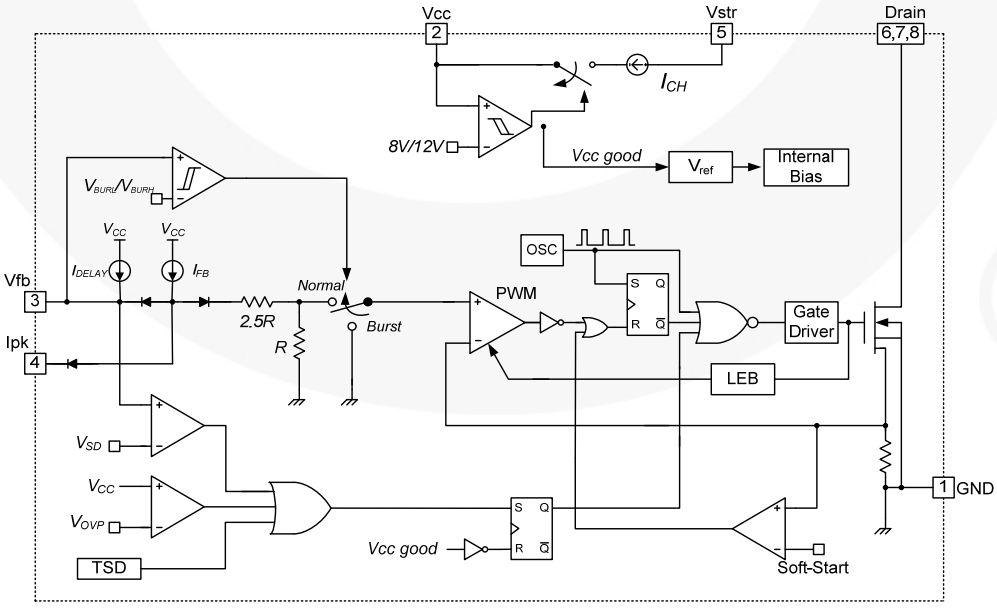



**Figure 2. Functional Block Diagram**

## Pin Assignments

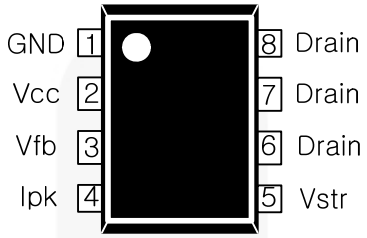



**Figure 3. Pin Configuration (Top View)**

## Pin Definitions

| Pin# | Name | Description |
|---|---|---|
| 1 | GND | SenseFET source terminal on the primary side and internal control ground. |
| 2 | Vcc | Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup *(see Figure 2)*. It is not until $V_{CC}$ reaches the UVLO upper threshold (12V) that the internal startup switch opens and device power is supplied via the auxiliary transformer winding. |
| 3 | Vfb | The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally, while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers overload protection (OLP). There is a delay while charging external capacitor $C_{fb}$ from 3V to 6V using an internal 5μA current source. This delay prevents false triggering under transient conditions, but allows the protection mechanism to operate in true overload conditions. |
| 4 | Ipk | This pin adjusts the peak current limit of the SenseFET. The 0.9mA feedback current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin. This determines the peak current limit. If this pin is tied to Vcc or left floating, the typical peak current limit is 1.1A. |
| 5 | Vstr | This pin is connected to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once $V_{CC}$ reaches 12V, the internal switch is opened. |
| 6, 7, 8 | Drain | The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 700V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance. |

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A$=25°C, unless otherwise specified.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DRAIN}$ | Drain Pin Voltage | 700 | | V |
| $V_{STR}$ | Vstr Pin Voltage | 700 | | V |
| $I_{DM}$ | Drain Current Pulsed[5] | | 12 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy[6] | | 230 | mJ |
| $V_{CC}$ | Supply Voltage | | 20 | V |
| $V_{FB}$ | Feedback Voltage Range | -0.3 | $V_{CC}$ | V |
| $P_D$ | Total Power Dissipation | | 1.5 | W |
| $T_J$ | Recommended Operating Junction Temperature | -40 | Internally Limited | °C |
| $T_A$ | Operating Ambient Temperature | -40 | +85 | °C |
| $T_{STG}$ | Storage Temperature | -55 | +150 | °C |

**Notes:**

5. Non-repetitive rating: pulse-width limited by maximum junction temperature.
6. L=51mH, starting $T_J$=25°C.

## Thermal Impedance

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance[7] | 80 | °C/W |
| $\theta_{JC}$ | Junction-to-Case Thermal Resistance[8] | 20 | |
| $\Psi_{JT}$ | Junction-to-Top Thermal Resistance[9] | 35 | |

**Notes:**

7. Free-standing with no heat-sink, without copper clad.
8. Measured on the drain pin, close to the plastic interface.
9. Measured on the package top surface.

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## Electrical Characteristics

$T_A$=25°C unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SenseFET Section**[10] | | | | | | |
| $I_{DSS}$ | Zero-Gate-Voltage Drain Current | $V_{DS}$=700V, $V_{GS}$=0V | | | 50 | μA |
| | | $V_{DS}$=560V, $V_{GS}$=0V, $T_C$=125°C | | | 200 | |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance[10] | $V_{GS}$=10V, $I_D$=0.5A | | 4.00 | 4.75 | Ω |
| $C_{ISS}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=25V, f=1MHz | | 315 | | pF |
| $C_{OSS}$ | Output Capacitance | $V_{GS}$=0V, $V_{DS}$=25V, f=1MHz | | 47 | | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | $V_{GS}$=0V, $V_{DS}$=25V, f=1MHz | | 9 | | pF |
| $t_{d(on)}$ | Turn-On Delay | $V_{DD}$=350V, $I_D$=1A | | 11.2 | | ns |
| $t_r$ | Rise Time | $V_{DD}$=350V, $I_D$=1A | | 34 | | ns |
| $t_{d(off)}$ | Turn-Off Delay | $V_{DD}$=350V, $I_D$=1A | | 28.2 | | ns |
| $t_f$ | Fall Time | $V_{DD}$=350V, $I_D$=1A | | 32 | | ns |
| **Control Section** | | | | | | |
| $f_{OSC}$ | Switching Frequency | | 92 | 100 | 108 | kHZ |
| $\Delta f_{OSC}$ | Switching Frequency Variation[11] | -25°C < $T_J$ < 85°C | | ±5 | ±10 | % |
| $D_{MAX}$ | Maximum Duty Cycle | Measured at 0.1 x $V_{DS}$ | 55 | 60 | 650 | % |
| $D_{MIN}$ | Minimum Duty Cycle | | 0 | 0 | 0 | % |
| $V_{START}$ | UVLO Threshold Voltage | $V_{FB}$=GND | 11 | 12 | 13 | V |
| $V_{STOP}$ | | | 7 | 8 | 9 | |
| $I_{FB}$ | Feedback Source Current | $V_{FB}$=GND | 0.7 | 0.9 | 1.1 | mA |
| $t_{S/S}$ | Internal Soft-Start Time[11] | $V_{FB}$=4V | | 10 | | ms |
| **Burst-Mode Section** | | | | | | |
| $V_{BURH}$ | Burst-Mode Voltage | $T_J$=25°C | 0.5 | 0.6 | 07 | V |
| $V_{BURL}$ | | | 0.3 | 0.4 | 0.5 | V |
| $V_{BUR(HYS)}$ | | | 100 | 200 | 300 | mV |
| **Protection Section** | | | | | | |
| $I_{LIM}$ | Peak Current Limit | di/dt=240mA/μs | 0.97 | 1.10 | 1.23 | A |
| $t_{CLD}$ | Current Limit Delay[11] | | | 500 | | ns |
| $T_{SD}$ | Thermal Shutdown Temperature[11] | | 125 | 140 | | °C |
| $V_{SD}$ | Shutdown Feedback Voltage | | 5.5 | 6.0 | 6.5 | V |
| $V_{OVP}$ | Over-Voltage Protection | | 18 | 19 | | V |
| $I_{DELAY}$ | Shutdown Delay Current | $V_{FB}$=4V | 3.5 | 5.0 | 6.5 | μA |
| $t_{LEB}$ | Leading-Edge Blanking Time[11] | | 200 | | | ns |
| **Total Device Section** | | | | | | |
| $I_{OP}$ | Operating Supply Current (Control Part Only) | $V_{CC}$=14V | 1 | 3 | 5 | mA |
| $I_{CH}$ | Startup Charging Current | $V_{CC}$=0V | 0.70 | 0.85 | 1.00 | mA |
| $V_{STR}$ | $V_{STR}$ Supply Voltage | $V_{CC}$=0V | | 24 | | V |

**Notes:**

10. Pulse test: Pulse width ≤ 300μs, duty ≤ 2%.
11. These parameters, although guaranteed, are not 100% tested in production.

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## Typical Performance Characteristics

Characteristic graphs are normalized at $T_A$=25°C.

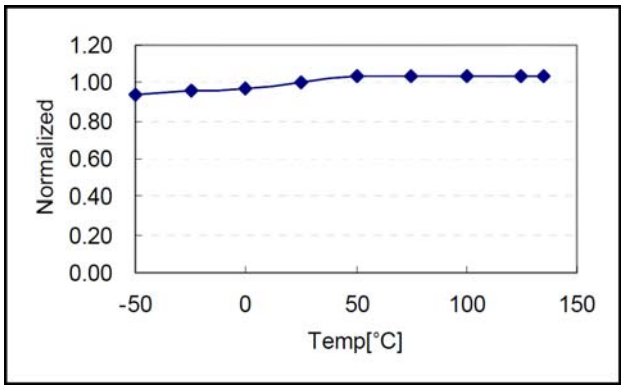



**Figure 4. Operating Frequency ($f_{OSC}$) vs. $T_A$**

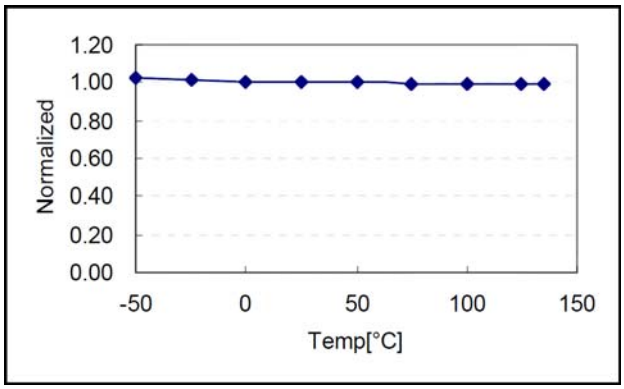



**Figure 5. Over-Voltage Protection ($V_{OVP}$) vs. $T_A$**

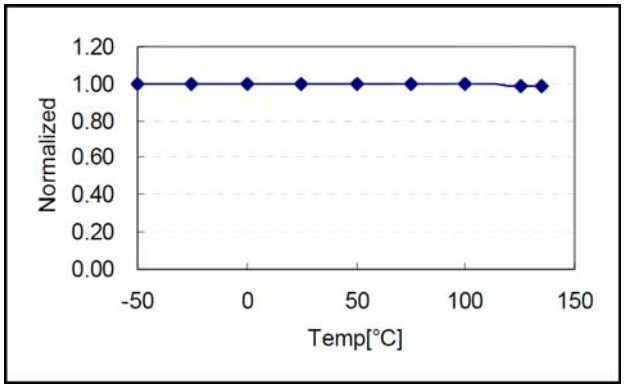



**Figure 6. Maximum Duty Cycle ($D_{MAX}$) vs. $T_A$**

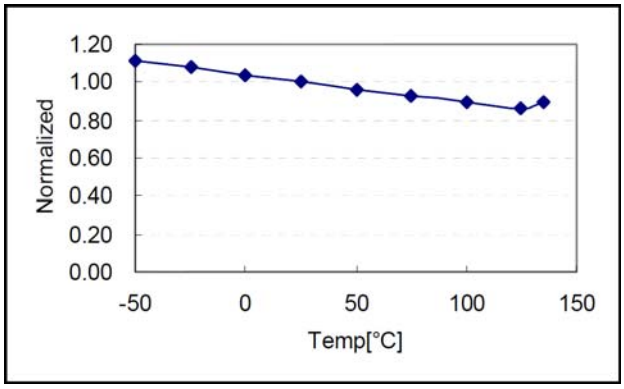



**Figure 7. Operating Supply Current ($I_{OP}$) vs. $T_A$**

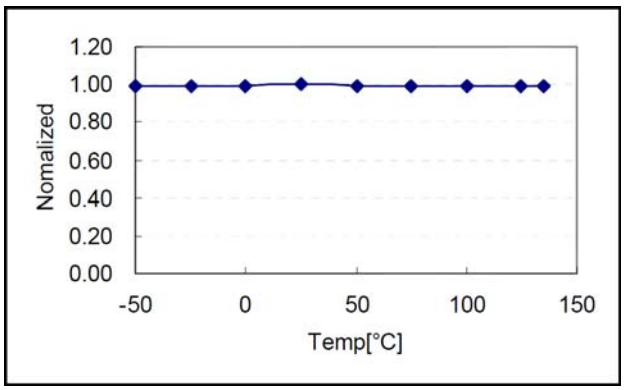



**Figure 8. Start Threshold Voltage ($V_{START}$) vs. $T_A$**

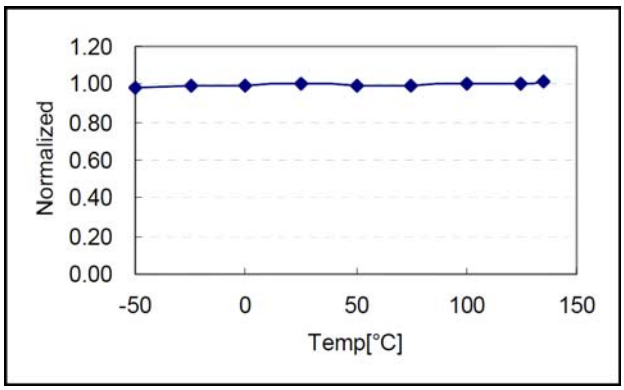



**Figure 9. Stop Threshold Voltage($V_{STOP}$) vs. $T_A$**

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## Typical Performance Characteristics

Characteristic graphs are normalized at $T_A$=25°C.

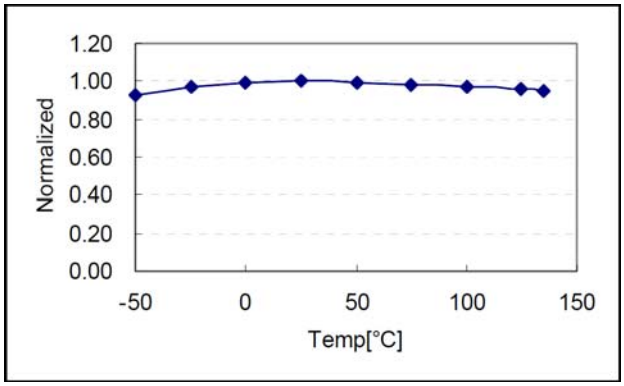



**Figure 10. Feedback Source Current ($I_{FB}$) vs. $T_A$**

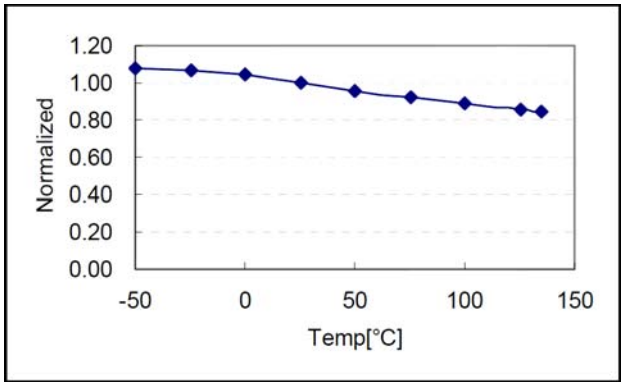



**Figure 11. Startup Charging Current ($I_{CH}$) vs. $T_A$**

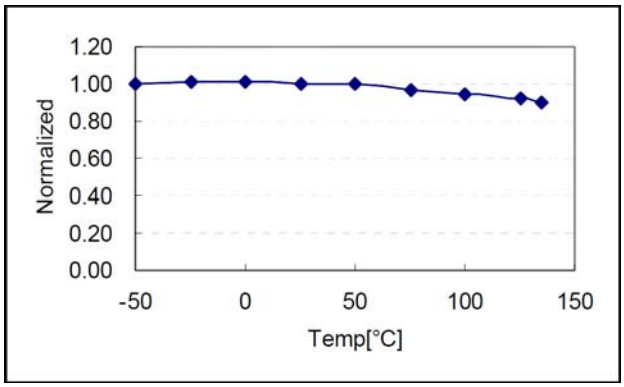



**Figure 12. Peak Current Limit ($I_{LIM}$) vs. $T_A$**

## Functional Description

**1. Startup**: In previous generations of Fairchild Power Switches (FPS™), the Vstr pin required an external resistor to the DC input voltage line. In this generation, the startup resistor is replaced by an internal high-voltage current source and a switch that shuts off 10ms after the $V_{CC}$ supply voltage goes above 12V. The source turns back on if $V_{CC}$ drops below 8V.

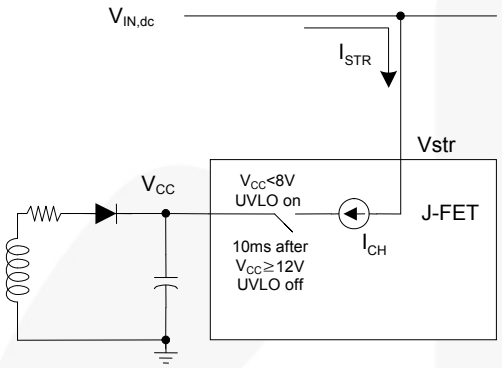



**Figure 13. Startup Circuit**

**2. Feedback Control**: The 700V FPS series employs Current Mode control, as shown in Figure 14. An optocoupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the $R_{sense}$ resistor of SenseFET, plus an offset voltage, makes it possible to control the switching duty cycle. When the regulator reference pin voltage exceeds the internal reference voltage of 2.5V; the optocoupler LED current increases, feedback voltage $V_{fb}$ is pulled down, and the duty cycle is reduced. This typically occurs when the input voltage increases or the output load decreases.

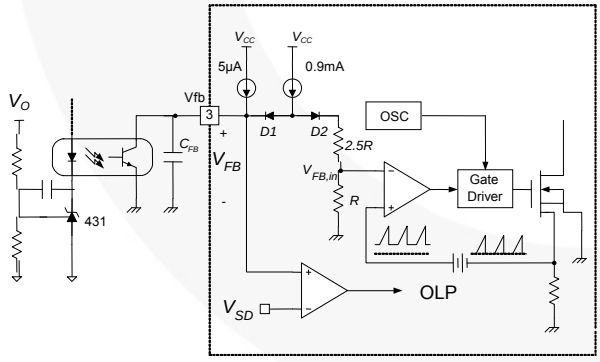
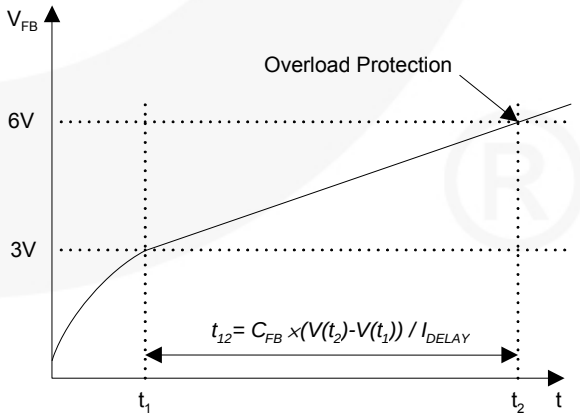



**Figure 14. Pulse Width Modulation (PWM) Circuit**

**3. Leading-Edge Blanking (LEB):** When the internal SenseFET is turned on; the primary-side capacitance and secondary-side rectifier diode reverse recovery typically cause a high current spike through the SenseFET. Excessive voltage across the $R_{sense}$ resistor leads to incorrect feedback operation in the Current Mode PWM control. To counter this effect, the FPS employs a Leading-Edge Blanking (LEB) circuit to inhibit the PWM comparator for a short time ($t_{LEB}$) after the SenseFET is turned on.

**4. Protection Circuits:** The FPS protective functions include Overload Protection (OLP), Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO), and Thermal Shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes $V_{CC}$ to fall. When $V_{CC}$ reaches the UVLO stop voltage, $V_{STOP}$ (typically 8V); the protection is reset and the internal high-voltage current source charges the $V_{CC}$ capacitor via the Vstr pin. When $V_{CC}$ reaches the UVLO start voltage, $V_{START}$ (typically 12V); the FPS resumes normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

**4.1 Overload Protection (OLP):** Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS is operating normally, the Overload Protection (OLP) circuit can be activated during the load transition. To avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or a true overload situation. In conjunction with the Ipk current limit pin (if used), the Current Mode feedback path would limit the current in the SenseFET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage ($V_O$) decreases below its nominal voltage. This reduces the current through the optocoupler LED, which also reduces the optocoupler transistor current, thus increasing the feedback voltage ($V_{FB}$). If $V_{FB}$ exceeds 3V, the feedback input diode is blocked and the 5μA current source ($I_{DELAY}$) starts to slowly charge $C_{fb}$ up to $V_{CC}$. In this condition, $V_{FB}$ increases until it reaches 6V, when the switching operation is terminated (as shown in Figure 15). The shutdown delay s the time required to charge $C_{fb}$ from 3V to 6V with 5μA current source.




$$t_{12} = C_{FB}\frac{V(t_2)-V(t_1)}{I_{DELAY}};\quad I_{DELAY} = 5\mu A, V(t_1) = 3V, V(t_2) = 6V$$

**Figure 15. Overload Protection (OLP)**

**4.2 Thermal Shutdown (TSD):** The SenseFET and the control IC are integrated, making it easier for the control IC to detect the temperature of the SenseFET. If the temperature exceeds approximately 140°C, thermal shutdown is activated.

**4.3 Over-Voltage Protection (OVP):** In the event of a malfunction in the secondary-side feedback circuit or an open feedback loop caused by a soldering defect, the current through the optocoupler transistor becomes almost zero (refer to Figure 14). Then, $V_{FB}$ climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an Over-Voltage Protection (OVP) circuit is employed. In general, $V_{CC}$ is proportional to the output voltage and the FPS uses $V_{CC}$ instead of directly monitoring the output voltage. If $V_{CC}$ exceeds 19V, the OVP circuit is activated, terminating switching. To avoid undesired activation of OVP during normal operation, $V_{CC}$ should be designed to be below 19V.

**5. Soft-Start**: The FPS internal soft-start circuit slowly increases the SenseFET current after startup, as shown in Figure 16. The typical soft-start time is 10ms, where progressive increments of the SenseFET current are allowed during the startup phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This helps to prevent transformer saturation and reduces the stress on the secondary diode during startup.

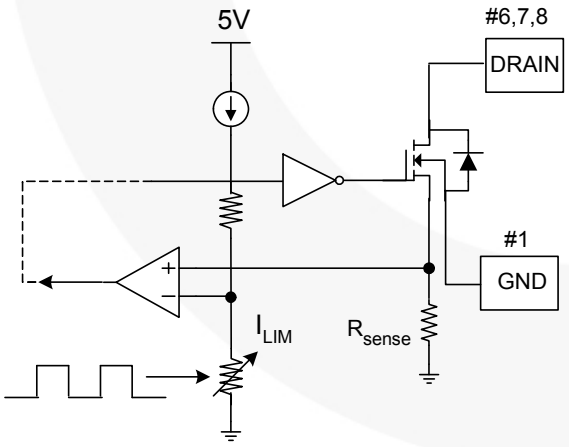



**Figure 16. Soft-Start Function**

**6. Burst Operation:** To minimize power dissipation in Standby Mode, the FPS enters Burst Mode. Feedback voltage decreases as the load decreases and, as shown in Figure 17, the device automatically enters Burst Mode when the feedback voltage drops below $V_{BURH}$ (typically 600mV). Switching continues until the feedback voltage drops below $V_{BURL}$ (typically 400mV). At this point, switching stops and the output voltage starts to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes $V_{BURH}$, switching resumes. The feedback voltage then falls and the process is repeated. Burst Mode alternately enables and disables switching of the SenseFET and reduces switching loss in Standby Mode.

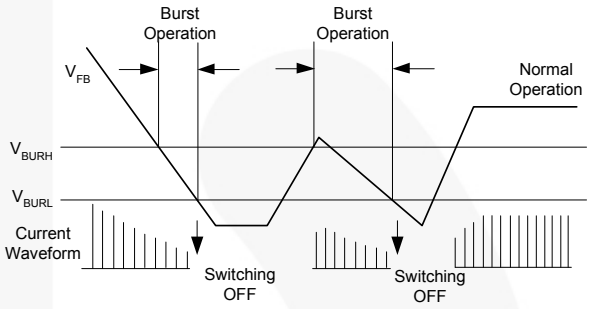



**Figure 17. Burst Operation Function**

**7. Adjusting Peak Current Limit:** As shown in Figure 18, a combined 2.8kΩ internal resistance is connected to the non-inverting lead on the PWM comparator. An external resistance of $R_x$ on the current limit pin forms a parallel resistance with the 2.8kΩ when the internal diodes are biased by the main current source of 900μA.

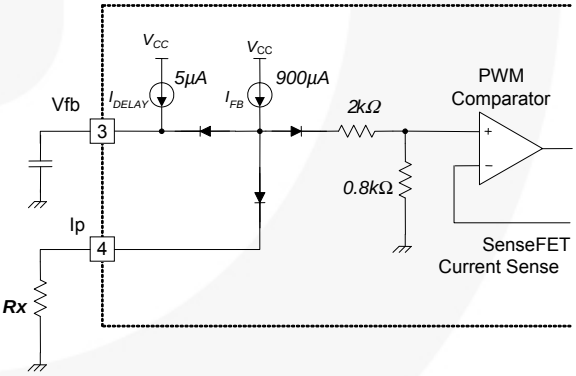



**Figure 18. Peak Current Limit Adjustment**

For example, FSQ0370 has a typical SenseFET peak current limit ($I_{LIM}$) of 1.1A. $I_{LIM}$ can be adjusted to 0.6A by inserting $R_x$ between the Ipk pin and the ground. The value of the $R_x$ can be estimated by:

$$1.1A: 0.6A = 2.8k\Omega: Xk\Omega, \quad (1)$$

$$X = R_x \parallel 2.8k\Omega. \quad (2)$$

where X represents the resistance of the parallel network.

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## Application Information

### Reducing Audible Noise

Switching mode power converters have electronic and magnetic components that generate audible noises when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20KHz, they can crease noise, depending on the load condition. Three methods of reducing noise are discussed below:

**Glue or Varnish**

The most common method of reducing audible noise includes using glue or varnish to tighten magnetic components. The motion of core, bobbin, and coil as well as the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish reduces the transformer noise. Glue or varnish can also crack the core because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio according to the temperature.

**Ceramic Capacitor**

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect, depending on the electric field intensity. A snubber capacitor can become one of the most significant sources of audible noise. Another possibility is to use a Zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

**Adjusting Sound Frequency**

Moving the fundamental frequency of noise out of 2~4KHz range is a third method. Generally, humans are more sensitive to noise in the range of 2~4KHz. When the fundamental frequency of noise is located in this range, the noise sounds louder though the noise intensity level is identical. Refer to Figure 19.

If Burst Mode is suspected as a source of noise, this method may be helpful. If the frequency of Burst Mode operation lies in the range of 2~4KHz, adjusting the feedback loop can shift the burst operation frequency. To reduce burst operation frequency, increase a feedback gain capacitor ($C_F$), optocoupler supply resistor ($R_D$), and feedback capacitor ($C_B$) and decrease a feedback gain resistor ($R_F$) as shown in Figure 20.

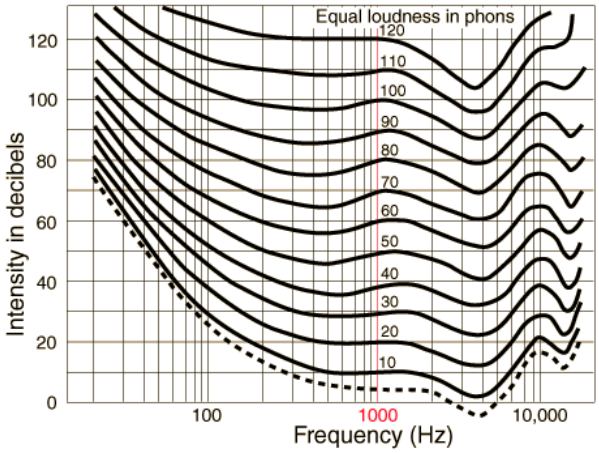



**Figure 19. Equal Loudness Curves**

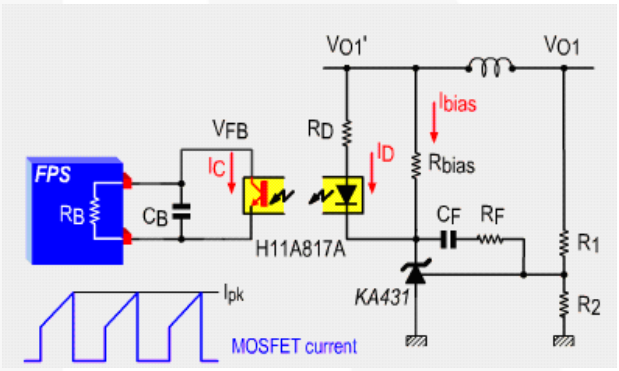



**Figure 20. Typical Feedback Network of FPS™**

### Reference Materials

*AN-4134 — Design Guidelines for Offline Forward Converters Using Fairchild Power Switch (FPS™)*

*AN-4137 — Design Guidelines for Offline Flyback Converters Using Fairchild Power Switch (FPS™)*

*AN-4140 — Transformer Design Consideration for Offline Flyback Converters Using Fairchild Power Switch (FPS™)*

*AN-4141 — Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*

*AN-4147 — Design Guidelines for RCD Snubber of Flyback Converters*

*AN-4148 — Audible Noise Reduction Techniques for FPS Applications*

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## Typical Application Circuit

| Application | Output Power | Input Voltage | Output Voltage (Maximum Current) |
|---|---|---|---|
| PC Auxiliary Power Supply (Using FSQ0270RNA) | 15W | Universal Input (85-264$V_{AC}$) | 5V (3A) |

### Features

- High efficiency (>78% at 115$V_{AC}$ and 230$V_{AC}$ input)
- Low Standby Mode power consumption (<0.8W at 230$V_{AC}$ input and 0.5W load)
- Enhanced system reliability through various protection functions
- Low EMI through frequency modulation
- Internal soft-start: 10ms
- Line UVLO function can be achieved using external components

### Key Design Notes

- The delay for overload protection is designed to be about 30ms with C8 of 47nF. If faster/slower triggering of OLP is required, C8 can be changed to a smaller or larger value (eg. 100nF for 60ms).
- ZP1, DL1, RL1, RL2, RL3, RL4, RL5, RL7, QL1, QL2, and CL9 build a line Under-Voltage Lockout block (UVLO). The Zener voltage of ZP1 determines the input voltage that turns the FPS on. RL5 and DL1 provide a reference voltage from $V_{CC}$. If the input voltage divided by RL1, RL2, and RL4 is lower than the Zener voltage of DL1; QL1, and QL2 turn on and pull $V_{fb}$ down to ground.
- An evaluation board and corresponding test report can be provided. Contact a Fairchild representative.

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## Schematic

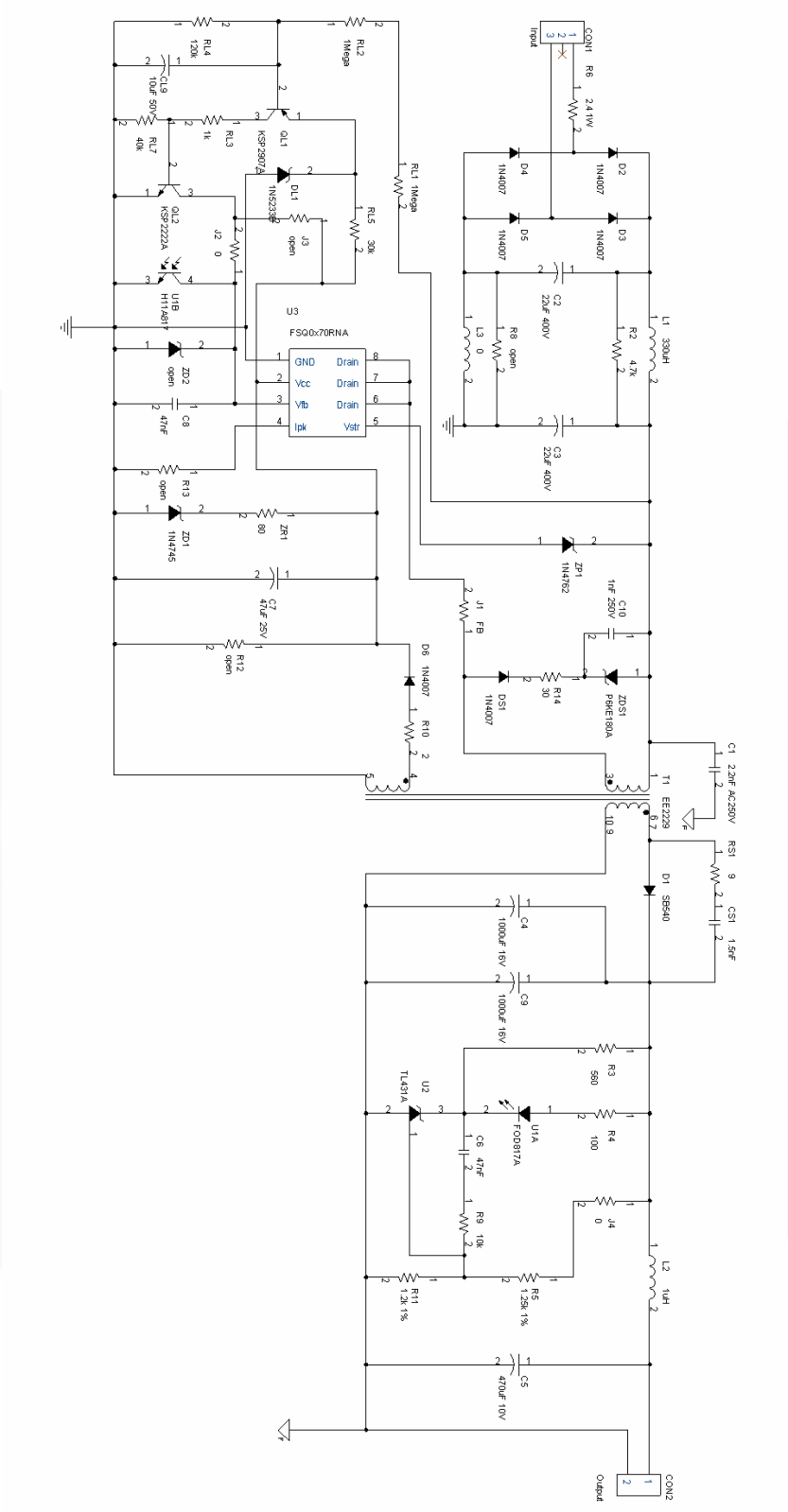



**Figure 21. Demonstration Circuit**

## Transformer

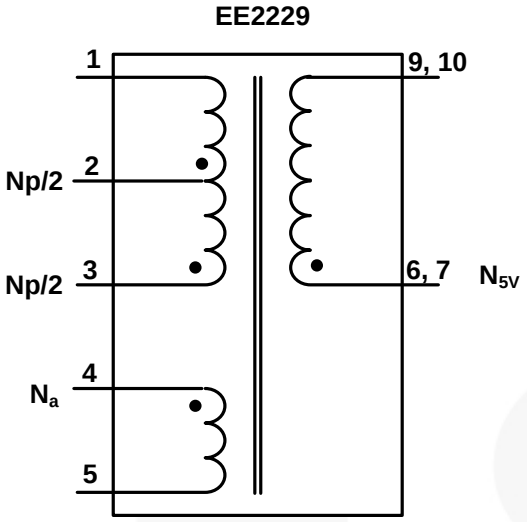



**Figure 22. Transformer Schematic Diagram**

**Table 2. Winding Specification**

| No. | Pin (s→f) | Wire | Turns | Winding Method |
|---|---|---|---|---|
| $N_p/2$ | 3 → 2 | $0.3^{\phi}$ x 1 | 72 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.025mm, 1-Layer | | | | |
| $N_a$ | 4 → 5 | $0.25^{\phi}$ x 2 | 22 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.0250mm, 2-Layer | | | | |
| $N_{5V}$ | 6, 7 → 9, 10 | $0.65^{\phi}$ x 2 | 8 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.025mm, 2-Layer | | | | |
| $N_p/2$ | 2 → 1 | $0.3^{\phi}$ x 1 | 72 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.025mm, 2-Layer | | | | |

**Table 3. Electrical Characteristics**

| | Pin | Specification | Remarks |
|---|---|---|---|
| Inductance | 1 - 3 | 1.20mH ± 5% | 100kHz, 1V |
| Leakage | 1 - 3 | <30μH Maximum | Short All Other Pins |

## Core & Bobbin

- Core: EER2229 ( PL-7, 37.2mm$^2$)
- Bobbin: BE2229

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**Table 4. Demonstration Board Part List**

| Part Number | Value | Quantity | Description (Manufacturer) |
|---|---|---|---|
| C6, C8 | 47nF | 2 | Ceramic Capacitor |
| C1 | 2.2nF (1KV) | 1 | AC Ceramic Capacitor(X1 & Y1) |
| C10 | 1nF (200V) | 1 | Mylar Capacitor |
| CS1 | 1.5nF (50V) | 1 | SMD Ceramic Capacitor |
| C2, C3 | 22μF (400V) | 2 | Low Impedance Electrolytic Capacitor KMX series (Samyoung Electronics) |
| C4, C9 | 1000μF (16V) | 2 | Low ESR Electrolytic Capacitor NXC series (Samyoung Electronics) |
| C5 | 470μF (10V) | 1 | Low ESR Electrolytic Capacitor NXC series (Samyoung Electronics) |
| C7 | 47μF (25V) | 1 | General Electrolytic Capacitor |
| CL9 | 10μF (50V) | 1 | General Electrolytic Capacitor |
| L1 | 330μH | 1 | Inductor |
| L2 | 1μH | 1 | Inductor |
| R6 | 2.4 (1W) | 1 | Fusible Resistor |
| J1, J2, J4, L3 | 0 | 4 | Jumper |
| R2 | 4.7kΩ | 1 | Resistor |
| R3 | 560Ω | 1 | Resistor |
| R4 | 100Ω | 1 | Resistor |
| R5 | 1.25kΩ | 1 | Resistor |
| R11 | 1.2kΩ | 1 | Resistor |
| R9 | 10kΩ | 1 | Resistor |
| R10 | 2Ω | 1 | Resistor |
| R14 | 30Ω | 1 | Resistor |
| RL3 | 1kΩ | 1 | Resistor |
| RL1, RL2 | 1MΩ | 2 | Resistor |
| RL4 | 120kΩ | 1 | Resistor |
| RL5 | 30kΩ | 1 | Resistor |
| RL7 | 40kΩ | 1 | Resistor |
| RS1 | 9Ω | 1 | Resistor |
| ZR1 | 80Ω | 1 | SMD Resistor |
| U1 | FOD817A | 1 | IC (Fairchild Semiconductor) |
| U2 | TL431 | 1 | IC (Fairchild Semiconductor) |
| U3 | FSQ0270RNA | 1 | IC (Fairchild Semiconductor) |
| QL1 | 2N2907 | 1 | IC (Fairchild Semiconductor) |
| QL2 | 2N2222 | 1 | IC (Fairchild Semiconductor) |
| D2, D3, D4, D5, D6, DS1 | 1N4007 | 6 | Diode (Fairchild Semiconductor) |
| D1 | SB540 | 1 | Schottky Diode (Fairchild Semiconductor) |
| ZD1 | 1N4745 | 1 | Zener Diode (Fairchild Semiconductor) |
| DL1 | 1N5233 | 1 | Zener Diode (Fairchild Semiconductor) |
| ZP1 | 82V (1W) | 1 | Zener Diode (Fairchild Semiconductor) |
| ZDS1 | P6KE180A | 1 | TVS (Fairchild Semiconductor) |

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## Layout

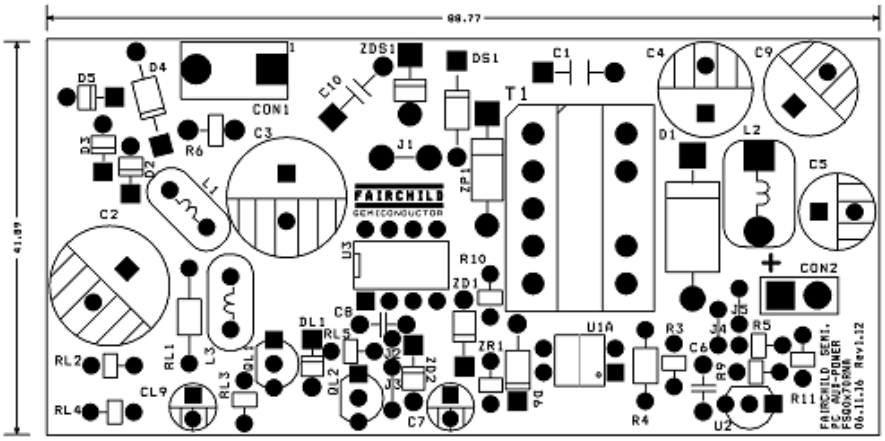



**Figure 23. Top Image of PCB**

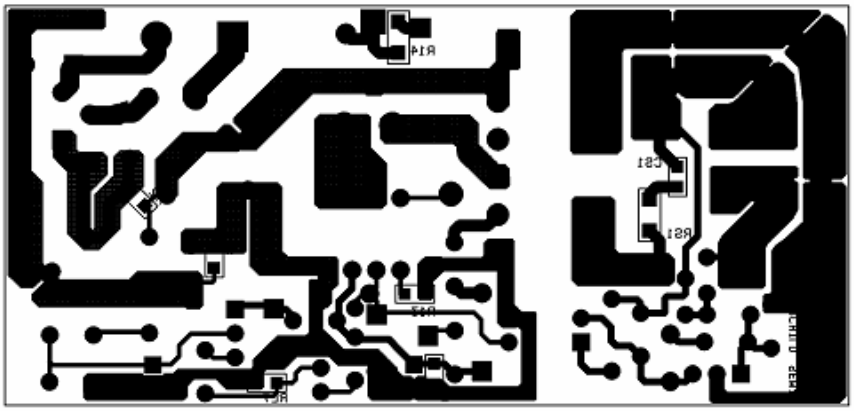
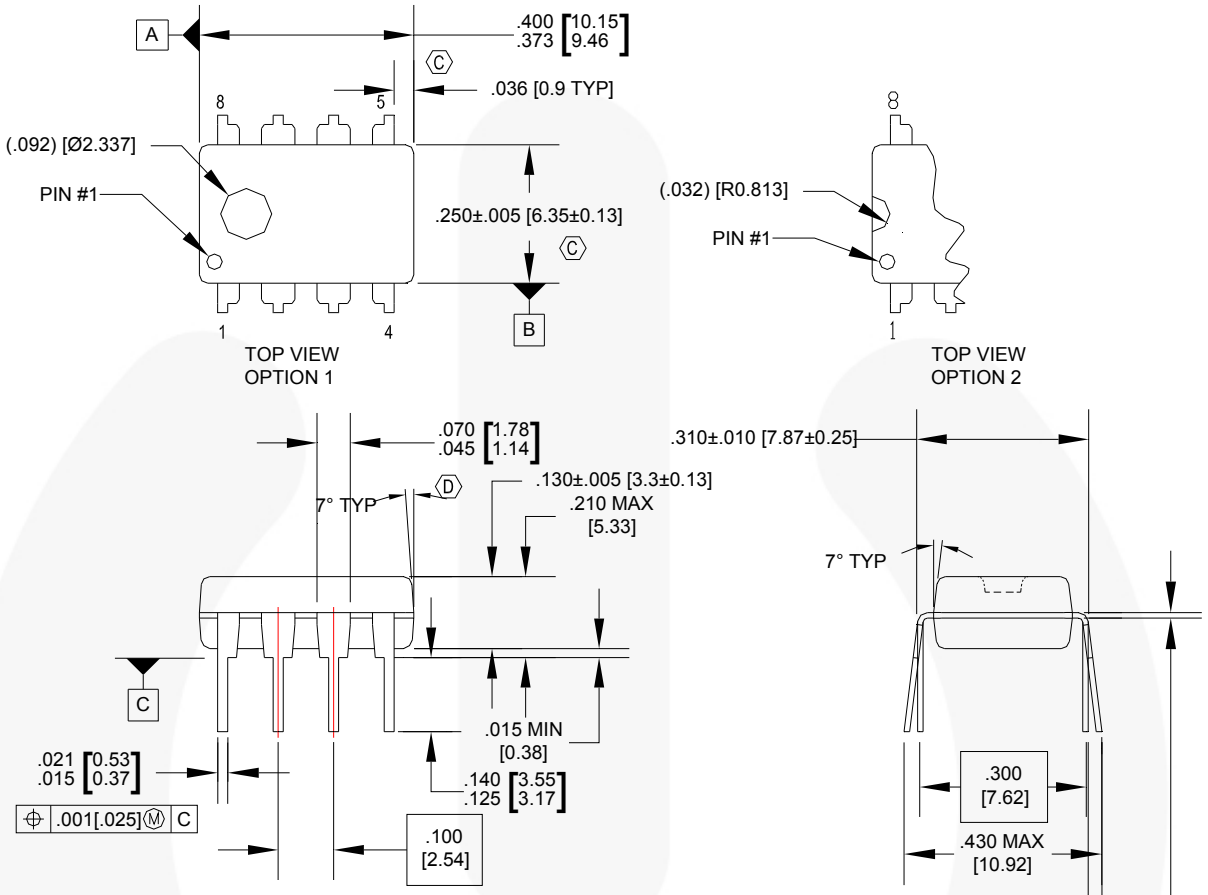


**Figure 24. Bottom of Image of PCB**

## Package Dimensions




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS BA
B. CONTROLING DIMENSIONS ARE IN INCHES REFERENCE DIMENSIONS ARE IN MILLIMETERS
C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

N08EREVG

**Figure 25. 8-Lead, Dual Inline Package (DIP)**

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## Package Dimensions (Continued)

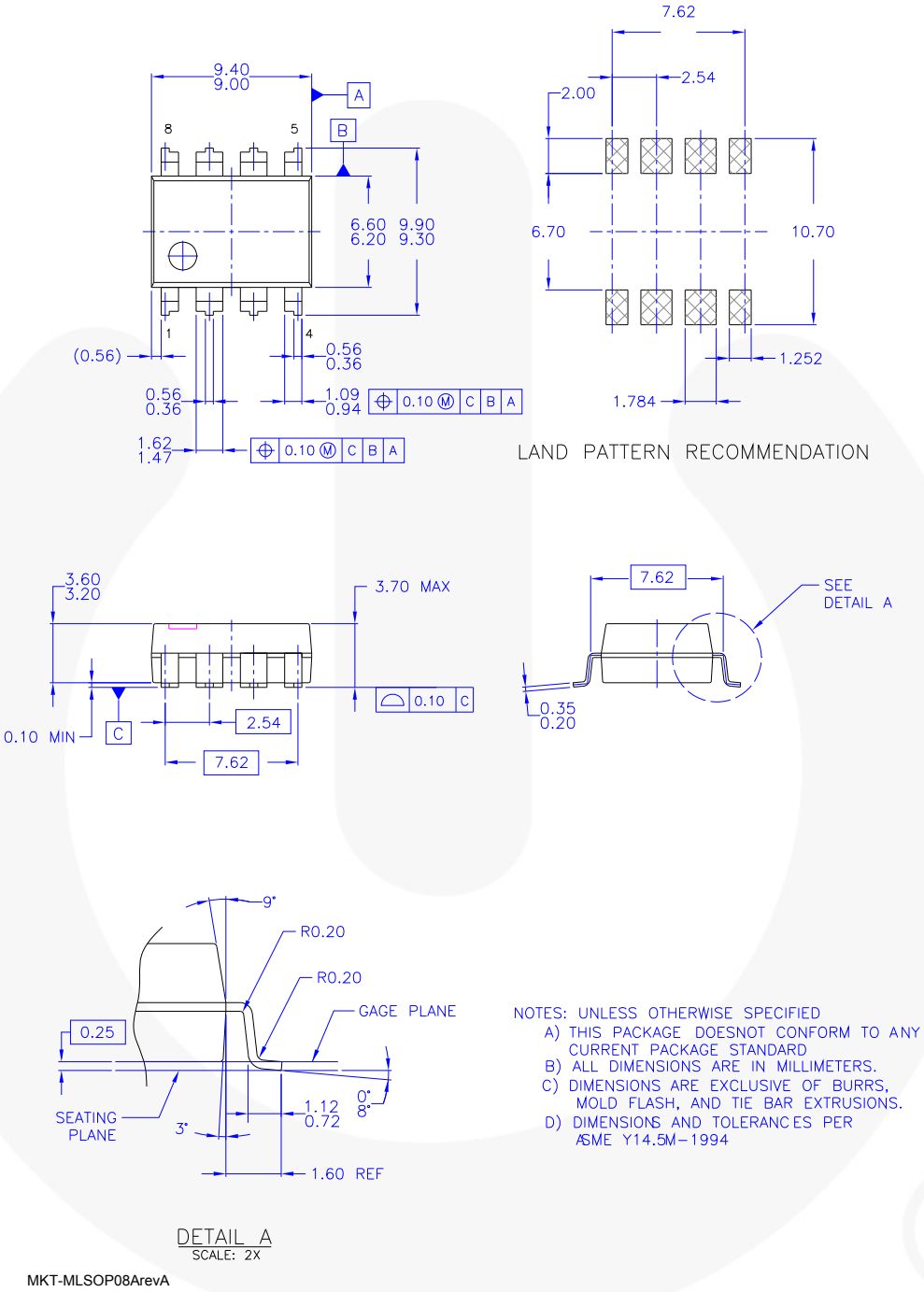



**Figure 26. 8-Lead, MLSOP**

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