PNPN Epitaxial Planar SCR

BCR1002A3

Descriptions

The BCR1002A3 is designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

Features

- Practical level triggering and holding characteristics
- On state current rating of 0.35A$_{RMS}$
- Sensitive gate allows triggering by microcontrollers and other logic circuits
- Pb-free package

Symbol

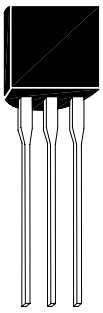
BCR1002A3



G：Gate
A：Anode
K：Cathode

Outline

TO-92



K G A

Ordering Information

Device	Package	Shipping
BCR1002A3-0-TB-G	TO-92 (Pb-free lead plating and halogen-free package)	2000 pcs / tape & box
BCR1002A3-0-BK-G	TO-92 (Pb-free lead plating and halogen-free package)	1000 pcs / bag; 10 bags/box, 10 boxes/carton

Absolute Maximum Ratings (T_J=25°C)

Parameter	Symbol	Limits	Unit
Peak Repetitive Off-State Voltage @T_J=-40℃ to 125℃, R_{GK}=1KΩ	V_{DRM}	140	V
On-State Current @T_C=80℃	$I_{T(RMS)}$	350	mA
Average On-State Current @ T_C=80℃	$I_{T(AV)}$	220	mA
Peak Non-repetitive Surge Current, half cycle, sine wave, 60Hz	I_{TSM}	4	A
Circuit Fusing Consideration (t=8.3ms)	I^2t	0.2	A^2s
Reverse Peak Gate Voltage @T_A=25℃, Pulse Width≤1μs	V_{GRM}	8	V
Forward Peak Gate Current @T_A=25℃, Pulse Width≤1μs	I_{GM}	500	mA
Forward Average Gate Power @ T_A=25℃, t=8.3ms	$P_{G(AV)}$	100	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Junction Temperature	Tj	-40~+125	°C
Storage Temperature	Tstg	-40~+150	°C
Lead Solder Temperature(<1/16" from case, 10secs max)	T_L	260	°C

Note : Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.
V_{DRM} can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however , positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltage shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.

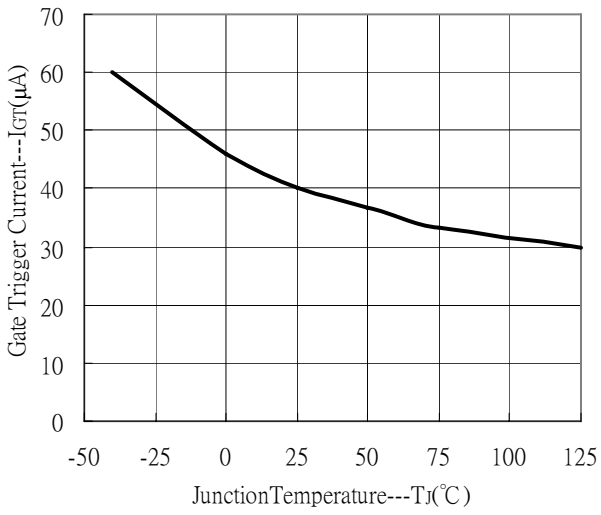
Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
I_{DRM}	-	-	100	μA	V_D=140V, R_{GK}=1KΩ, T_C=125℃
I_{DRM}	-	-	10	μA	V_D=140V, R_{GK}=1KΩ, T_C=25℃
*V_{TM}	-	-	1.5	V	I_{TM}=200mA
I_{GT}	-	-	100	μA	V_D=7V, R_L=100Ω
I_H	-	-	5	mA	V_D=7V, R_{GK}=1KΩ
I_L	-	-	6	mA	V_D=7V, I_G=200μA
V_{GT}	-	-	0.8	V	V_D=7V, R_L=100Ω
dV/dt	25	-	-	V/μs	V_D=35V, R_{GK}=1KΩ
dI/dt	30	-	-	A/μs	I_G=10mA, dI_G/dt=100mA/μs, P_W=10μs

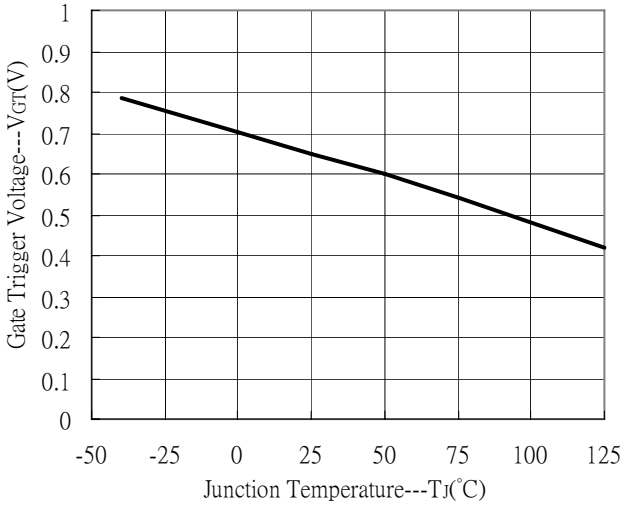
*Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

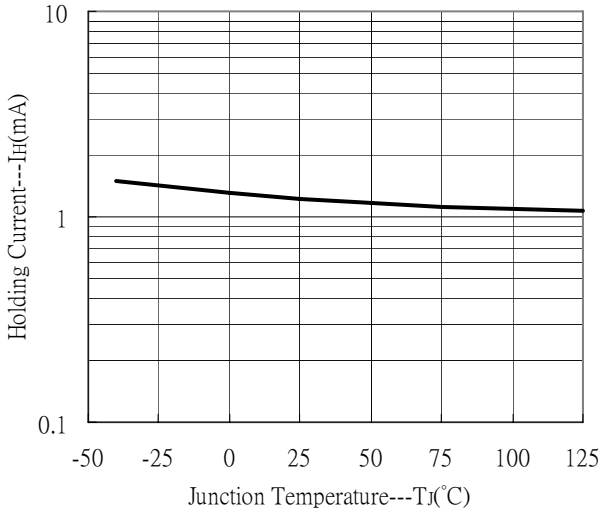
Gate Trigger Current vs Junction Temperature



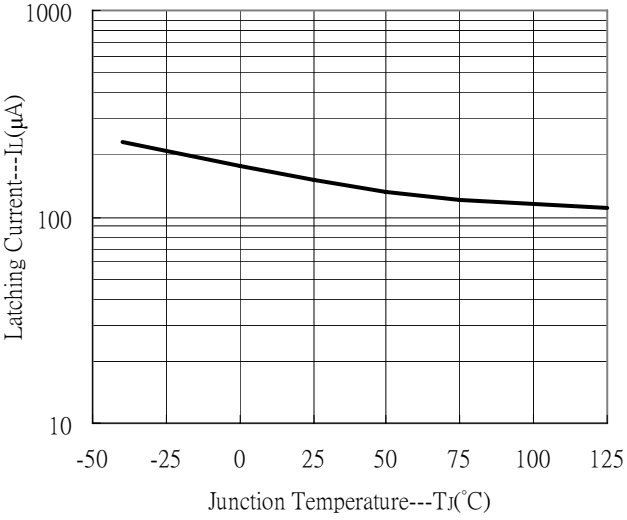
Gate Trigger Voltage vs Junction Temperature



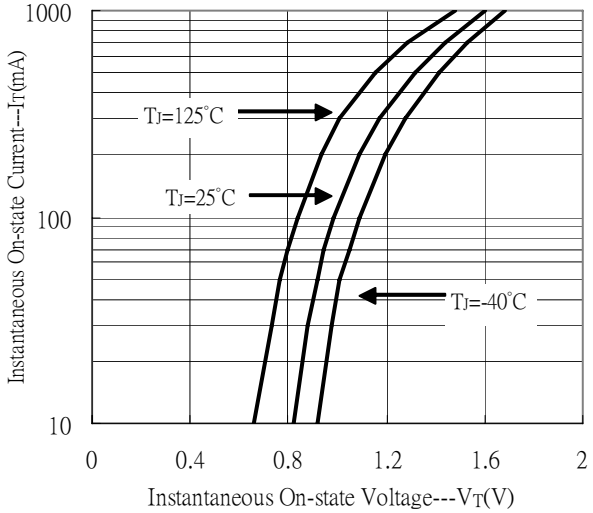
Holding Current vs Junction Temperature



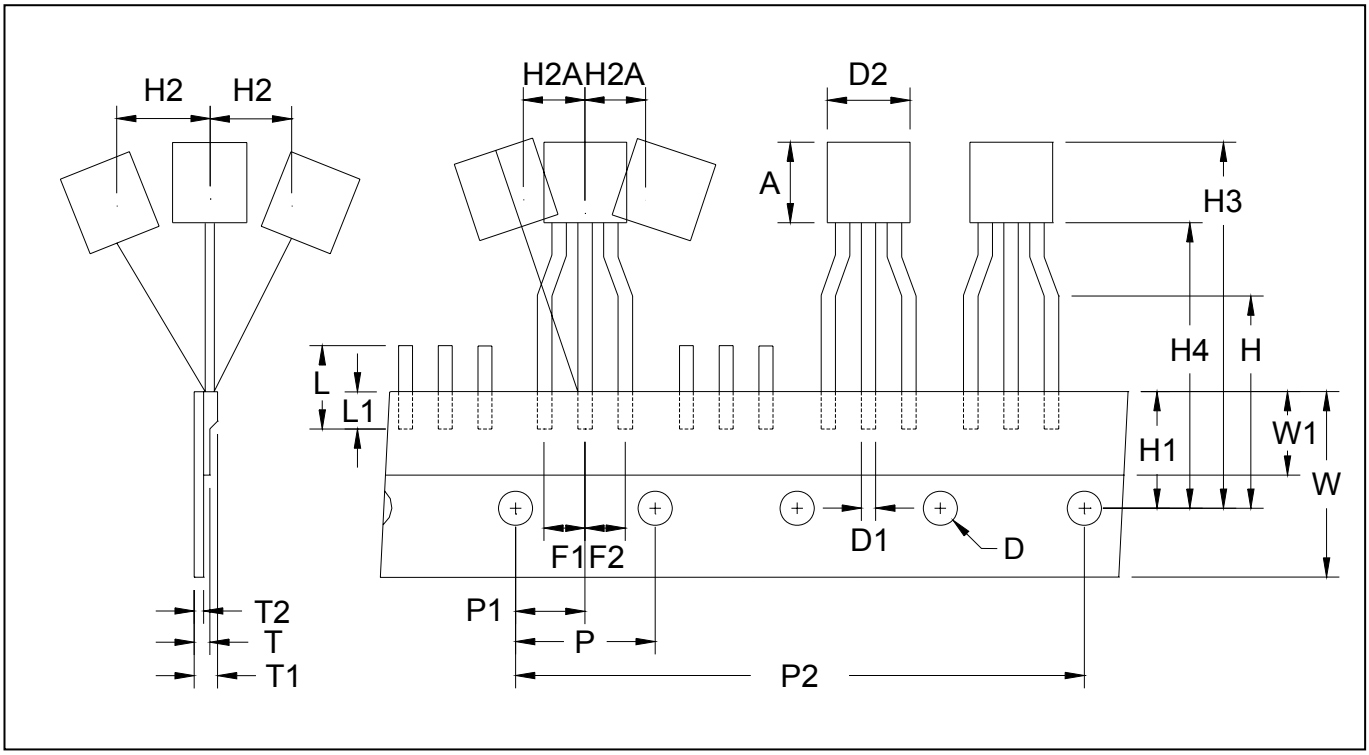
Latching Current vs Junction Temperature



On-state Characteristics



TO-92 Taping Outline

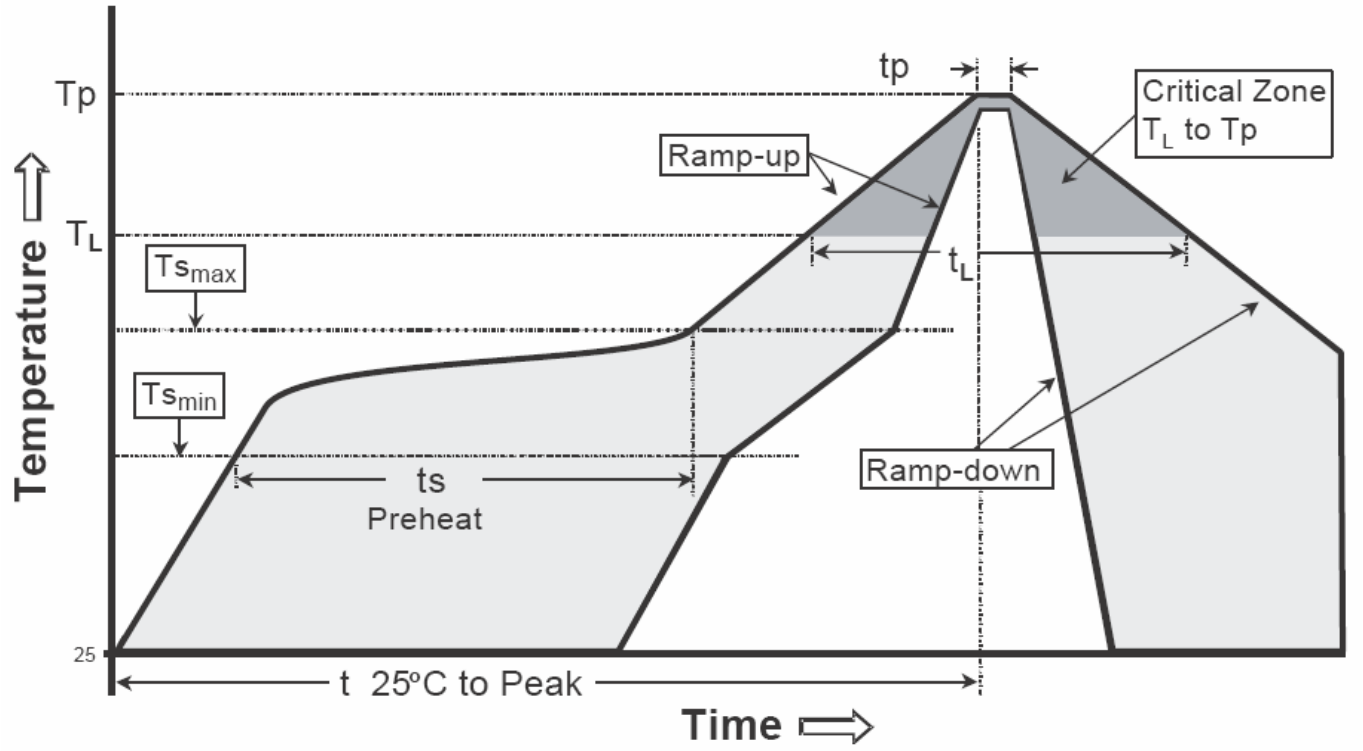


DIM	Item	Millimeters	
		Min.	Max.
A	Component body height	4.33	4.83
D	Tape Feed Diameter	3.80	4.20
D1	Lead Diameter	0.36	0.53
D2	Component Body Diameter	4.33	4.83
F1,F2	Component Lead Pitch	2.40	2.90
F1,F2	F1-F2	-	±0.3
H	Height Of Seating Plane	15.50	16.50
H1	Feed Hole Location	8.50	9.50
H2	Front To Rear Deflection	-	1
H2A	Deflection Left Or Right	-	1
H3	Component Height	-	27
H4	Feed Hole To Bottom Of Component	-	21
L	Lead Length After Component Removal	-	11
L1	Lead Wire Enclosure	2.50	-
P	Feed Hole Pitch	12.50	12.90
P1	Center Of Seating Plane Location	5.95	6.75
P2	4 Feed Hole Pitch	50.30	51.30
T	Over All Tape Thickness	-	0.55
T1	Total Taped Package Thickness	-	1.42
T2	Carrier Tape Thickness	0.36	0.68
W	Tape Width	17.50	19.00
W1	Adhesive Tape Width	5.00	7.00
-	20 pcs Pitch	253	255

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

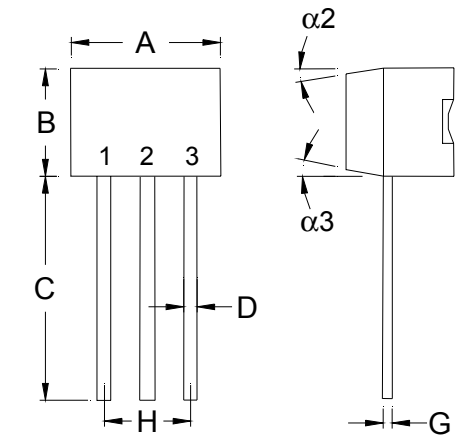
Recommended temperature profile for IR reflow

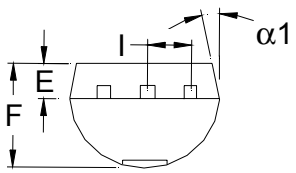


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-92 Dimension





Marking:

Product Name

R1002
□□

Date Code: Year+Month

Year: 4→2004, 5→2005

Month: 1→1, 2→2, • • • ,

9→9, A→10, B→11, C→12

Style: Pin 1.Cathode 2.Gate 3.Anode

3-Lead TO-92 Plastic Package
CYStek Package Code: A3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	α1	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	α2	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	α3	-	*2°	-	*2°

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek ***semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.***
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.