# ULTRA LOW OUTPUT VOLTAGE LINEAR N-FET CONTROLLER

## FEATURES

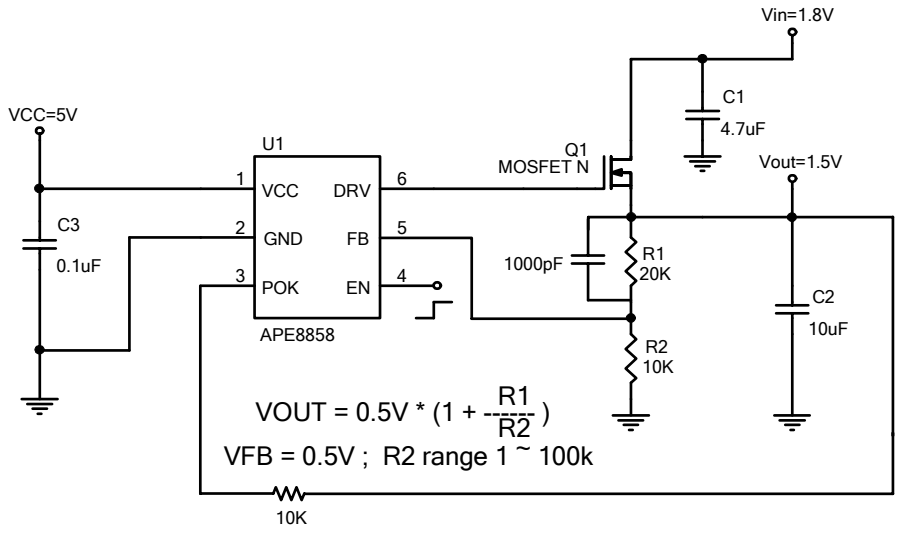
- **Low ESR Output Capacitor (MLCC and POSCAP) Applicable**
- **0.5V Reference Voltage with 2% Accuracy**
- **Internal Soft-Start**
- **Enable Control**
- **Under-Voltage Short Circuit Protection**
- **Fast Transient Response**
- **Power OK Output with a Delay Time**
- **Adjustable Output Voltage Down to 0.5V**
- **Drive N-Channel MOSFETs**
- **Halogen Free & RoHS Compliant**

## DESCRIPTION

The APE8858 is an ultra low output voltage linear N-FET controller. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The APE8858 integrates many functions. A Power-On-Reset (POR) circuit monitors supply voltages to prevent wrong operations. A POK indicates the output status with time delay which is set internally. It can control other converter for power sequence. The APE8858 can be enabled by other power system.

A 0.5V reference voltage with 2% accuracy provide tight regulation of the output voltage, enable control, open drain power good signal, under-voltage protection and soft start.

## TYPICAL APPLICATION




## ORDERING INFORMATIO

**APE8858□-HF**

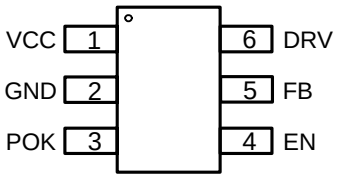
- **Package**
  - **Y : SOT-26**
- Halogen Free

## ABSOLUTE MAXIMUM RATINGS (at $T_A$=25°C)

| | |
|---|---|
| VCC …… | -0.3V to 7V |
| DRV to GND …… | -0.3V to VCC+0.3V |
| Power Dissipation (SOT-26) …… | 0.4W |
| Storage Temperature Range …… | -65 to 150°C |
| Operating Temperature Range …… | -40 to 85°C |
| Junction Temperature Range …… | -40 to 125°C |

## PACKAGE INFORMATION

(Top View)




SOT-26

**Rthja=250°C/W**

## ELECTRICAL SPECIFICATIONS

($V_{IN}$=1.5V, $V_{SHDN}$=$V_{IN}$, $T_A$=25°C, $C_{IN}$=$C_{OUT}$=1µF, unless otherwise noted.)

| Parameter | SYM | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | | 4.5 | - | 5.5 | V |
| Input Voltage UVLO Threshold | $V_{UVLO}$ | $V_{CC}$ rising | - | 3.75 | - | V |
| Input Voltage UVLO Hysteresis | $V_{HYST}$ | $V_{CC}$ falling | - | 0.25 | - | V |
| Supply Current | $I_{CC}$ | EN= $V_{CC}$ | - | 0.4 | 0.8 | mA |
| Shutdown Current | $I_{SD}$ | EN= 0V | -1 | - | 1 | uA |
| Feedback Voltage | $V_{FB}$ | | 0.49 | 0.5 | 0.51 | V |
| Feedback Pin Input Current | $I_{FB}$ | VFB =0.5V | -100 | - | 100 | nA |
| Soft Start Time | TSS | | - | 1 | - | ms |
| EN Pin Logic High threshold voltage | VENH | Enable | 1.3 | - | - | V |
| | $V_{ENL}$ | Disable | - | - | 0.5 | |
| EN Pin Input Current | $I_{EN}$ | $I_{OUT}$=0mA, $V_{IN}$=5V | -1 | - | +1 | uA |
| Output Voltage UVLO Threshold | $V_{TH(UV)}$ | $V_{FB}$ Falling | 0.2 | 0.25 | 0.3 | V |
| Ton Duty | $T_{ON}$ | $V_{FB}$ < 0.25V | - | 30 | - | % |
| DRV Output Current | $I_{DRV(SRC)}$ | Sourcing,$V_{FB}$=0.48V | - | 20 | - | mA |
| | $I_{DRV(SINK)}$ | Sinking ,$V_{FB}$=0.52V | - | 20 | - | |
| DRV Pin Output Voltage | $V_{DRV}$ | $V_{FB}$=0.48V,$V_{CC}$=5V, no load | 4.9 | - | 5.0 | V |
| POK Threshold Voltage for Power OK | $V_{POK}$ | $V_{FB}$ Rising | 90% | 93% | 96% | VFB |

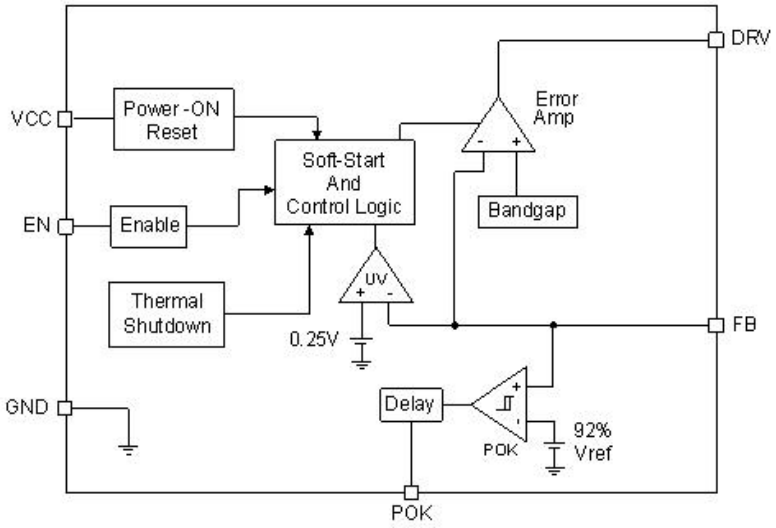
## ELECTRICAL SPECIFICATIONS(Cont.)

| Parameter | SYM | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| POK Threshold Voltage for Power Not OK | $V_{PNOK}$ | $V_{FB}$ Falling | 82% | 85% | 88% | VFB |
| POK Low Voltage | | POK sinks 1mA | - | 50 | 100 | mV |
| POK Delay Time | $T_{DELAY}$ | | 0.8 | 2 | 10 | ms |
| Thermal Shutdown Temperature | TSD | | - | 150 | - | °C |
| Thermal Shutdown Hysteresis | | | - | 50 | - | °C |

## PIN DESCRIPTIONS

| PIN SYMBOL | PIN DESCRIPTION |
|---|---|
| **FB** | Feedback Pin |
| **GND** | Common Ground Pin |
| **DRV** | Gate Drive to N-FET |
| **POK** | Power ok Output Pin |
| **EN** | H : Normal Operation<br>L : Shutdown |
| **VCC** | Input Voltage |

## BLOCK DIAGRAM



# FUNCTION DESCRIPTIONS

### Power-On-Reset

A Power-On-Reset (POR) circuit monitors input voltages at VCC pins to prevent wrong logic controls. The POR function initiates a soft-start process after the supply voltages exceed the rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the VCC voltage falls below it's falling POR threshold.

### Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 1ms.

### Output Voltage Regulation

An error amplifier working with a temperature compensated 0.5V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation.

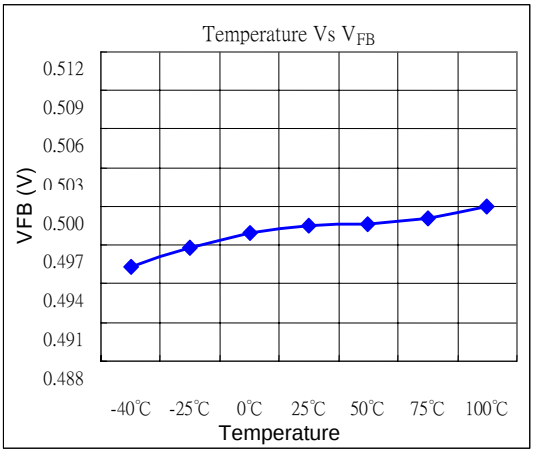
### Under-Voltage Protection (UVP)

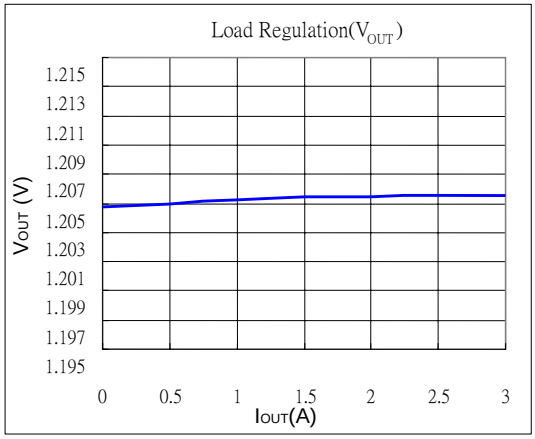
APE8858 monitors the voltage on FB pin after soft-start process is finished. Therefore the UVP is disabling during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while ( ~ 70% Duty ) , APE8858 starts a new soft-start to regulate output.

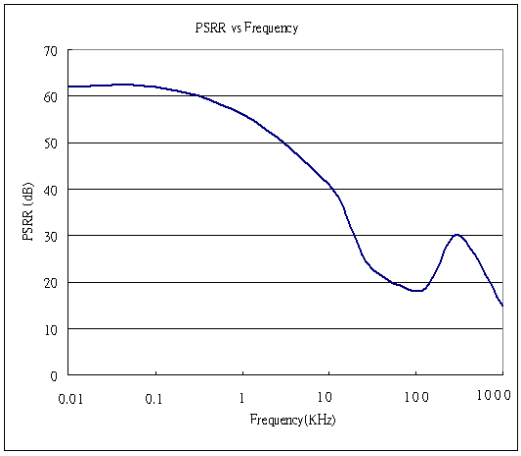
### Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APE8858. When the junction temperature exceeds +150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions.

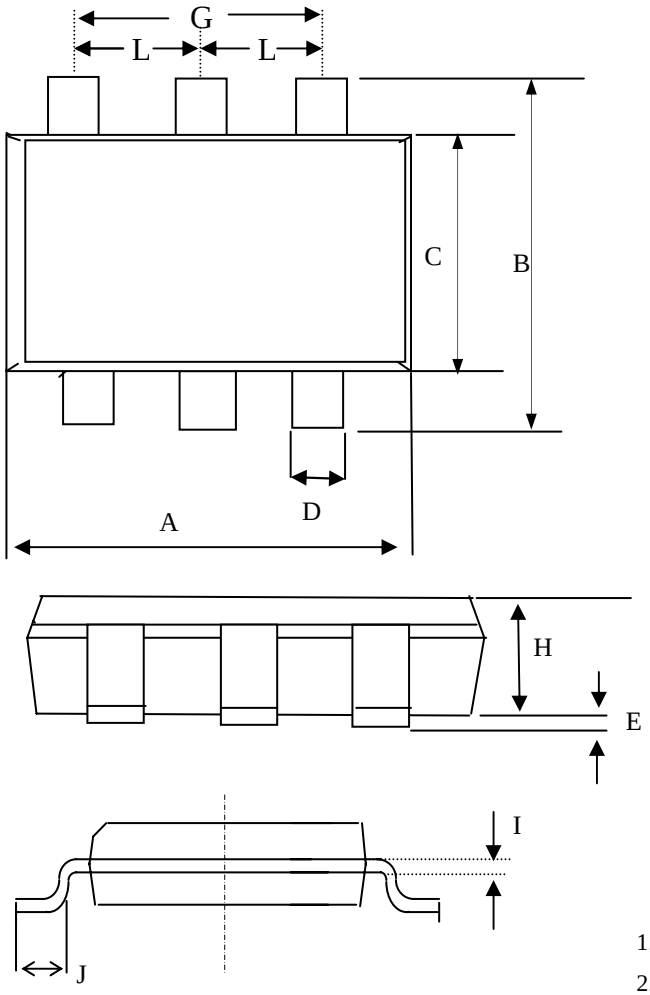
## TYPICAL CHARACTERISTICS



## Package Outline : SOT-26




| | Millimeters | | |
|---|---|---|---|
| SYMBOLS | MIN | NOM | MAX |
| A | 2.70 | 2.90 | 3.10 |
| B | 2.60 | 2.80 | 3.00 |
| C | 1.40 | 1.60 | 1.80 |
| D | 0.30 | 0.43 | 0.55 |
| E | 0.00 | 0.05 | 0.10 |
| H | 1.20REF | | |
| G | 1.90REF | | |
| I | 0.12REF | | |
| J | 0.37REF | | |
| L | 0.95REF | | |

1.All Dimension Are In Millimeters.

2.Dimension Does Not Include Mold Protrusions.

## Part Marking Information & Packing : SOT-26

