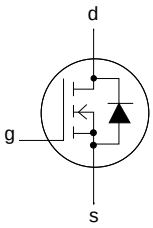
N-channel TrenchMOS™ transistor Logic level FET

BSS123

FEATURES

- **'Trench'** technology
- Extremely fast switching
- Logic level compatible
- Subminiature surface mounting package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 100 V

I_D = 150 mA

$R_{DS(ON)} \leq 6\ \Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

N-channel enhancement mode field-effect transistor in a plastic envelope using '**trench**' technology.

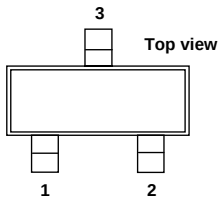
Applications:-
- Relay driver
- High-speed line driver
- Telephone ringer

The BSS123 is supplied in the SOT23 subminiature surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	source
3	drain

SOT23



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 150˚C	-	100	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 150˚C; R_{GS} = 20 kΩ	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	T_a = 25 ˚C	-	150	mA
I_{DM}	Pulsed drain current	T_a = 25 ˚C	-	600	mA
P_D	Total power dissipation	T_a = 25 ˚C	-	0.25	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	surface mounted on FR4 board	500	-	K/W

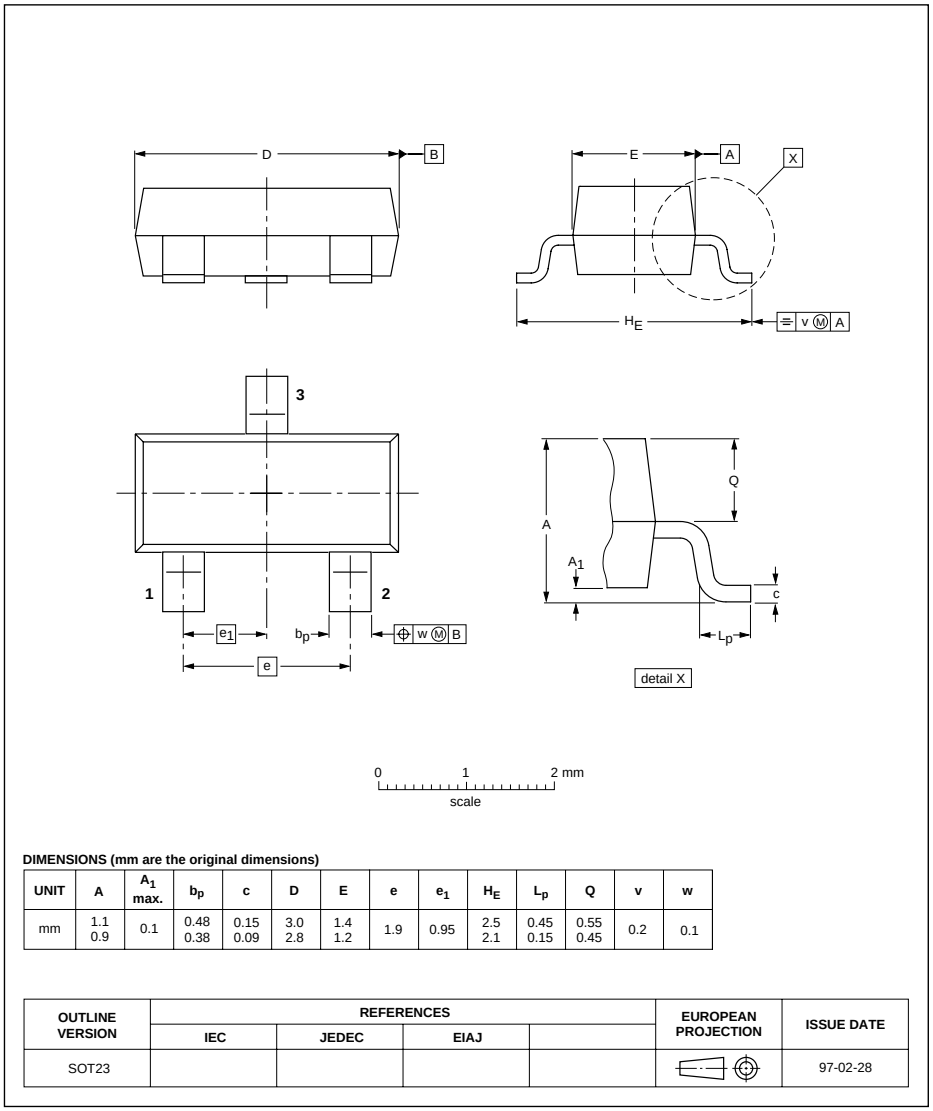
ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 10 μA	100	130	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	2	2.8	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 120 mA	-	3.5	6	Ω
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 120 mA	-	350	-	mS
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V	-	10	100	nA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
t_{on}	Turn-on time	V_{DD} = 50 V; R_D = 250 Ω; V_{GS} = 10 V; R_G = 50 Ω; Resistive load	-	3	10	ns
t_{off}	Turn-off time		-	12	20	ns
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	23	40	pF
C_{oss}	Output capacitance		-	6	25	pF
C_{rss}	Feedback capacitance		-	4	10	pF

MECHANICAL DATA

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

Fig.1. SOT23 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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