# TLV700 200-mA, Low-$I_Q$, Low-Dropout Regulator for Portable Devices

## 1 Features

- Very Low Dropout:
  - 43 mV at $I_{OUT}$ = 50 mA, $V_{OUT}$ = 2.8 V
  - 85 mV at $I_{OUT}$ = 100 mA, $V_{OUT}$ = 2.8 V
  - 175 mV at $I_{OUT}$ = 200 mA, $V_{OUT}$ = 2.35 V
- 2% Accuracy
- Low $I_Q$: 31 µA
- Available in Fixed-Output Voltages from 1.2 V to 4.8 V
- High PSRR: 68 dB at 1 kHz
- Stable With Effective Capacitance of 0.1 µF(1)
- Thermal Shutdown and Overcurrent Protection
- Available in 1.5-mm × 1.5-mm SON-6, SOT23-5, and SC-70 Packages

(1) See the *Input and Output Capacitor Requirements*.

## 2 Applications

- Wireless Handsets
- Smart Phones, PDAs
- ZigBee® Networks
- *Bluetooth*® Devices
- Li-Ion Operated Handheld Products
- WLAN and Other PC Add-on Cards

## 3 Description

The TLV700 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

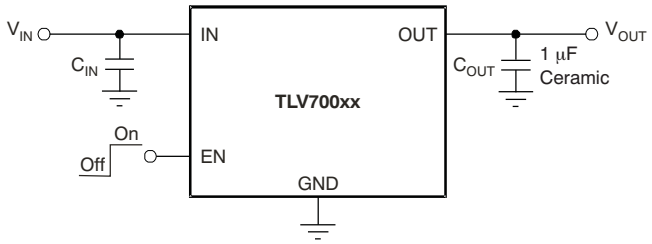
The TLV700 series of LDOs are available in 1.5-mm × 1.5-mm SON-6, SOT-5, and SC70 packages.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TL700xx | SC70 (5) | 2.00 mm × 1.25 mm |
| | SOT (5) | 2.90 mm × 1.60 mm |
| | WSON (6) | 1.50 mm × 1.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application Circuit**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision D (October 2012) to Revision E** — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Applications bullet for *MP3 Players* ... 1
- Changed front-page graphic ... 1
- Changed *Pin Configuration and Functions* section; updated table format ... 4
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement ... 5
- Deleted *Dissipation Ratings* table ... 5
- Changed *Thermal Information* table; updated thermal resistance values for all packages ... 5

**Changes from Revision C (July 2011) to Revision D** — **Page**

- Updated Figure 5 ... 7

**Changes from Revision B (December, 2010) to Revision C** — **Page**

- Added footnote 2 to *Absolute Maximum Ratings* table ... 5
- Changed *output current limit* typical and maximum specifications ... 6
- Deleted previous Figure 12, *Current Limit vs Input Voltage* typical characteristic ... 7

**Changes from Revision A (April, 2010) to Revision B** — **Page**

- Removed TLV701xx device references throughout document ... 1
- Changed minimum output voltage available from 0.7 V to 1.2 V ... 1
- Added footnote (1) ... 1
- Deleted $V_{OUT}$ < *1 V* specification ... 6
- Deleted *Active pulldown resistance* parameter ... 6

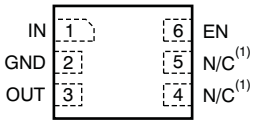

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- Changed Figure 4 title ..... 7
- Changed Figure 5 title ..... 7
- Removed TLV701xx block diagram..... 11
- Revised *Shutdown* section ..... 11
- Updated *Application Information* section to reflect minimum output voltage availability of 1.2 V ..... 13
- Deleted references to TLV701xx throughout *Application Information* ..... 13
- Changed footnote 2 for *Ordering Information* table to reflect minimum output voltage of 1.2 V ..... 17

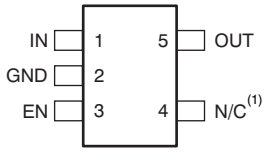
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# 5 Pin Configuration and Functions

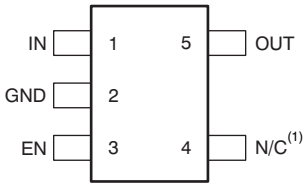
**DSE Package**
**6-Pin WSON**
**Top View**




**DCK Package**
**5-Pin SC70**
**Top View**




**DDC Package**
**5-Pin SOT**
**Top View**




(1) No connection.

**Pin Functions**

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | WSON | SC70 | SOT | | |
| IN | 1 | 1 | 1 | I | Input pin. A small, 1-µF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See *Input and Output Capacitor Requirements* for more details. |
| GND | 2 | 2 | 2 | — | Ground pin |
| EN | 6 | 3 | 3 | I | Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 µA, nominal. |
| NC | 4, 5 | 4 | 4 | — | No connection. This pin can be tied to ground to improve thermal dissipation. |
| OUT | 3 | 5 | 5 | O | Regulated output voltage pin. A small, 1-µF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* for more details. |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$ | –0.3 | 6 | V |
| | $V_{EN}$ | –0.3 | 6 (2) | |
| | $V_{OUT}$ | –0.3 | 6 | |
| Maximum output current $I_{OUT}$ | | Internally limited | | |
| Output short-circuit duration | | Indefinite | | |
| Temperature | Operating junction, $T_J$ | –55 | 150 | °C |
| | Storage, $T_{stg}$ | –55 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $V_{EN}$ absolute maximum rating is $V_{IN}$ + 0.3 V or 6 V, whichever is less.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1) | ±2000 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | 2 | | 5.5 | V |
| $V_{OUT}$ | 1.2 | | 4.8 | V |
| $I_{OUT}$ | 0 | | 200 | mA |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TLV700 | | | UNIT |
|---|---|---|---|---|---|
| | | DCK [SC70] | DDC [SOT] | DSE [WSON] | |
| | | 5 PINS | 5 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 307.6 | 235.9 | 321.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 79.1 | 61.9 | 207.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 93.7 | 54 | 281.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.3 | 0.8 | 42.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 92.8 | 53.4 | 284.8 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | 142.3 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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## 6.5 Electrical Characteristics

At $V_{IN}$ = $V_{OUT(nom)}$ + 0.3 V or 2 V (whichever is greater); $I_{OUT}$ = 10 mA, $V_{EN}$ = 0.9 V, $C_{OUT}$ = 1 µF, and $T_J$ = –40°C to +125°C, unless otherwise noted. Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | | 2 | | 5.5 | V |
| $V_{OUT}$ | DC output accuracy | –40°C ≤ $T_J$ ≤ +125°C | –2% | | 2% | |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation | $V_{OUT(nom)}$ + 0.3 V ≤ $V_{IN}$ ≤ 5.5 V, $I_{OUT}$ = 10 mA | | 1 | 5 | mV |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation | 0 mA ≤ $I_{OUT}$ ≤ 200 mA | | 1 | 15 | mV |
| $V_{DO}$ | Dropout voltage(1) | $V_{IN}$ = 0.98 × $V_{OUT(nom)}$, $I_{OUT}$ = 50 mA, $V_{OUT}$ = 2.8 V | | 43 | | mV |
| | | $V_{IN}$ = 0.98 × $V_{OUT(nom)}$, $I_{OUT}$ = 100 mA, $V_{OUT}$ = 2.8 V | | 85 | | |
| | | $V_{IN}$ = 0.98 × $V_{OUT(nom)}$, $I_{OUT}$ = 200 mA, $V_{OUT}$ = 2.35 V | | 175 | 250 | |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$ | 220 | | 860 | mA |
| $I_{GND}$ | Ground pin current | $I_{OUT}$ = 0 mA | | 31 | 55 | µA |
| | | $I_{OUT}$ = 200 mA, $V_{IN}$ = $V_{OUT}$ + 0.5 V | | 270 | | |
| $I_{SHDN}$ | Ground pin current (shutdown) | $V_{EN}$ ≤ 0.4 V, $V_{IN}$ = 2 V | | 400 | | nA |
| | | $V_{EN}$ ≤ 0.4 V, 2 V ≤ $V_{IN}$ ≤ 4.5 V | | 1 | 2 | µA |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = 2.3 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 10 mA, f = 1 kHz | | 68 | | dB |
| $V_n$ | Output noise voltage | BW = 100 Hz to 100 kHz, $V_{IN}$ = 2.3 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 10 mA | | 48 | | $\mu V_{RMS}$ |
| $t_{STR}$ | Start-up time(2) | $C_{OUT}$ = 1 µF, $I_{OUT}$ = 200 mA | | 100 | | µs |
| $V_{EN(high)}$ | Enable pin high (enabled) | | 0.9 | | $V_{IN}$ | V |
| $V_{EN(low)}$ | Enable pin low (disabled) | | 0 | | 0.4 | V |
| $I_{EN}$ | Enable pin current | $V_{IN}$ = $V_{EN}$ = 5.5 V | | 0.04 | 0.5 | µA |
| UVLO | Undervoltage lockout | $V_{IN}$ rising | | 1.9 | | V |
| $T_{sd}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | 160 | | °C |
| | | Reset, temperature decreasing | | 140 | | |
| $T_J$ | Operating junction temperature | | –40 | | 125 | °C |

(1) $V_{DO}$ is measured for devices with $V_{OUT(nom)}$ ≥ 2.35 V.
(2) Start-up time = time from EN assertion to 0.98 × $V_{OUT(nom)}$.


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## 6.6 Typical Characteristics

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; $I_{OUT}$ = 10 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

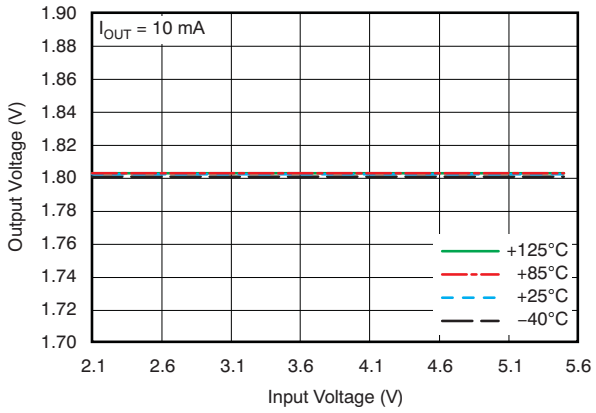



**Figure 1. TLV70018 Line Regulation**

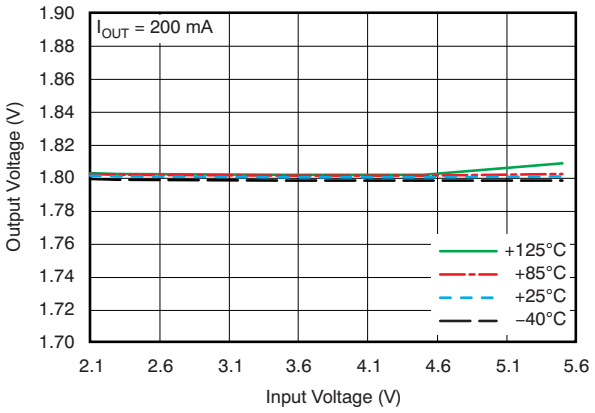



**Figure 2. TLV70018 Line Regulation**

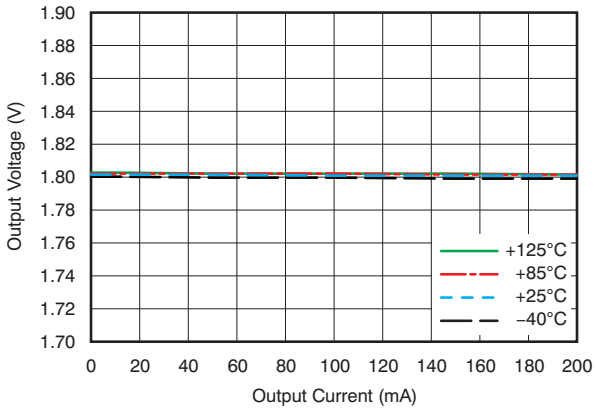



**Figure 3. TLV70018 Load Regulation**

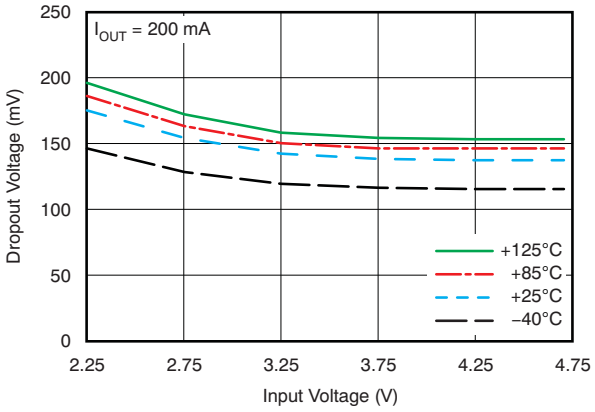



**Figure 4. Dropout Voltage vs Input Voltage**

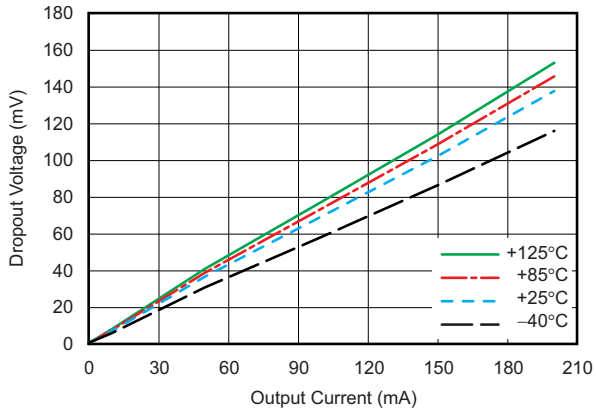



**Figure 5. Dropout Voltage vs Output Current, $V_{OUT}$ = 4.8 V**

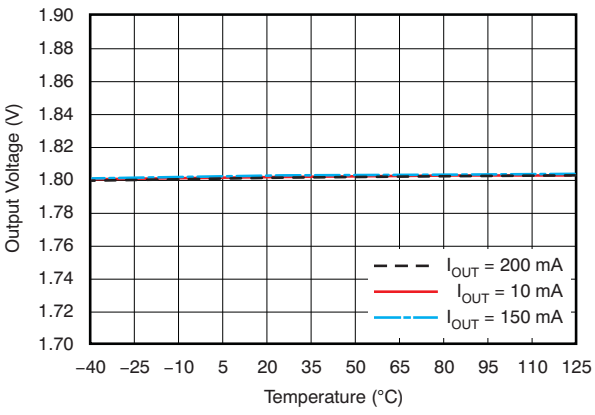



**Figure 6. TLV70018 Output Voltage vs Temperature**

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## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; $I_{OUT}$ = 10 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

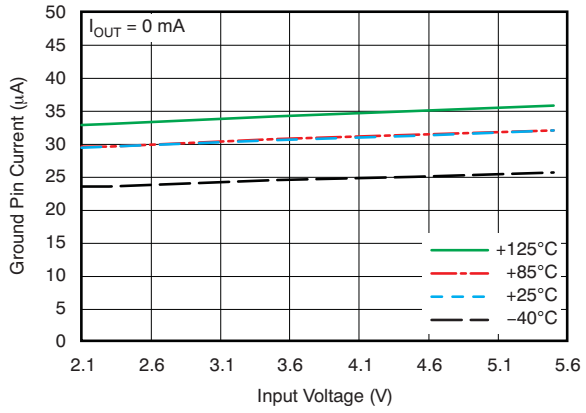



**Figure 7. TLV70018 Ground Pin Current vs Input Voltage**

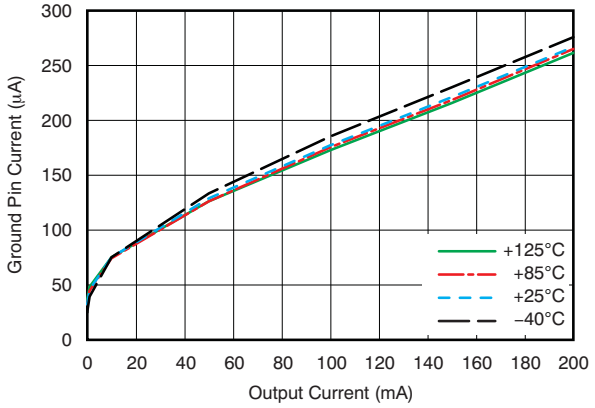



**Figure 8. TLV70018 Ground Pin Current vs Load**

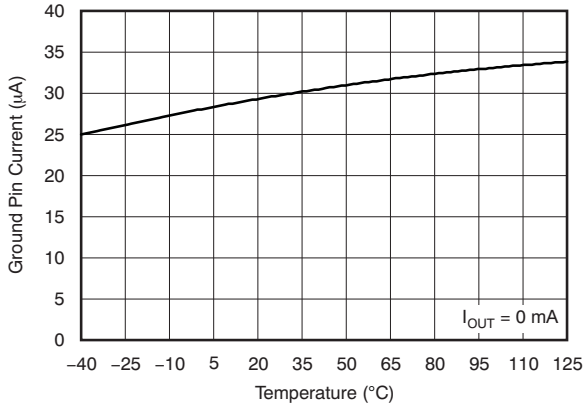



**Figure 9. TLV70018 Ground Pin Current vs Temperature**

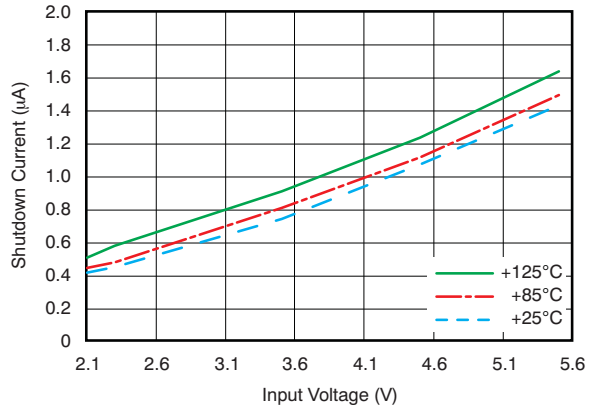



**Figure 10. TLV70018 Shutdown Current vs Input Voltage**

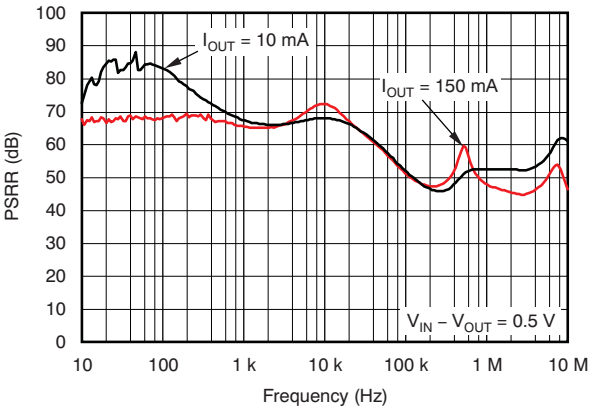



**Figure 11. TLV70018 Power-Supply Ripple Rejection vs Frequency**

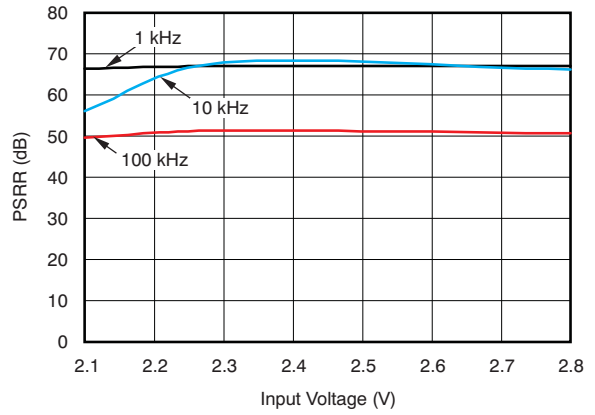



**Figure 12. TLV70018 Power-Supply Ripple Rejection vs Input Voltage**


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## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; $I_{OUT}$ = 10 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

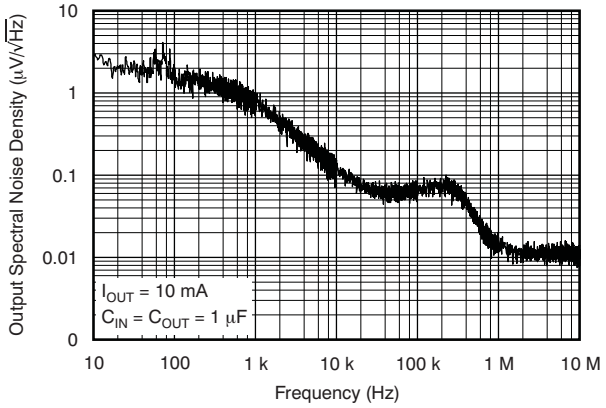



**Figure 13. TLV70018 Output Spectral Noise Density vs Output Voltage**

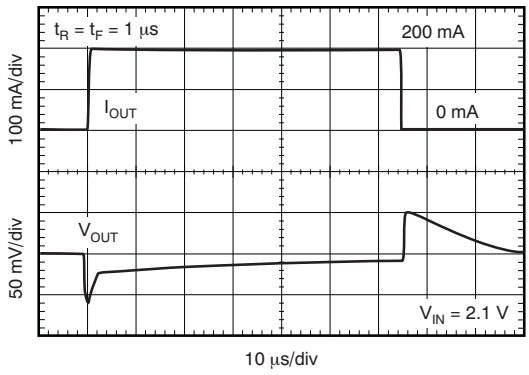



**Figure 14. TLV70018 Load Transient Response**

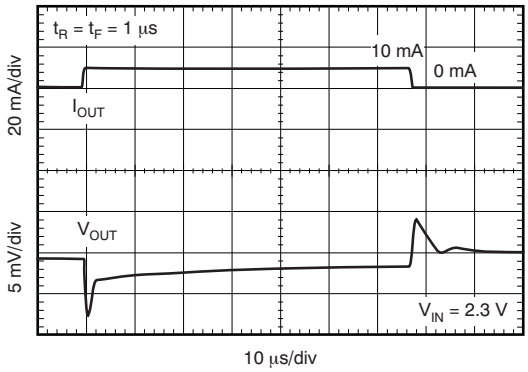



**Figure 15. TLV70018 Load Transient Response**

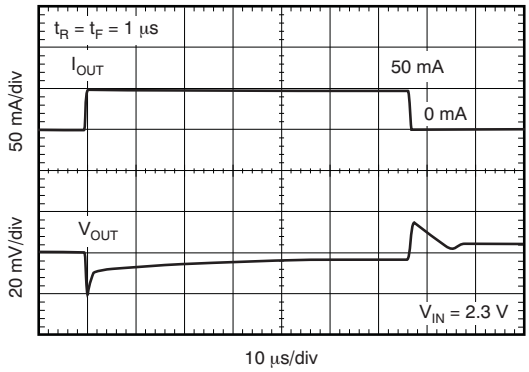



**Figure 16. TLV70018 Load Transient Response**

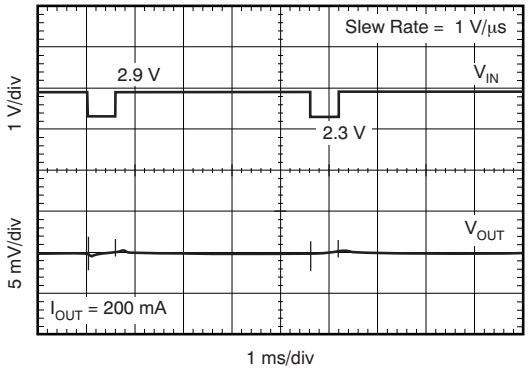



**Figure 17. TLV70018 Line Transient Response**

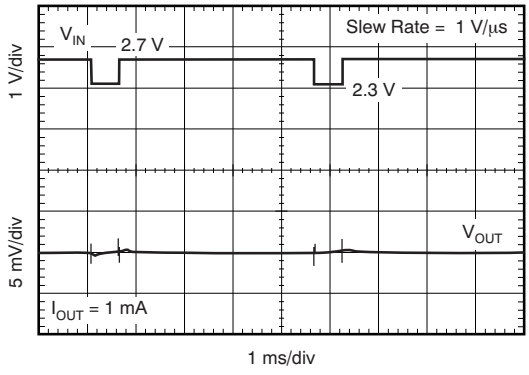



**Figure 18. TLV70018 Line Transient Response**

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## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; $I_{OUT}$ = 10 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

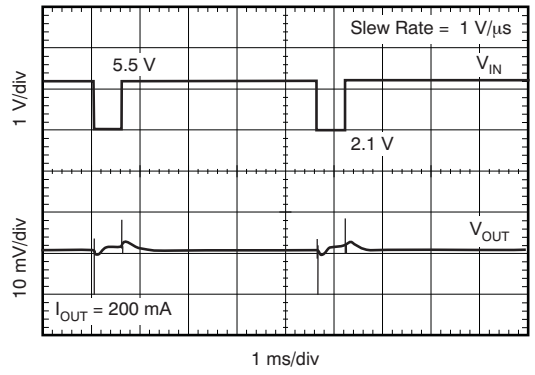



**Figure 19. TLV70018 Line Transient Response**

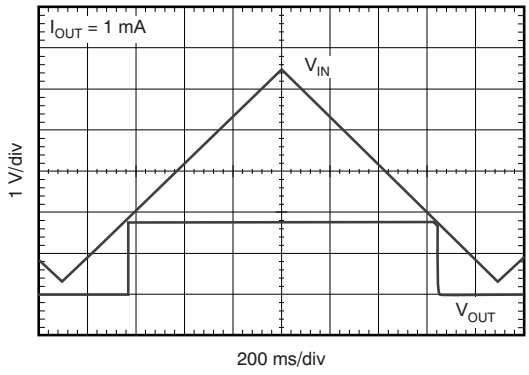



**Figure 20. TLV70018 $V_{IN}$ Ramp-Up, Ramp-Down Response**

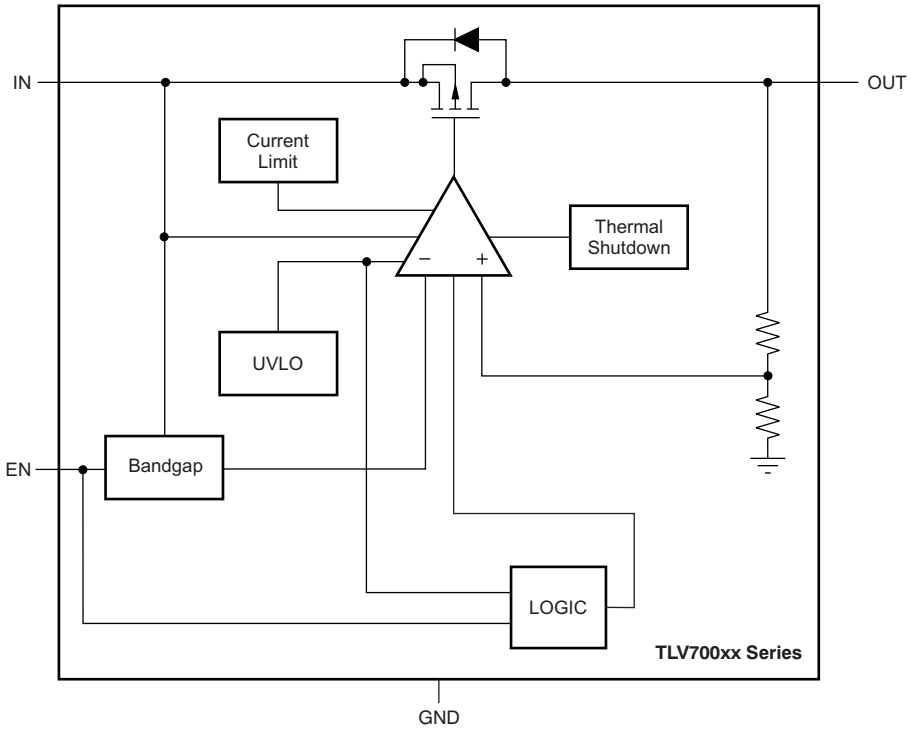

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# 7 Detailed Description

## 7.1 Overview

The TLV700 series of LDO linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high PSRR, and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have integrated thermal shutdown, current limit, and undervoltage lockout (UVLO).

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Internal Current Limit

The TLV700 internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{CL} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{CL}$ until thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See *Thermal Protection* for more details.

The PMOS pass element in the TLV700 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

### 7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at EN pin goes above 0.9 V. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

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## Feature Description (continued)

### 7.3.3 Dropout Voltage

The TLV700 uses a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. $V_{DO}$ scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as ($V_{IN}$ – $V_{OUT}$) approaches dropout. This effect is shown in Figure 12 in *Typical Characteristics*.

### 7.3.4 Undervoltage Lockout (UVLO)

The TLV700 uses a UVLO circuit to keep the output shut off until internal circuitry is operating properly.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The output current is less than the current limit.
- The input voltage is greater than the UVLO voltage.

### 7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer regulates the output voltage of the LDO. Line or load transients in dropout may result in large output voltage deviations.

Table 1 lists the conditions that lead to the different modes of operation.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | |
|---|---|---|
| | $V_{IN}$ | $I_{OUT}$ |
| Normal mode | $V_{IN} > V_{OUT(nom)} + V_{DO}$ | $I_{OUT} < I_{CL}$ |
| Dropout mode | $V_{IN} < V_{OUT(nom)} + V_{DO}$ | $I_{OUT} < I_{CL}$ |
| Current limit | $V_{IN} >$ UVLO | $I_{OUT} > I_{CL}$ |


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TLV700 belongs to a new family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little ($V_{IN}$ – $V_{OUT}$) headroom, make this family of devices ideal for RF portable applications. This family of regulators offers current limit and thermal protection, and is specified from –40°C to +125°C.

## 8.2 Typical Application

Figure 21 shows a typical application circuit.

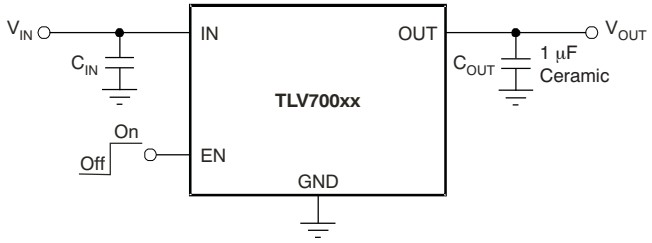



**Figure 21. Typical Application Circuit**

### 8.2.1 Design Requirements

Table 2 lists the design parameters.

**Table 2. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 2.5 V to 3.3 V |
| Output voltage | 1.8 V |
| Output current | 100 mA |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Input and Output Capacitor Requirements*

TI recommends using 1-µF X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV700 is designed to be stable with an *effective capacitance* of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions must not be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

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Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF, low ESR capacitor across the IN pin and GND in of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

#### *8.2.2.2 Transient Response*

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response.

### 8.2.3 Application Curves

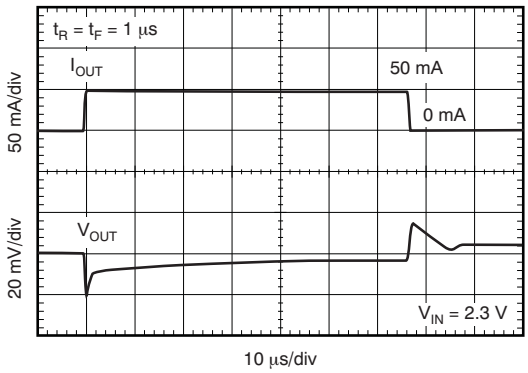



**Figure 22. TLV70018 Load Transient Response**

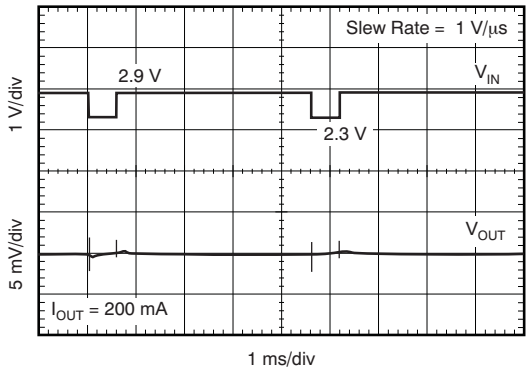



**Figure 23. TLV70018 Line Transient Response**

## 9 Power Supply Recommendations

Connect a low output impedance power supply directly to the INPUT pin of the TLV700. Inductive impedances between the input supply and the INPUT pin can create significant voltage excursions at the INPUT pin during start-up or load transient events.


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# 10 Layout

## 10.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the printed-circuit-boards with separate ground planes for $V_{IN}$ and $V_{OUT}$, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

## 10.2 Layout Examples

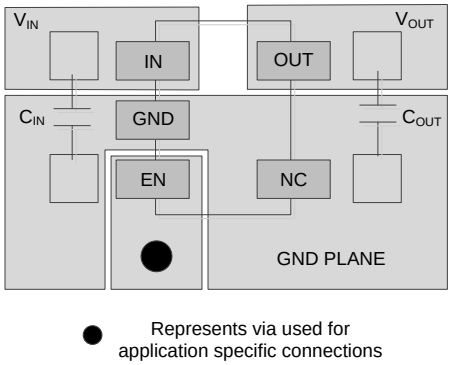



**Figure 24. Layout Example for the DCK and DDC Package**

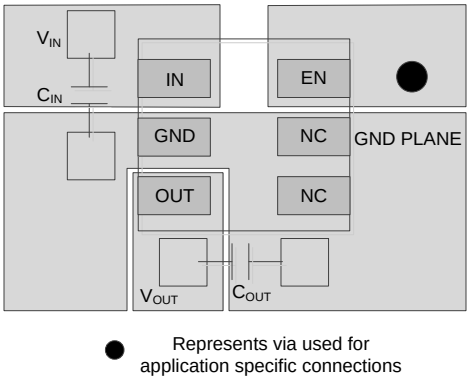



**Figure 25. Layout Example for the DSE Package**

## 10.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

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## Thermal Protection (continued)

The internal protection circuitry of the TLV700 has been designed to protect against overload conditions. The protection circuitry was not intended to replace proper heatsinking. Continuously running the TLV700 into thermal shutdown degrades device reliability.

## 10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ($P_D$) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$


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# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### *11.1.1.1 Evaluation Modules*

Three evaluation modules (EVMs) are available to assist in the initial circuit performance evaluation using the TLV700:

- TLV70033EVM-503
- TLV70018EVM-503
- TLV70028EVM-463

These EVMs can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

#### *11.1.1.2 Spice Models*

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV700 is available through the product folders under *Tools & Software*.

### 11.1.2 Device Nomenclature

**Table 3. Ordering Information(1)**

| PRODUCT | $V_{OUT}$ (2) |
|---|---|
| TLV700**xx** ***yyyz*** | **XX** is nominal output voltage (for example, 28 = 2.8 V).<br>**YYY** is the package designator.<br>**Z** is tape and reel quantity (R = 3000, T = 250). |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact factory for details and availability.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

- *Using the TLV700xxEVM-463 Evaluation Module*, SLUU390
- *Using the TLV700xxEVM-503 Evaluation Module*, SLUU391

## 11.3 Trademarks

*Bluetooth* is a registered trademark of Bluetooth SIG.
ZigBee is a registered trademark of the ZigBee Alliance.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70012DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODT | Samples |
| TLV70012DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODT | Samples |
| TLV70012DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODO | Samples |
| TLV70012DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODO | Samples |
| TLV70012DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NH | Samples |
| TLV70012DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NH | Samples |
| TLV70013DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SAH | Samples |
| TLV70013DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SAH | Samples |
| TLV70015DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODU | Samples |
| TLV70015DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODU | Samples |
| TLV70015DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODP | Samples |
| TLV70015DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODP | Samples |
| TLV70015DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NJ | Samples |
| TLV70015DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NJ | Samples |
| TLV70018DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODV | Samples |
| TLV70018DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODV | Samples |
| TLV70018DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODK | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70018DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODK | Samples |
| TLV70018DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NK | Samples |
| TLV70018DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | NK | Samples |
| TLV70019DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SCJ | Samples |
| TLV70019DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SCJ | Samples |
| TLV70022DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SCI | Samples |
| TLV70022DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SCI | Samples |
| TLV70025DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | QTP | Samples |
| TLV70025DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | QTP | Samples |
| TLV70025DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | DAU | Samples |
| TLV70025DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | DAU | Samples |
| TLV70025DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | QY | Samples |
| TLV70025DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | QY | Samples |
| TLV70028DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODW | Samples |
| TLV70028DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODW | Samples |
| TLV70028DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODL | Samples |
| TLV70028DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODL | Samples |
| TLV70028DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NL | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70028DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NL | Samples |
| TLV70029DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | QJ | Samples |
| TLV70029DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | QJ | Samples |
| TLV70030DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODR | Samples |
| TLV70030DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODR | Samples |
| TLV70030DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODM | Samples |
| TLV70030DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODM | Samples |
| TLV70030DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NP | Samples |
| TLV70030DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NP | Samples |
| TLV70031DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C4 | Samples |
| TLV70031DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C4 | Samples |
| TLV70032DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SCH | Samples |
| TLV70032DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SCH | Samples |
| TLV70033DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODS | Samples |
| TLV70033DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ODS | Samples |
| TLV70033DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODN | Samples |
| TLV70033DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ODN | Samples |
| TLV70033DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NR | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70033DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NR | Samples |
| TLV70036DDCR | ACTIVE | SOT | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SCG | Samples |
| TLV70036DDCT | ACTIVE | SOT | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SCG | Samples |
| TLV70036DSER | ACTIVE | WSON | DSE | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | UG | Samples |
| TLV70036DSET | ACTIVE | WSON | DSE | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | UG | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

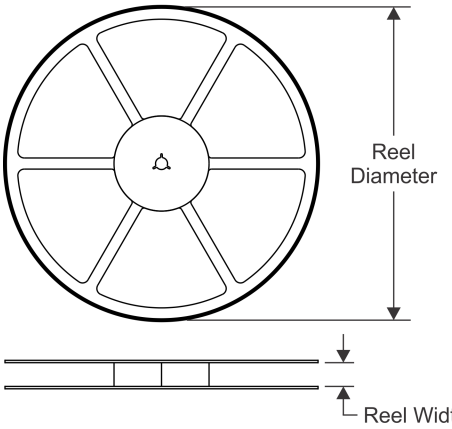
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

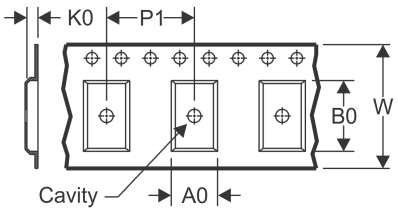
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

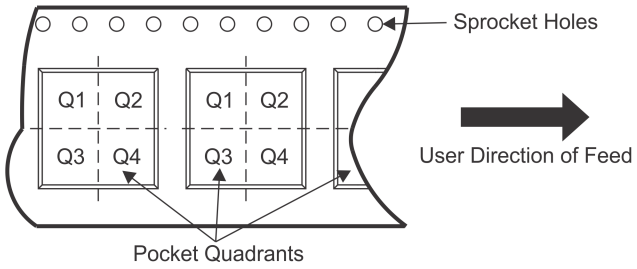



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



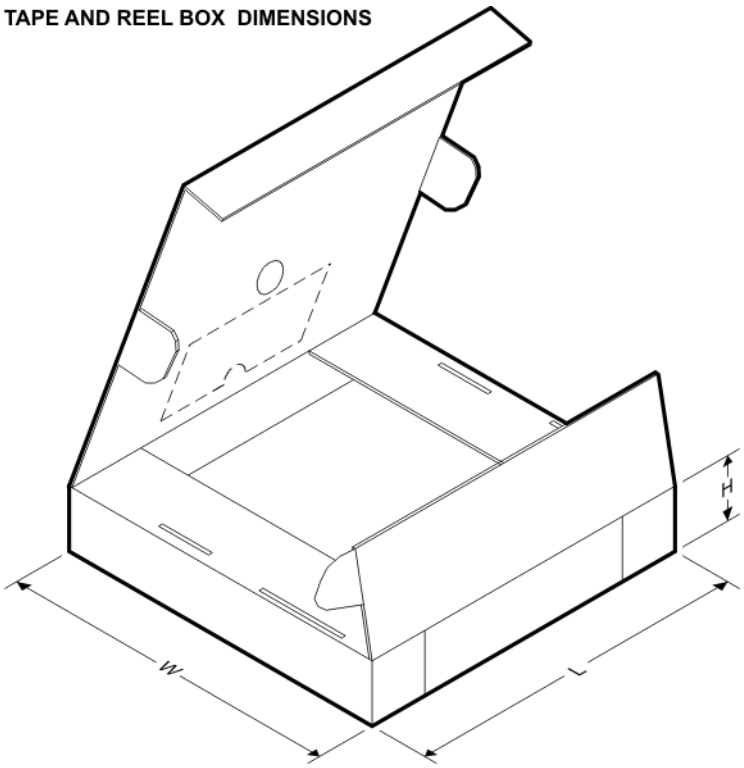

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70012DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70012DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70012DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70012DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70012DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70012DDCR | SOT | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70012DDCT | SOT | DDC | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70012DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70012DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70012DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70013DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70013DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70015DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70015DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70015DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70015DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70015DDCR | SOT | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70015DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70015DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70015DDCT | SOT | DDC | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70015DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70015DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70018DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70018DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70018DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70018DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70018DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70018DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70018DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70018DDCR | SOT | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70018DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70018DDCT | SOT | DDC | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70018DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70018DSER | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TLV70018DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70019DDCR | SOT | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70019DDCT | SOT | DDC | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70022DDCR | SOT | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70022DDCT | SOT | DDC | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70025DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70025DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70025DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70025DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70025DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70025DDCR | SOT | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70025DDCT | SOT | DDC | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70025DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70025DSER | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TLV70025DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70025DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70025DSET | WSON | DSE | 6 | 250 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TLV70028DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70028DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70028DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70028DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70028DDCR | SOT | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70028DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70028DDCT | SOT | DDC | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70028DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70028DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70028DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70029DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70029DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70030DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70030DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70030DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70030DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70030DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70030DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70030DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70030DDCR | SOT | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70030DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70030DDCT | SOT | DDC | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70030DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70030DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70031DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70031DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70032DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70032DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70033DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70033DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70033DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| TLV70033DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV70033DDCR | SOT | DDC | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70033DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70033DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70033DDCT | SOT | DDC | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV70033DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70033DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70036DDCR | SOT | DDC | 5 | 3000 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70036DDCT | SOT | DDC | 5 | 250 | 180.0 | 8.4 | 3.1 | 3.05 | 1.1 | 4.0 | 8.0 | Q3 |
| TLV70036DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |
| TLV70036DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.83 | 1.83 | 0.89 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



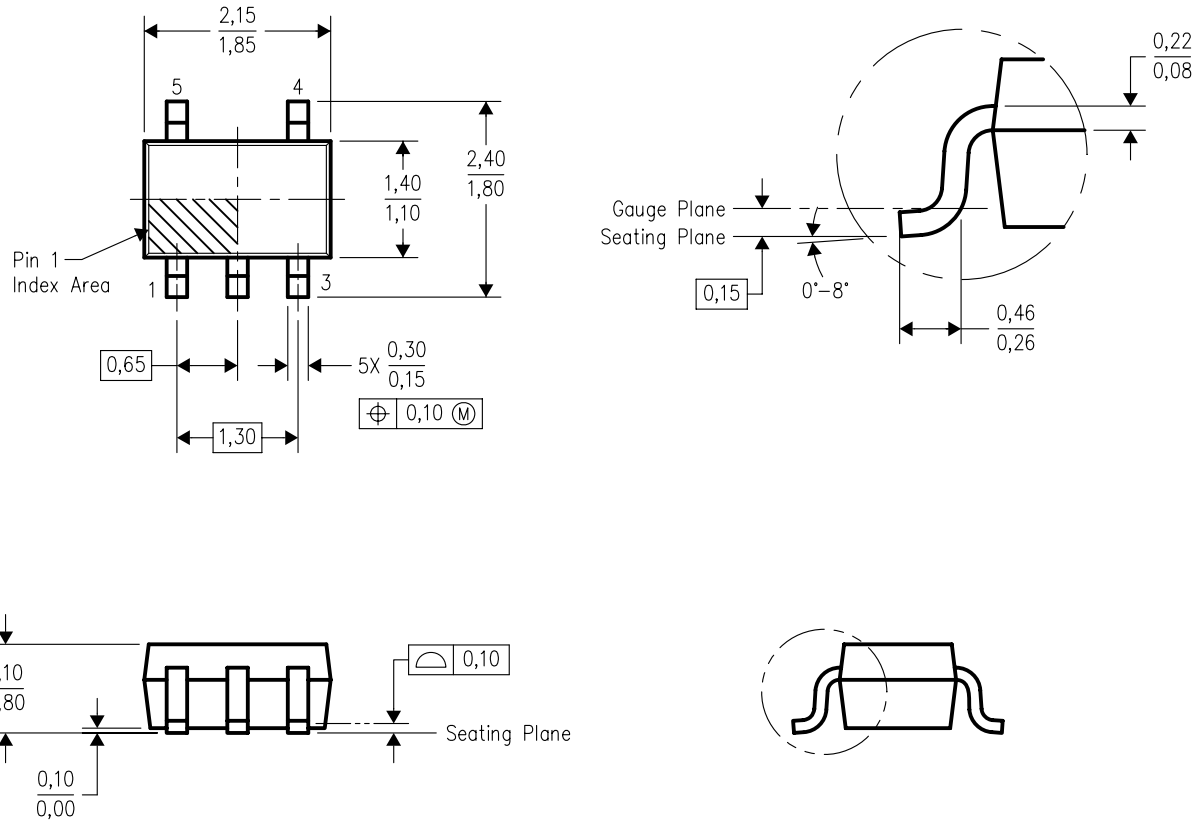

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV70012DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV70012DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70012DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70012DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV70012DDCR | SOT | DDC | 5 | 3000 | 406.0 | 348.0 | 63.0 |
| TLV70012DDCR | SOT | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70012DDCT | SOT | DDC | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TLV70012DDCT | SOT | DDC | 5 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70012DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70012DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70013DDCR | SOT | DDC | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70013DDCT | SOT | DDC | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV70015DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV70015DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70015DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70015DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV70015DDCR | SOT | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70015DDCR | SOT | DDC | 5 | 3000 | 223.0 | 270.0 | 35.0 |
| TLV70015DDCT | SOT | DDC | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV70015DDCT | SOT | DDC | 5 | 250 | 195.0 | 200.0 | 45.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV70015DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70015DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70018DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70018DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV70018DCKR | SC70 | DCK | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV70018DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TLV70018DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70018DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV70018DDCR | SOT | DDC | 5 | 3000 | 223.0 | 270.0 | 35.0 |
| TLV70018DDCR | SOT | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70018DDCT | SOT | DDC | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV70018DDCT | SOT | DDC | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TLV70018DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70018DSER | WSON | DSE | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV70018DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70019DDCR | SOT | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70019DDCT | SOT | DDC | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TLV70022DDCR | SOT | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70022DDCT | SOT | DDC | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TLV70025DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV70025DCKR | SC70 | DCK | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV70025DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TLV70025DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV70025DDCR | SOT | DDC | 5 | 3000 | 223.0 | 270.0 | 35.0 |
| TLV70025DDCR | SOT | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70025DDCT | SOT | DDC | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TLV70025DDCT | SOT | DDC | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV70025DSER | WSON | DSE | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV70025DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70025DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70025DSET | WSON | DSE | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TLV70028DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV70028DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70028DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV70028DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70028DDCR | SOT | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70028DDCR | SOT | DDC | 5 | 3000 | 223.0 | 270.0 | 35.0 |
| TLV70028DDCT | SOT | DDC | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TLV70028DDCT | SOT | DDC | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV70028DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70028DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70029DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70029DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70030DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV70030DCKR | SC70 | DCK | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV70030DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV70030DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TLV70030DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV70030DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70030DDCR | SOT | DDC | 5 | 3000 | 223.0 | 270.0 | 35.0 |
| TLV70030DDCR | SOT | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70030DDCT | SOT | DDC | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV70030DDCT | SOT | DDC | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TLV70030DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70030DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70031DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70031DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70032DDCR | SOT | DDC | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70032DDCT | SOT | DDC | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV70033DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70033DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV70033DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70033DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV70033DDCR | SOT | DDC | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| TLV70033DDCR | SOT | DDC | 5 | 3000 | 223.0 | 270.0 | 35.0 |
| TLV70033DDCT | SOT | DDC | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV70033DDCT | SOT | DDC | 5 | 250 | 195.0 | 200.0 | 45.0 |
| TLV70033DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70033DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TLV70036DDCR | SOT | DDC | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70036DDCT | SOT | DDC | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV70036DSER | WSON | DSE | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TLV70036DSET | WSON | DSE | 6 | 250 | 202.0 | 201.0 | 28.0 |

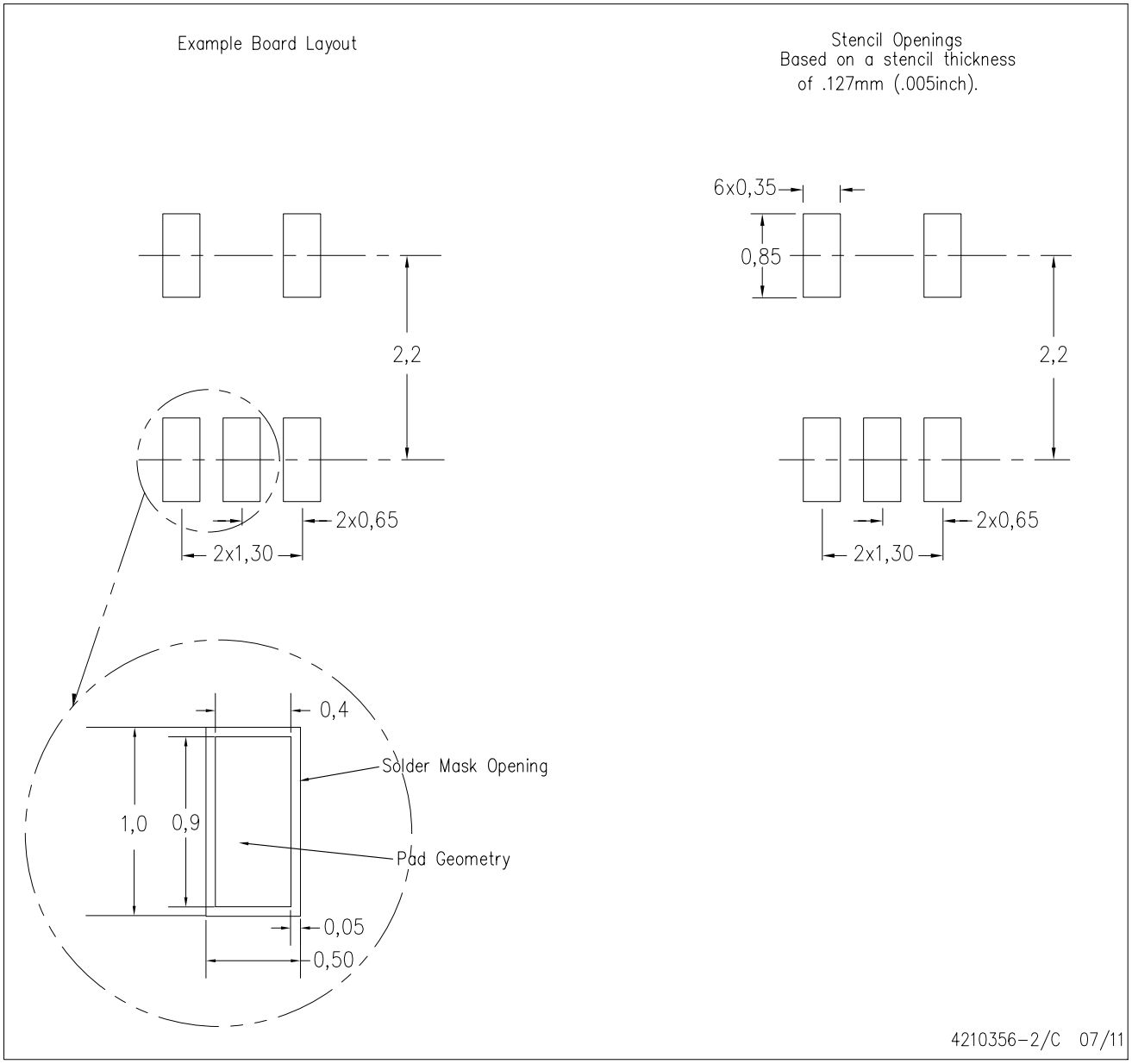
## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4093553–3/G 01/2007

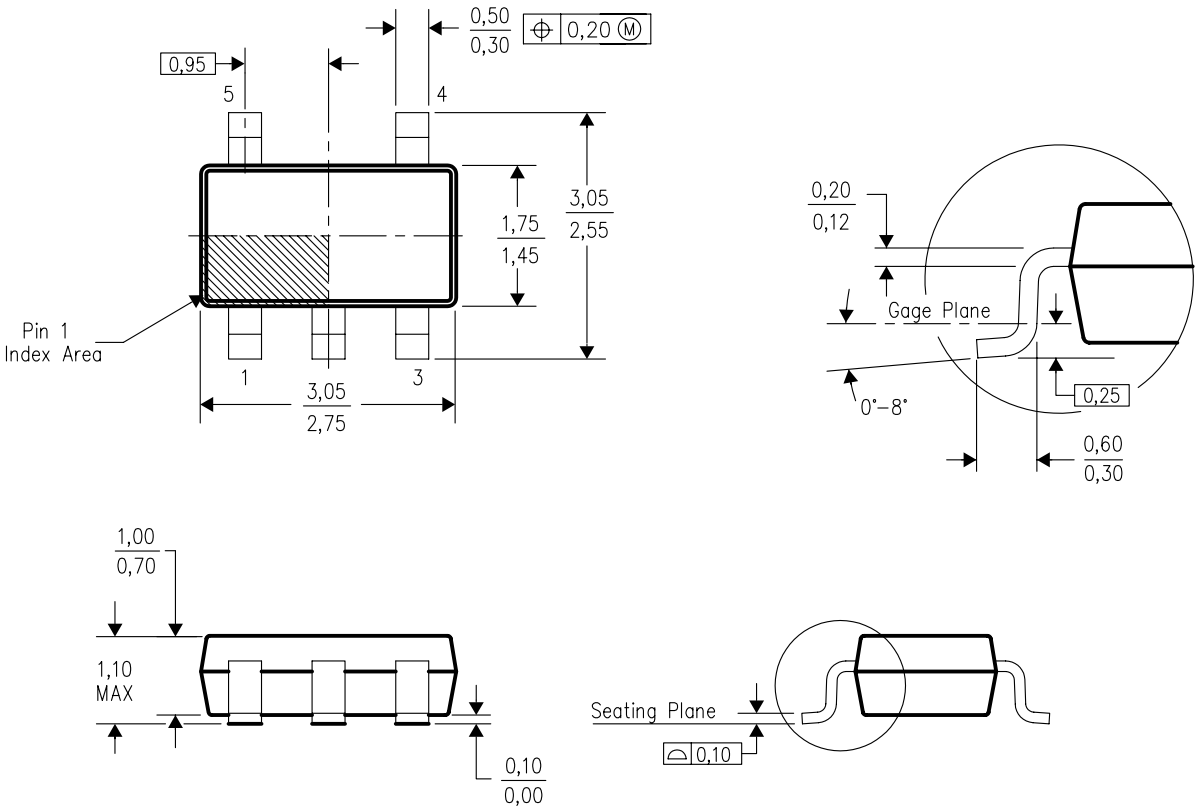
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

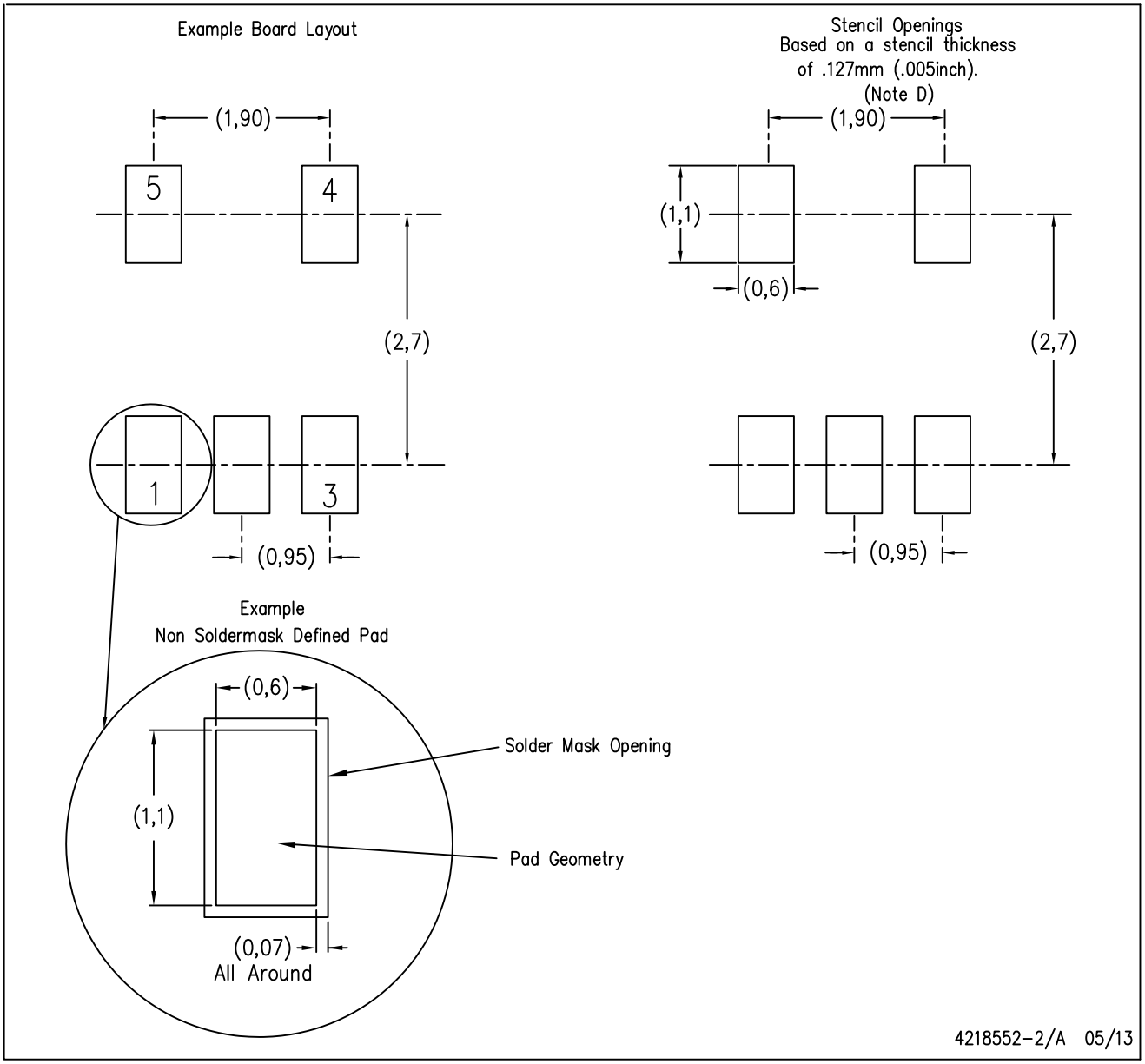
## DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE




4204403–2/E 06/05

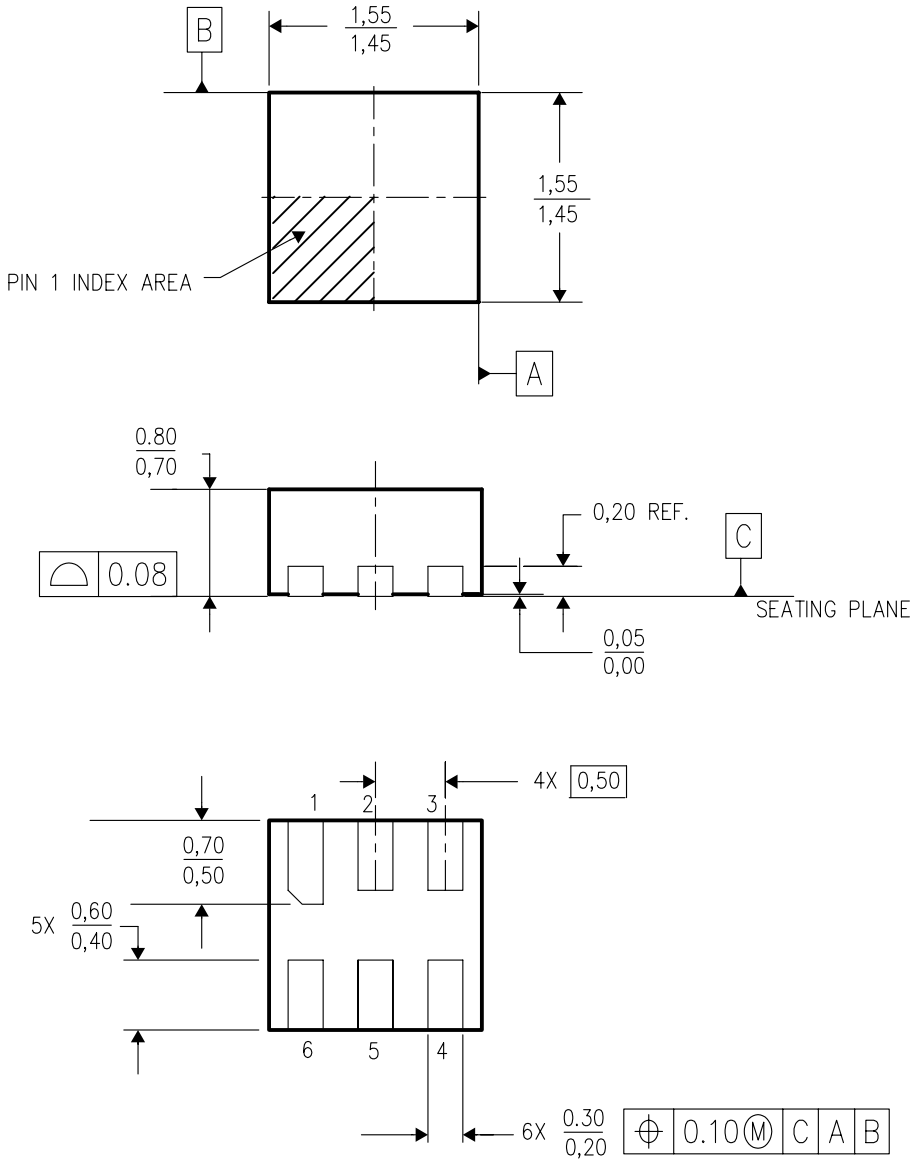
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

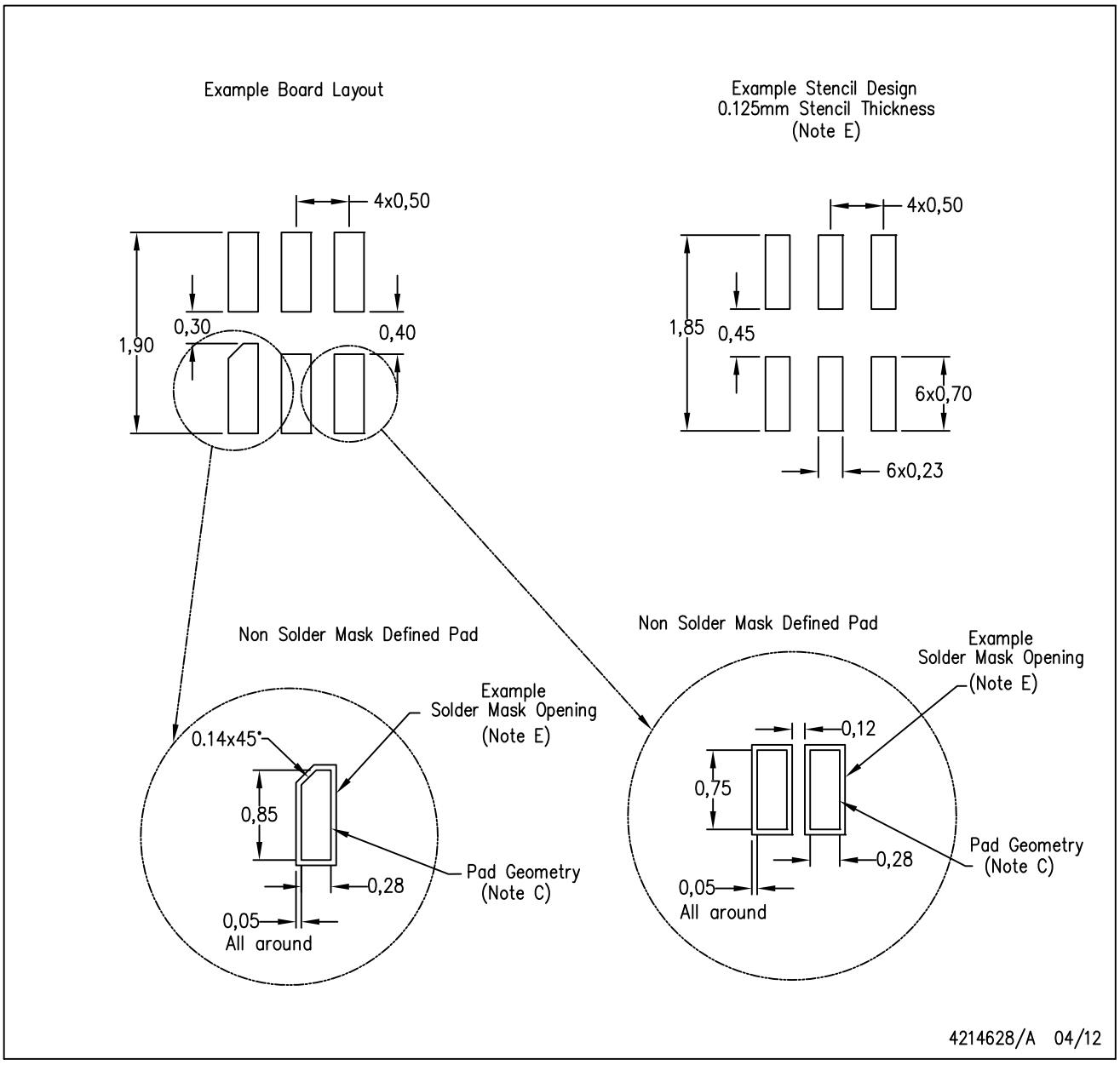
DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE




4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

# DSE (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for solder mask tolerances.

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