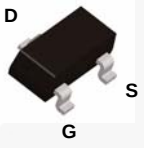
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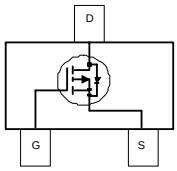
February 2013

BSS84
P-Channel Enhancement Mode Field-Effect Transistor

Features

- -0.13 A, -50 V, $R_{DS(ON)}$ = 10 Ω at V_{GS} = -5 V
- Voltage-Controlled P-Channel Small-Signal Switch
- High-Density Cell Design for Low $R_{DS(ON)}$
- High Saturation Current





Description

This P-channel enhancement-mode field-effect transistor is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process minimizes on-state resistance and to provide rugged and reliable performance and fast switching. The BSS84 can be used, with a minimum of effort, in most applications requiring up to 0.13 A DC and can deliver current up to 0.52 A. This product is particularly suited to low-voltage applications requiring a low-current high-side switch.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain-Source Voltage		–50	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current[1]	Continuous	–0.13	A
		Pulsed	–0.52	A
P_D	Maximum Power Dissipation[1]		0.36	W
	Derate Above 25°C		2.9	mW / °C
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds		300	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient[1]	350	°C/W

Note:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the user's board design.



a) 350°C/W when mounted on a minimum pad

Scale 1: 1 on letter-size paper.

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
SP	BSS84	7"	8mm	3000

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Electrical Characteristics[2]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–50			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–48		mV / °C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –50 V, V_{GS} = 0 V			–15	µA
		V_{DS} = –50 V, V_{GS} = 0 V, T_J = 125°C			–60	µA
I_{GSS}	Gate–Body Leakage.	V_{GS} = ±20 V, V_{DS} = 0 V			±10	nA
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–50			V
On Characteristics[2]						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –1 mA	–0.8	–1.7	–2	V
$\frac{V_{GS(TH)}}{T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –1 mA, Referenced to 25°C		3		mV / °C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –5 V, I_D = –0.10 A		1.2	10.0	Ω
		V_{GS} = –5 V, I_D = –0.10 A, T_J = 125°C		1.9	17.0	Ω
$I_{D(on)}$	On–State Drain Current	V_{GS} = –5 V, V_{DS} = – 10 V	–0.6			A
g_{FS}	Forward Transconductance	V_{DS} = –25 V, I_D = – 0.10 A	0.05	0.60		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = –25 V, V_{GS} = 0 V, f = 1.0 MHz		73		pF
C_{OSS}	Output Capacitance			10		pF
C_{RSS}	Reverse Transfer Capacitance			5		pF
R_G	Gate Resistance	V_{GS} = –15 mV, f = 1.0 MHz		9		Ω
Switching Characteristics[2]						
$t_{d(on)}$	Turn–On Delay	V_{DD} = –30 V, I_D = – 0.27 A, V_{GS} = –10 V, R_{GEN} = 6		2.5	5.0	ns
t_r	Turn–On Rise Time			6.3	13.0	ns
$t_{d(off)}$	Turn–Off Delay			10	20	ns
t_f	Turn–Off Fall Time			4.8	9.6	ns
Q_g	Total Gate Charge	V_{DS} = –25 V, I_D = –0.10 A, V_{GS} = –5 V		0.9	1.3	nC
Q_{gs}	Gate–Source Charge			0.2		nC
Q_{gd}	Gate–Drain Charge			0.3		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.13	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = - 0.26 A[2]		-0.8	-1.2	V
t_{RR}	Diode Reverse-Recovery Time	I_F = -0.1 A, d_{iF} / d_t = 100 A / µs[2]		10		ns
Q_{RR}	Diode Reverse-Recovery Charge			3		nC

Note:

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

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Typical Characteristics

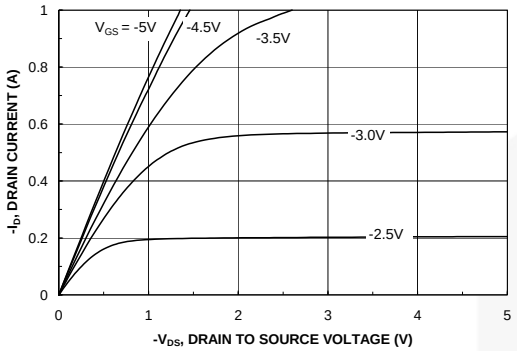


Figure 1. On-Region Characteristics

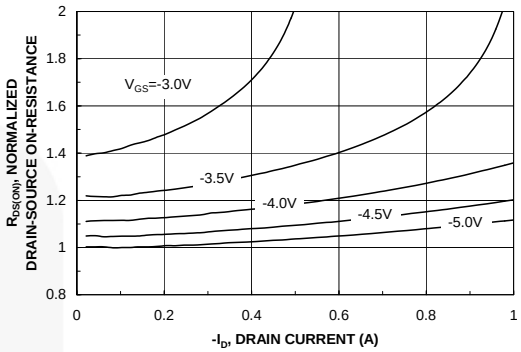


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

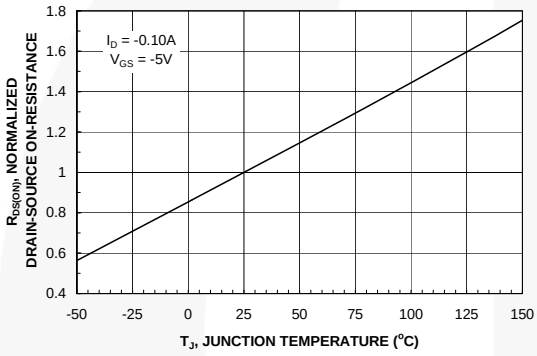


Figure 3. On-Resistance Variation with Temperature

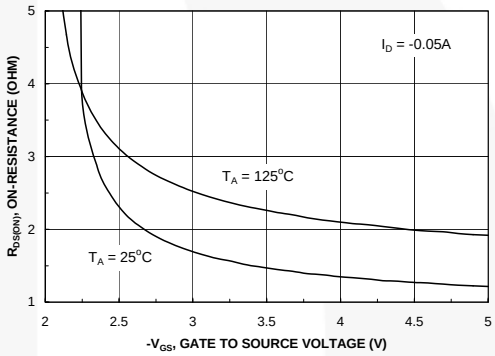


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

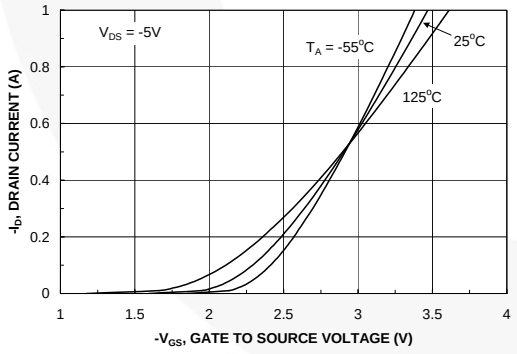


Figure 5. Transfer Characteristics

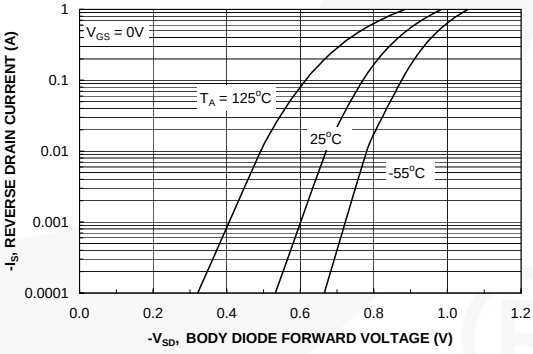


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

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Typical Characteristics (Continued)

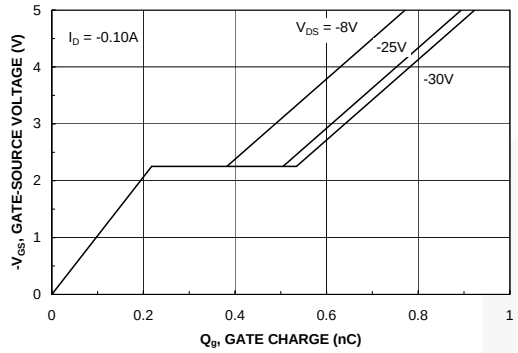


Figure 7. Gate Charge Characteristics

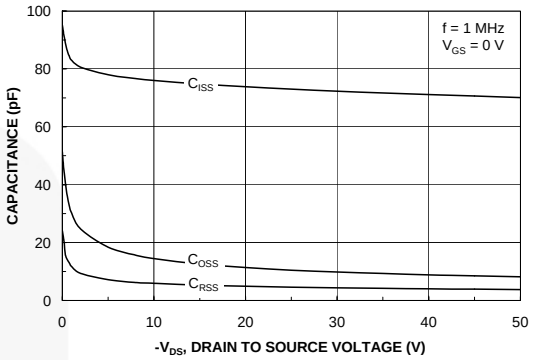


Figure 8. Capacitance Characteristics

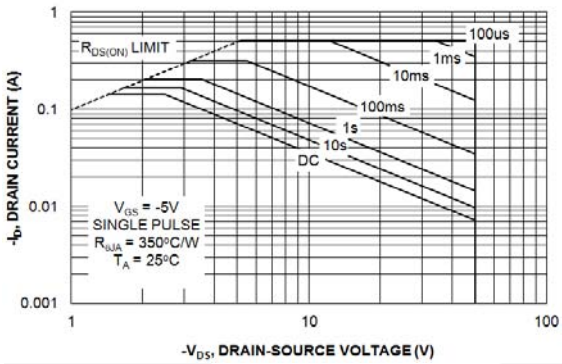


Figure 9. Maximum Safe Operating Area

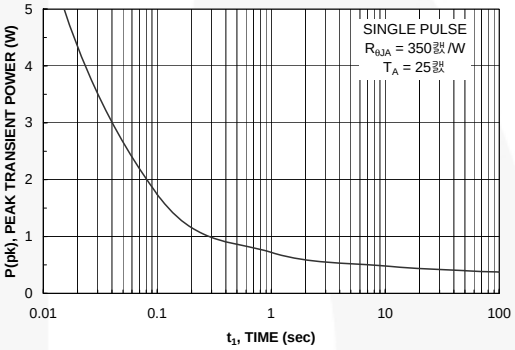


Figure 10. Single-Pulse Maximum Power Dissipation

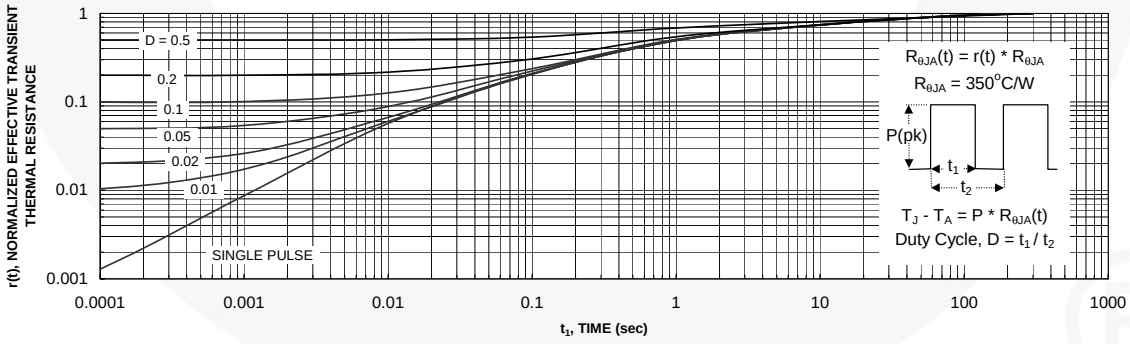


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described on page 1.
Transient thermal response will change depending on the circuit board design.

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Physical Dimension

SOT-23 3L

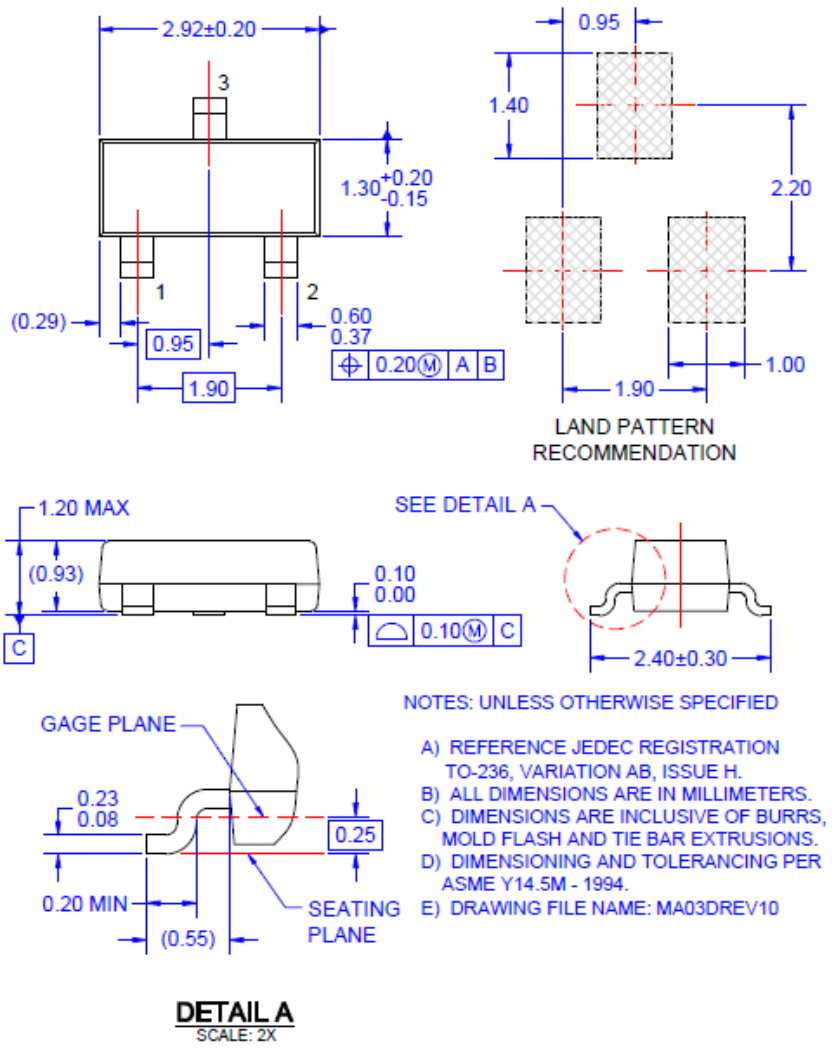


Figure 12. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE

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