

P-Channel Enhancement Mode Vertical DMOS FETs

Features

- High input impedance and high gain
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- Free from secondary breakdown

Applications

- Logic level interfaces - ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic systems
- Analog switches
- Power management
- Telecom switches

General Description

This low threshold enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options	BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$I_{D(ON)}$ (min) (mA)
	TO-236AB (SOT-23)			
TP0610T	TP0610T-G	-60	10	-50

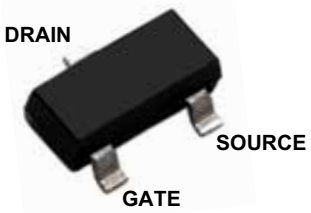
For packaged products, -G indicates package is RoHS compliant ('Green').
Consult factory for die / wafer form part numbers.
Refer to Die Specification VF21 for layout and dimensions.

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



TO-236AB (SOT-23) (T)

Product Marking



W = Code for week sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-236AB (SOT-23) (T)

Thermal Characteristics

Package	I_D (continuous)† (mA)	I_D (pulsed) (mA)	Power Dissipation @ T_A = 25°C (W)	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}† (mA)	I_{DRM} (mA)
TO-236AB (SOT-23)	-120	-400	0.36	200	350	-120	-400

† I_D (continuous) is limited by max rated T_j .

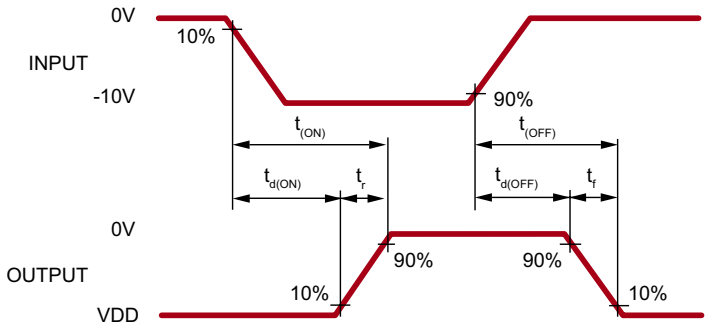
Electrical Characteristics (T_A = 25°C unless otherwise specified)

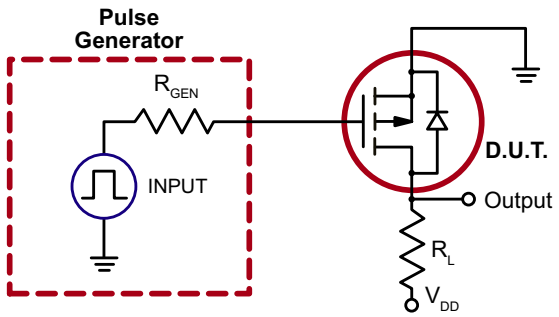
Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-60	-	-	V	V_{GS} = 0V, I_D = -10µA
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	V_{GS} = V_{DS}, I_D= -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	6.5	mV/°C	V_{GS} = V_{DS}, I_D= -1.0mA
I_{GSS}	Gate body leakage	-	-	±10	nA	V_{GS} = ± 20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	-1.0	µA	V_{GS} = 0V, V_{DS} = Max Rating
			-	-200		V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-50	-	-	mA	V_{GS} = -4.5V, V_{DS} = -10V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	25	Ω	V_{GS} = -4.5V, I_D = -25mA
			-	10		V_{GS} = -10V, I_D = -200mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/°C	V_{GS} = -10V, I_D = -200mA
G_{FS}	Forward transconductance	60	-	-	mmho	V_{DS} = -10V, I_D = -100mA
C_{ISS}	Input capacitance	-	-	60	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz
C_{OSS}	Common source output capacitance	-	-	30		
C_{RSS}	Reverse transfer capacitance	-	-	10		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	V_{DD} = -25V, I_D = -180mA, R_{GEN} = 25Ω
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	15		
t_f	Fall time	-	-	20		
V_{SD}	Diode forward voltage drop	-	-	-2.0	V	V_{GS} = 0V, I_{SD} = -120mA
t_{rr}	Reverse recovery time	-	400	-	ns	V_{GS} = 0V, I_{SD} = -400mA

Notes:

1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

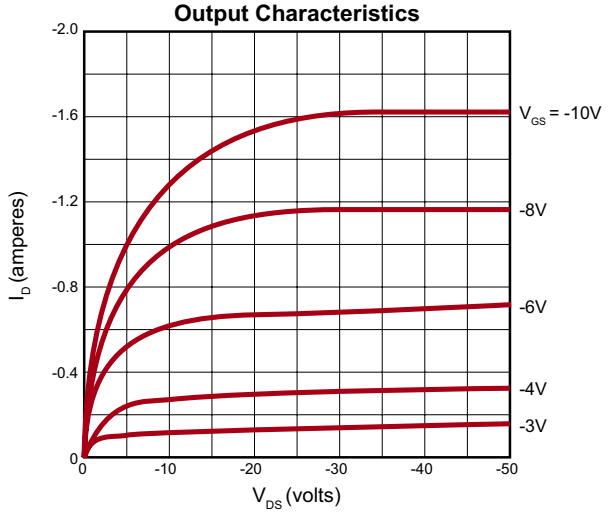
Switching Waveforms and Test Circuit



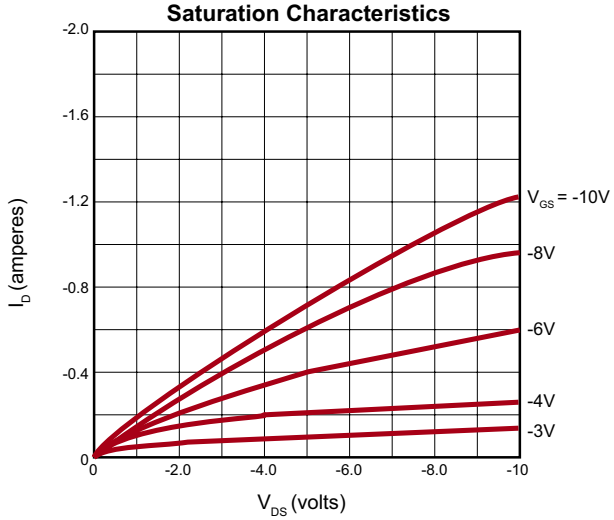


Typical Performance Curves

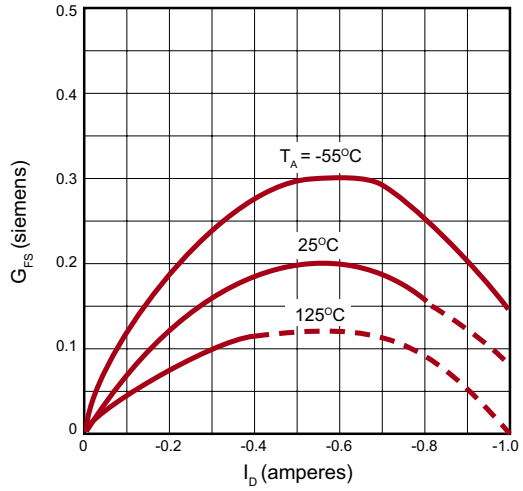
Output Characteristics



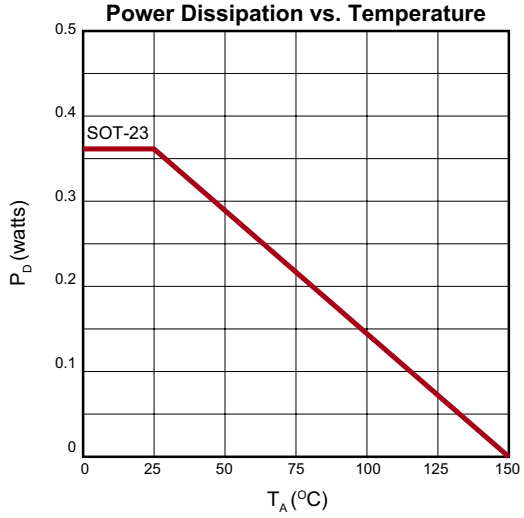
Saturation Characteristics



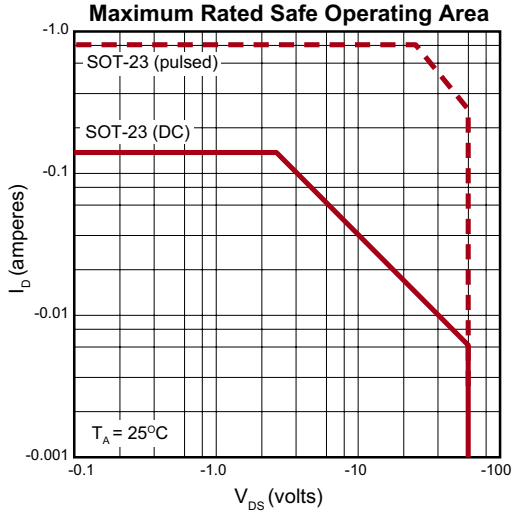
Transconductance vs. Drain Current



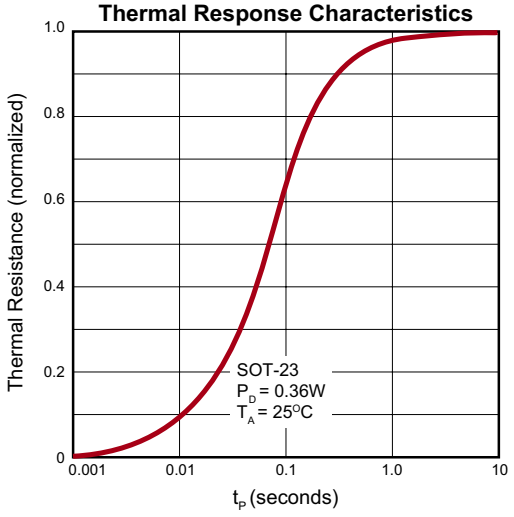
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area

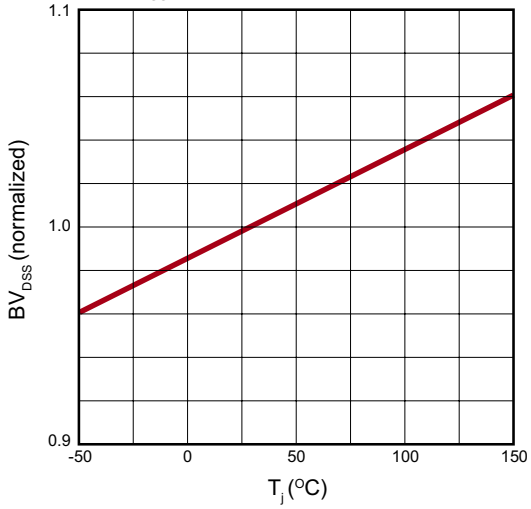


Thermal Response Characteristics

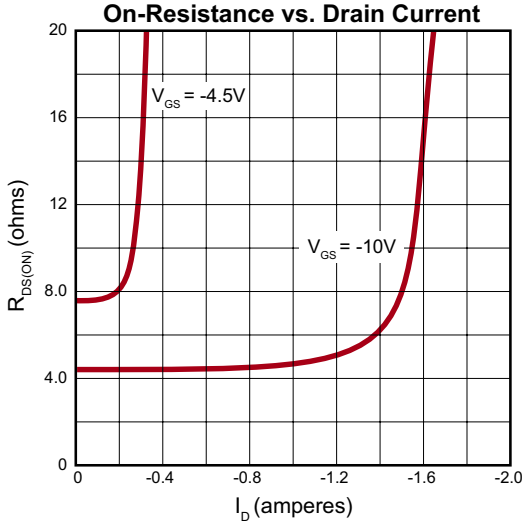


Typical Performance Curves *(cont.)*

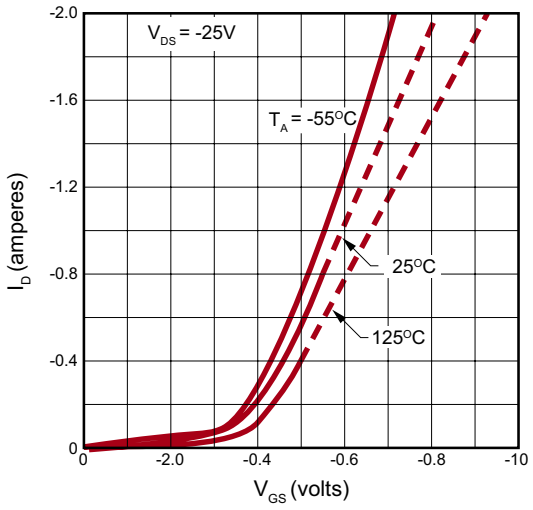
BV_{DSS} Variation with Temperature



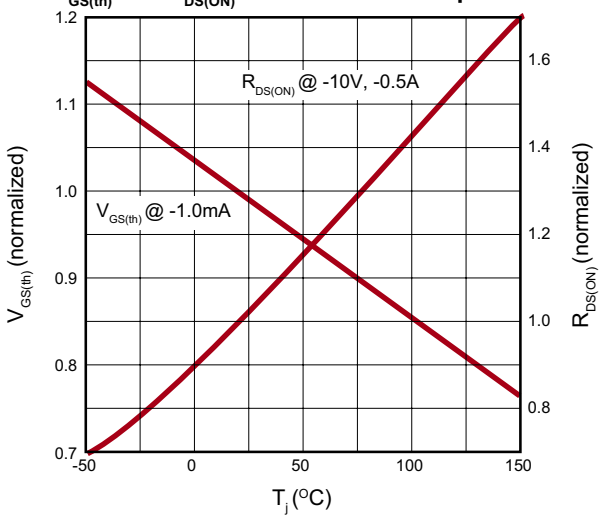
On-Resistance vs. Drain Current



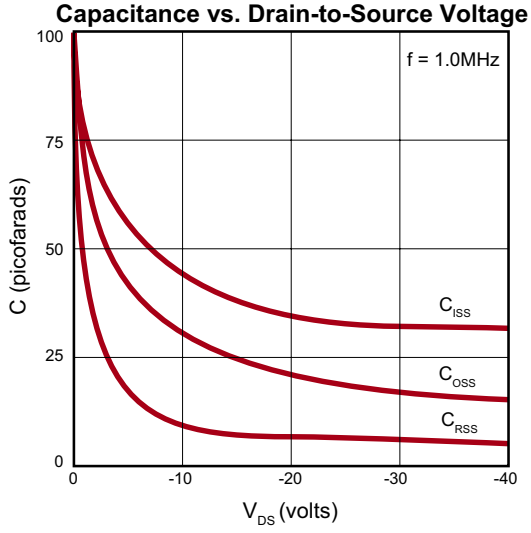
Transfer Characteristics



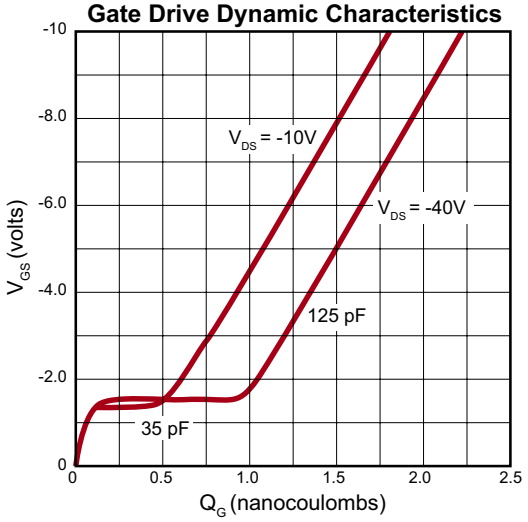
$V_{GS(th)}$ and $R_{DS(ON)}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage

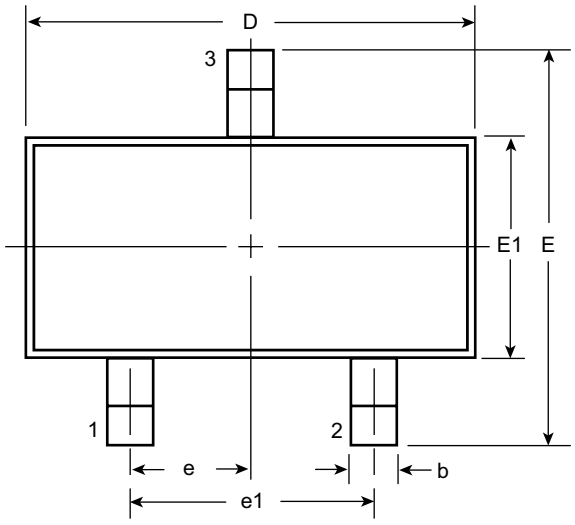


Gate Drive Dynamic Characteristics

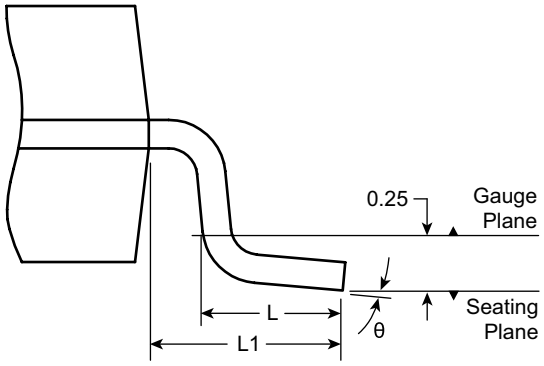


3-Lead TO-236AB (SOT-23) Package Outline (T)

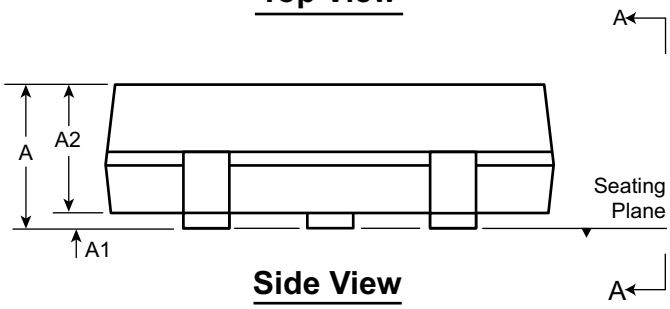
2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



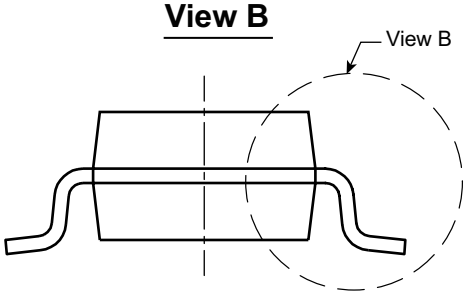
Top View



View B



Side View



View A - A

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20†	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO236ABK1, Version C041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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