4V Drive Pch+SBD MOSFET

US5U35

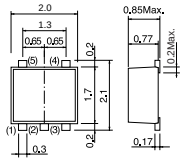
●**Structure**
Silicon P-channel MOSFET
Schottky Barrier DIODE

●**Features**
1) The US5U35 combines Pch MOSFET with a Schottky barrier diode in a TUMT5 package.
2) With fast switching.
3) Built-in schottky barrier diode has low forward voltage.

●**Applications**
Switching

●**Dimensions** (Unit : mm)

TUMT5

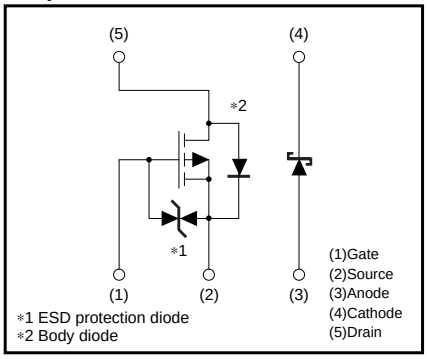


Abbreviated symbol : U35

●**Packaging specifications**

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US5U35		○

●**Equivalent circuit**



∗1 ESD protection diode
∗2 Body diode

●**Absolute maximum ratings** (Ta=25°C)

<MOSFET>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−45	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	±0.7	A
	Pulsed	I_{DP} *1	±2.8	A
Source current (Body diode)	Continuous	I_S	−0.4	A
	Pulsed	I_{SP} *1	−2.8	A
Channel temperature		Tch	150	°C
Power dissipation		P_D *3	0.7	W / ELEMENT

<Di>

Repetitive peak reverse voltage	V_{RM}	45	V
Reverse voltage	V_R	40	V
Forward current	I_F	100	mA
Forward current surge peak	I_{FSM} *2	1.0	A
Junction temperature	Tj	150	°C
Power dissipation	P_D *3	0.5	W / ELEMENT

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Power dissipation	P_D *3	1.0	W / TOTAL
Range of storage temperature	Tstg	−55 to +150	°C

*1 Pw≤10µs, Duty cycle≤1% *2 60Hz•1cyc. *3 Mounted on a ceramic board

●**Electrical characteristics** (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	µA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	−45	–	–	V	I_D=−1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	−1	µA	V_{DS}=−45V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	−1.0	–	−2.5	V	V_{DS}=−10V, I_D=−1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	0.6	0.8	Ω	I_D=−0.7A, V_{GS}=−10V
		–	0.9	1.3	Ω	I_D=−0.7A, V_{GS}=−4.5V
		–	1.0	1.4	Ω	I_D=−0.35A, V_{GS}=−4.0V
Forward transfer admittance	$\|Y_{fs}\|$ *	0.6	–	–	S	V_{DS}=−10V, I_D=−0.7A
Input capacitance	C_{iss}	–	120	–	pF	V_{DS}=−10V
Output capacitance	C_{oss}	–	14	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	11	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	6	–	ns	I_D=−0.35A, V_{DD}≒−25V, V_{GS}=−10V, R_L≒71Ω, R_G=10Ω
Rise time	t_r *	–	5	–	ns	
Turn-off delay time	$t_{d\ (off)}$ *	–	17	–	ns	
Fall time	t_f *	–	6	–	ns	
Total gate charge	Q_g	–	1.7	–	nC	V_{DD}≒−25V, V_{GS}=−5V
Gate-source charge	Q_{gs}	–	0.8	–	nC	I_D=−0.7A
Gate-drain charge	Q_{gd}	–	0.5	–	nC	R_L≒36Ω, R_G=10Ω

* Pulsed

<Body diode (source−drain)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	−1.2	V	I_S=−0.7A, V_{GS}=0V

* Pulsed

<Di>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_F	–	–	0.55	V	I_F=100mA
Reverse current	I_R	–	–	30	µA	V_R=10V

●**Electrical characteristic curves**

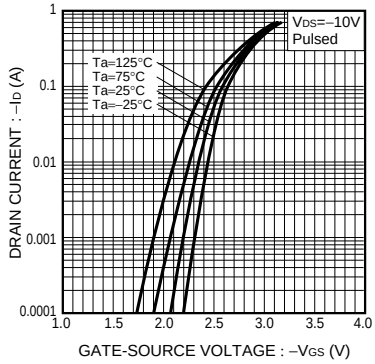


Fig.1 Typical Transfer Characteristics

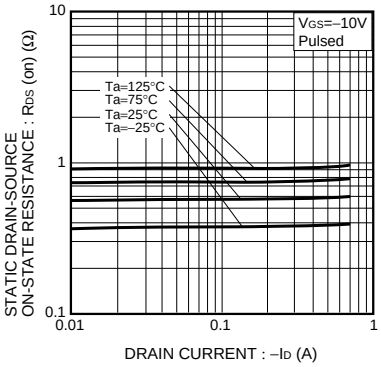


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current(I)

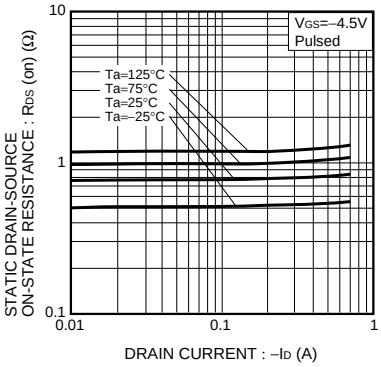


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current(II)

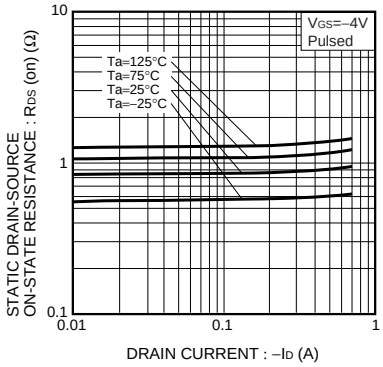


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(III)

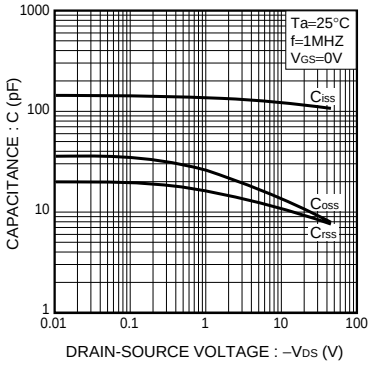


Fig.5 Typical Capacitance vs. Drain-Source Voltage

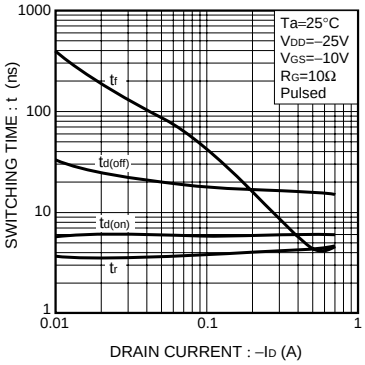


Fig.6 Switching Characteristics

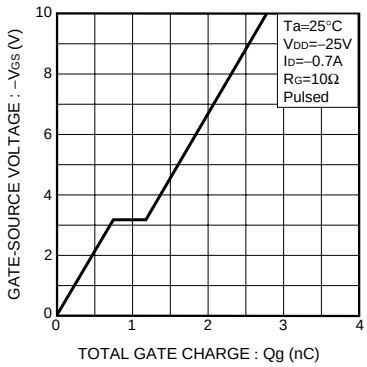


Fig.7 Dynamic Input Characteristics

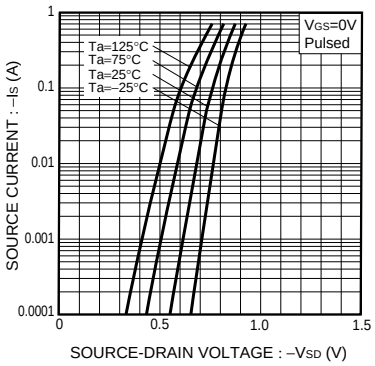


Fig.8 Source Current vs. Source-Drain Voltage

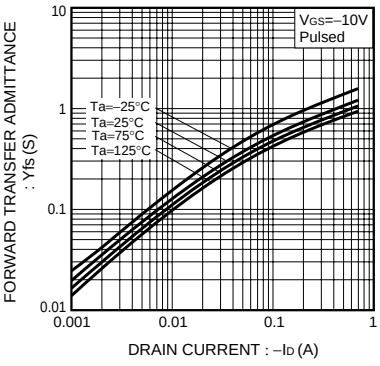


Fig.9 Forward Transfer Admittance vs.Drain Current

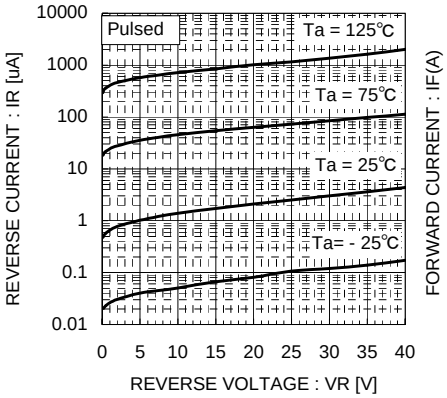


Fig.10 Reverse Current vs. Reverse Voltage

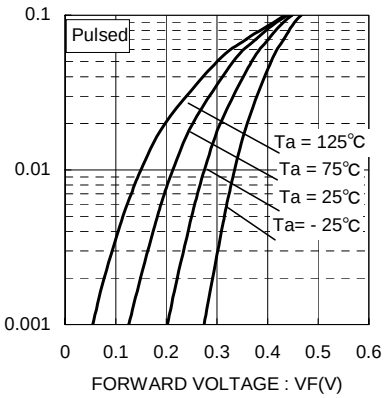


Fig.11 Forward Current vs. Forward Voltage

●Notice

1. SBD has a large reverse leak current compared to other type of diode. Therefore; it would raise a junction temperature, and increase a reverse power loss. Further rise of inside temperature would cause a thermal runaway.
   This built-in SBD has low V_F characteristics and therefore, higher leak current. Please consider enough the surrounding temperature, generating heat of MOSFET and the reverse current.
2. This product might cause chip aging and breakdown under the large electrified environment.
   Please consider to design ESD protection circuit.

●**Measurement circuits**

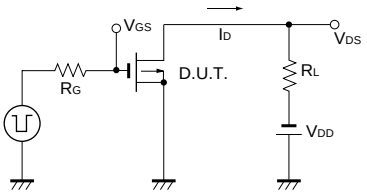


Fig.12 Switching Time Measurement Circuit

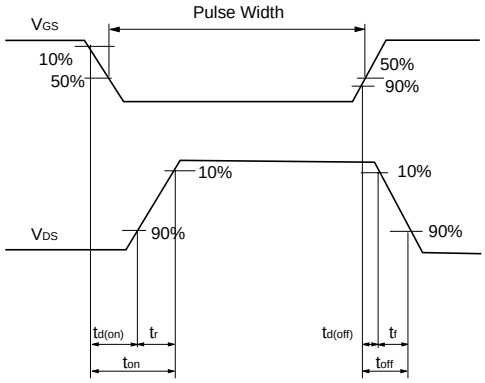


Fig.13 Switching Waveforms

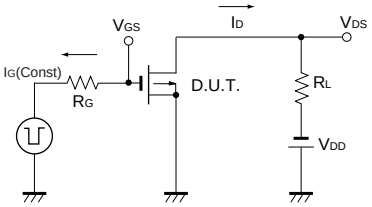


Fig.14 Gate Charge Measurement Circuit

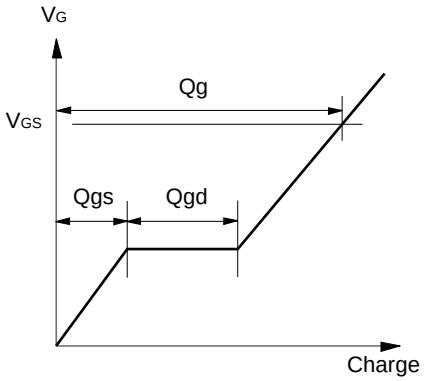


Fig.15 Gate Charge Waveforms

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