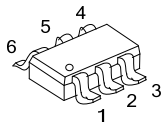
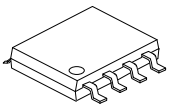
UC3863

*LINEAR INTEGRATED CIRCUIT*

# LOW COST POWER-SAVING MODE PWM CONTROLLER FOR FLYBACK CONVERTERS




SOT-26



SOP-8

## ■ DESCRIPTION

The **UC3863** is a high performance current mode PWM controller ideally suited for low standby power. The PWM switching frequency is programmable externally at normal operation. Low $V_{DD}$ startup current make the power reliable on startup design and a large value resistor could be used in the startup circuit to minimize the standby power. At no load condition, the IC operates in power-saving mode for lower standby power, decreasing frequency for Higher conversion efficiency at light load condition.

The **UC3863** contains protection with automatic recovery including OLP (over load protection), OTP (over temperature protection), OVP (over voltage protection), UVLO ($V_{DD}$ over voltage clamp and under voltage lockout).To protect the power MOSFET, Gate-drive output is fixed up to 15V max. The **UC3863** contains protection OCP (cycle-by-cycle current limiting).

The internal slope compensation improves system stability at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch, which offering minimal external component count in the design. Excellent EMI performance is achieved with UTC proprietary frequency hopping technique (ZL201020615247.1) together with soft driver control. Audio noise is eliminated due to switch frequency more than 20kHz during operation.

The **UC3863** has such applications as: battery charger, power adaptor, set-top box power supplies, ink jet printers, open-frame SMPS

## ■ FEATURES

* UTC proprietary frequency hopping technology for Improved EMI performance.
* Power-saving mode for high light-load and standby efficiency
* Dynamic peak current limiting for constant output power
* Built-in synchronized slope compensation
* OTP,OLP,OVP and $V_{DD}$ clamp for higher security
* Programmable PWM Frequency
* Gate output voltage clamped at 15V
* Low start-up current
* Cycle-by-cycle Current Limiting
* Under voltage lockout (UVLO)
* Few external components required


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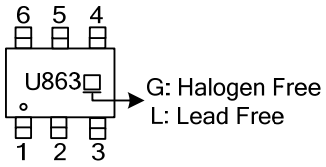
## ■ ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|---|---|---|---|
| Lead Free | Halogen Free | | |
| UC3863L-AG6-R | UC3863G-AG6-R | SOT-26 | Tape Reel |
| UC3863L-S08-T | UC3863G-S08-T | SOP-8 | Tube |
| UC3863L-S08-R | UC3863G-S08-R | SOP-8 | Tape Reel |

Note: xx: Output Voltage, refer to Marking Information.

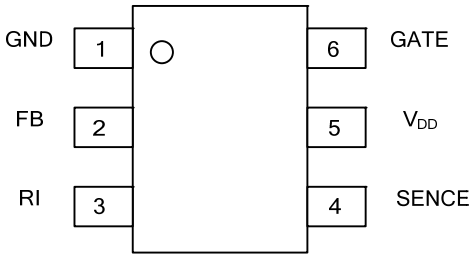
| | |
|---|---|
| UC3863L-AG6-R<br>(1)Packing Type<br>(2)Package Type<br>(3)Halogen Free | (1) R: Tape Reel, T: Tube<br>(2) AG6: SOT-26, S08: SOP-8<br>(3) L: Lead Free, G: Halogen Free |

## ■ MARKING INFORMATION(For SOT-26)

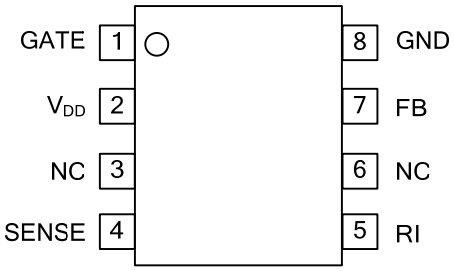



## ■ PIN CONFIGURATION

SOT-26



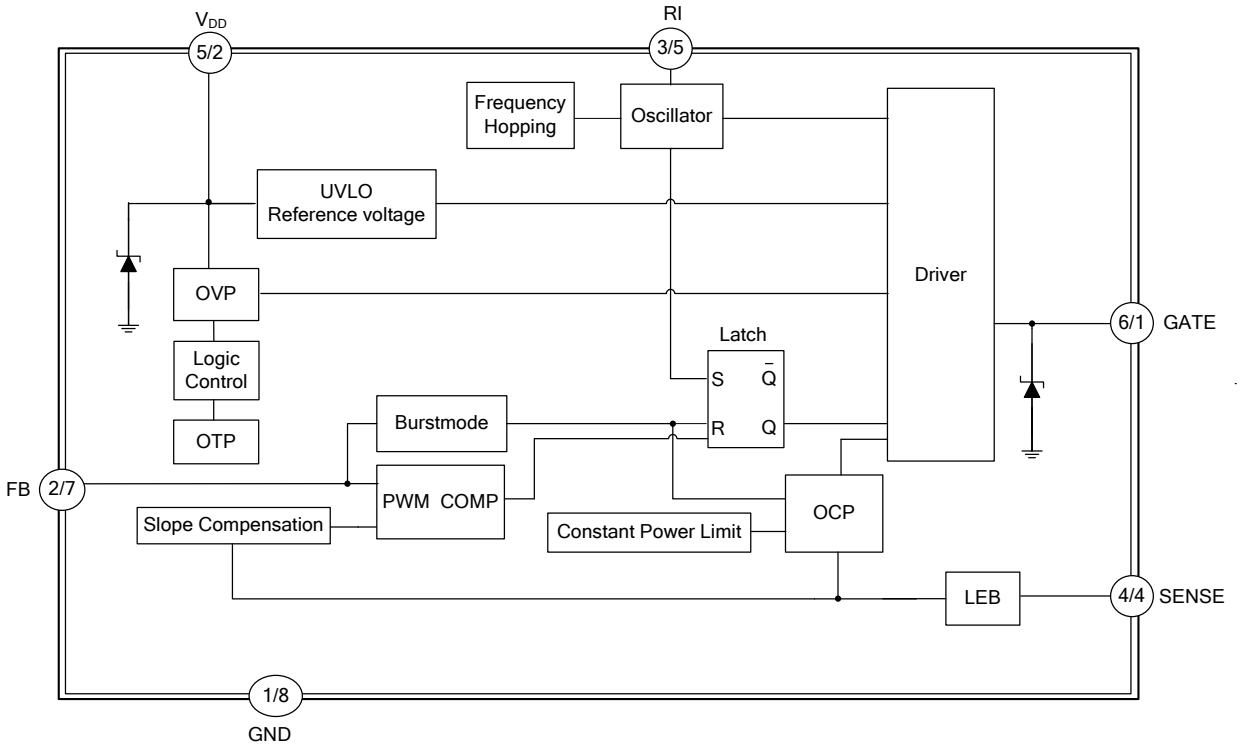

SOP-8




## ■ PIN DESCRIPTION

| PIN NO. | | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|---|
| SOT-26 | SOP-8 | | | |
| 1 | 8 | GND | P | Ground. |
| 2 | 7 | FB | I | Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input. |
| 3 | 5 | RI | I | A resistor connected between RI and GND sets switching frequency. A 100kΩ resistor $R_I$ results in a 65KHz switching frequency. |
| 4 | 4 | SENSE | I | Current sense input pin. Connected to MOSFET current sensing resistor node. |
| 5 | 2 | $V_{DD}$ | P | Power supply. |
| 6 | 1 | GATE | O | The totem-pole output driver for driving the power MOSFET. |
| - | 3, 6 | NC | - | No Connection |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS ($T_A$=25°C, $V_{DD}$ =15V, unless otherwise specified)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 30 | V |
| Input Voltage to FB Pin | $V_{FB}$ | -0.3 ~ 7 | V |
| Input Voltage to CS Pin | $V_{SENSE}$ | -0.3 ~ 7 | V |
| Junction Temperature | $T_J$ | +150 | °C |
| Operating Temperature | $T_{OPR}$ | -40 ~ +125 | °C |
| Storage Temperature | $T_{STG}$ | -50 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ OPERATING RANGE

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 10 ~ 26 | V |

## ■ ELECTRICAL CHARACTERISTICS ($T_A$=25°C, $V_{DD}$=15V, $R_I$ =100KΩ，unless otherwise specified)

| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY SECTION** | | | | | | | |
| Start Up Current | | $I_{STR}$ | $V_{DD}$ = $V_{DD(ON)}$-0.1V | | 5 | 20 | μA |
| IC Operating current | | $I_{OP}$ | $V_{FB}$=3.5V | | 1.5 | 5 | mA |
| VDD Zener Clamp current | | $I_{CLAMP}$ | $V_{DD}$>$V_{OVP}$ | | 15 | | mA |
| **UNDER-VOLTAGE LOCKOUT SECTION** | | | | | | | |
| Start Threshold Voltage | | $V_{THD(ON)}$ | | 13 | 14 | 15 | V |
| Min. Operating Voltage | | $V_{DD(MIN)}$ | | 7.5 | | 12 | V |
| **CONTROL SECTION** | | | | | | | |
| $V_{FB}$ Open Loop Voltage Level | | $V_{FB-OPEN}$ | | | 5 | | V |
| PWM Input Gain | | $A_{VCS}$ | $\Delta V_{FB}/\Delta V_{CS}$ | | 3 | | V/V |
| Burst-Mode Out FB Voltage | | $V_{FB(OUT)}$ | $V_{SENSE}$ =0 | | 1.1 | | V |
| Reduce-Frequency end FB Voltage | | $V_{FB(END)}$ | $V_{SENSE}$ =0 | | 1.8 | | V |
| Burst-Mode Enter FB Voltage | | $V_{FB(IN)}$ | $V_{SENSE}$ =0 | | 0.9 | | V |
| Switch Frequency | Normal | $F_{SW}$ | $V_{FB}$=3.5V, RI=100KΩ | 60 | 65 | 70 | KHz |
| | Power-Saving | | Before enter burst mode | | 22 | | KHz |
| Duty Cycle | | $D_{MAX}$ | $V_{FB}$=3.5V, $V_{SENSE}$=0 | | 75 | | % |
| Frequency Hopping | | $F_{J(SW)}$ | | -4 | | +4 | % |
| Frequency VDD Stability | | $F_{DV}$ | $V_{DD}$=12V~20V | | | 5 | % |
| Frequency Temperature Stability | | $F_{DT}$ | T=-20~100°C | | 1.5 | 5 | % |
| RI Resistor Value Range | | $R_I$ | | 50 | 100 | 150 | KΩ |
| Feedback Resistor | | $R_{FB}$ | | | 11 | | KΩ |
| **PROTECTION SECTION** | | | | | | | |
| VCC Over Voltage Protection Threshold | | $V_{OVP}$ | $V_{FB}$=4.2V | | 26 | | V |
| FB PIN Over Load Protection Threshold | | $V_{OLP}$ | | 4.7 | 4.5 | 5.2 | V |
| Over Load Protection Delay-Time | | $T_{Delay}$ | | | 55 | | mS |
| OTP threshold | | $T_{(THR)}$ | $V_{FB}$=4.2V | | 135 | | °C |
| **CURRENT LIMITING SECTION** | | | | | | | |
| Peak Current Flat Threshold Voltage | | $V_{CS-F}$ | $V_{FB}$=4.2V, Duty≥60% | 0.6 | 0.65 | 0.7 | V |
| Peak Current Valley Threshold Voltage | | $V_{CS-V}$ | $V_{FB}$=4.2V, Duty=0% | 0.6 | 0.65 | 0.7 | V |
| Lead Edge Blanking Time | | $T_{LEB}$ | | | 400 | | ns |
| **DRIVER OUTPUT SECTION** | | | | | | | |
| Output Voltage Low State | | $V_{OL}$ | $V_{DD}$=16,$I_O$=-20mA | | | 0.8 | V |
| Output Voltage High State | | $V_{OH}$ | $V_{DD}$=16,$I_O$= 20mA | 11 | | | V |
| Output Voltage Rise Time | | $t_R$ | $C_L$=1.0nF | | 100 | | ns |
| Output Voltage Fall Time | | $t_F$ | $C_L$=1.0nF | | 60 | | ns |

## ■ OPERATION DESCRIPTION

The **UC3863** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the **UC3863** series.

**Start-up Current**

The start-up current is only 5μA. Low start-up current allows a start-up resistor with a high resistance and a low-wattage to supply the start-up power for the controller. For AC/DC adaptor with universal input range design, a 2.5~3MΩ, 1/8W startup resistor could be used together with a $V_{DD}$ capacitor to provide a fast startup and low power dissipation solution.

**Power-Saving Mode Operation**

The proprietary Power-Saving Mode function provides linearly decreasing the switching frequency under light-load conditions for higher efficiency. The feedback voltage, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback voltage dropped below the threshold voltage, the switching frequency starts to decrease. This Power-Saving Mode function dramatically reduces power consumption under light-load conditions. The 22KHz minimum frequency control also eliminates the audio noise at any loading conditions.

At zero load condition, the magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. The **UC3863** enter burst mode at standby condition to minimize the switching loss and reduces the standby power consumption. Power supplies using the **UC3863** can easily meet even the strictest regulations regarding standby power consumption.

**Switch Frequency Set**

The maximum switch frequency is set through the 100KΩ RI-pin resistor to 65KHz. Switch frequency is modulated by output power $P_{OUT}$ during IC operating. At no load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. So lower switch frequency at lower load, which more and more improve IC's efficiency at light load. At from no load to light load condition, The IC will operate at from Burst mode to Reducing Frequency Mode. The relation curve between $f_{SW}$ and $P_{OUT}/P_{OUT\ (MAX)}$ as followed Fig.1. The maximum switch frequency is set through the RI-pin resistor RI: $F_{SW}$=6500/RI (KΩ) KHz.

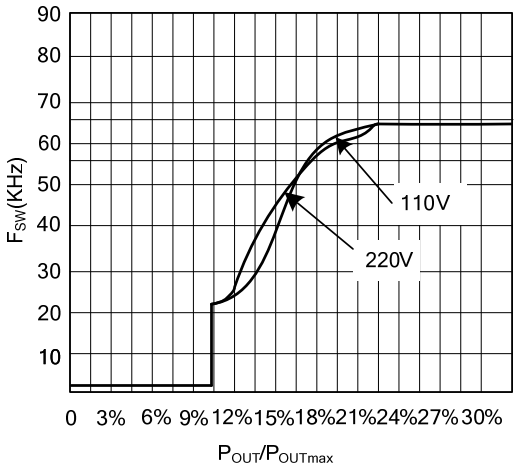



Fig.1 The relation curve between $f_{SW}$ and relative output power $P_{OUT}$/ $P_{OUT\ (MAX)}$

## ■ OPERATION DESCRIPTION (Cont.)

**Frequency Hopping For EMI Improvement**

The Frequency hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed Fig.2. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

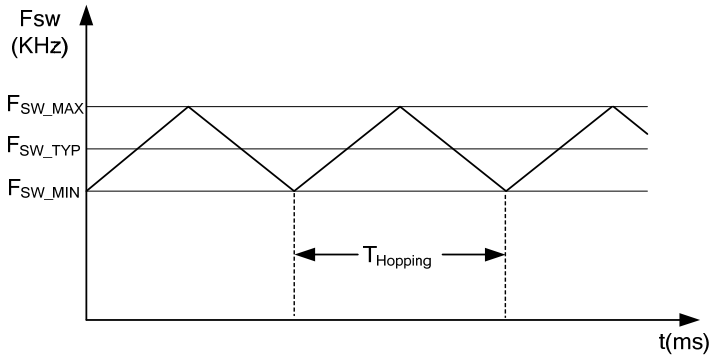



Fig.2 Frequency Hopping

**Built-in Slope Compensation**

Built-in slope compensation circuit greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation.

**Leading-Edge Blanking**

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a 400ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

**Constant Output Power Limit**

When the SENSE voltage, across the sense resistor $R_S$, reaches the threshold voltage, around 0.8V, the output GATE drive will be turned off after a small propagation delay $t_D$. This propagation delay will introduce an additional current proportional to $t_D \times V_{IN}/Lp$. Since the propagation delay is nearly constant regardless of the input line voltage $V_{IN}$. Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To compensate this variation for wide AC input range, the threshold voltage is adjusted by the $V_{IN}$ current. Since $V_{IN}$ pin is connected to the rectified input line voltage through a resistor $R_{VIN}$, a higher line voltage will generate higher $V_{IN}$ current into the $V_{IN}$ pin. The threshold voltage is decreased if the $V_{IN}$ current is increased. Smaller threshold voltage, forces the output GATE drive to terminate earlier, thus reduce the total PWM turn-on time and make the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for wide AC input voltage from 90VAC to 264VAC.

**Under Voltage Lockout (UVLO)**

The turn-on and turn-off thresholds of the **UC3863** are fixed internally at 15.8V/10V. During start-up, the hold-up capacitor must be charged to 15.8V through the start-up resistor, so that the **UC3863** will be enabled. The hold-up capacitor will continue to supply $V_{DD}$ until power can be delivered from the auxiliary winding of the main transformer. $V_{DD}$ must not drop below 10V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor will be adequate to supply $V_{DD}$ during start-up.

**Gate Output**

The **UC3863** output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. A good tradeoff is achieved through dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 15V clamp is added for MOSFET gate protection at higher than expected $V_{DD}$ input.

## ■ OPERATION DESCRIPTION (Cont.)

**Protection Controls**

The IC takes on more protection functions such as OVP, OLP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. Driver is reset after failure is eliminated.

**OVP**

The OVP will shut down the switching of the power MOSFET whenever $V_{DD}$ >$V_{OVP}$. The OVP event as followed Fig.3.

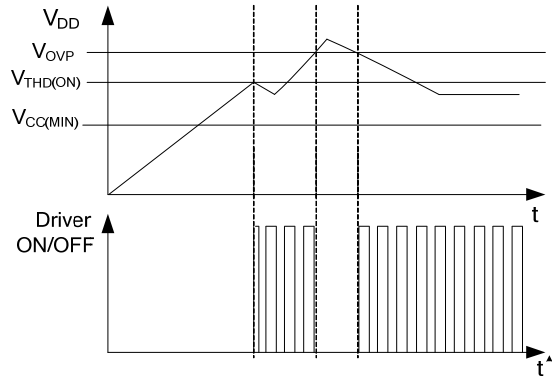



Fig.3 OVP case

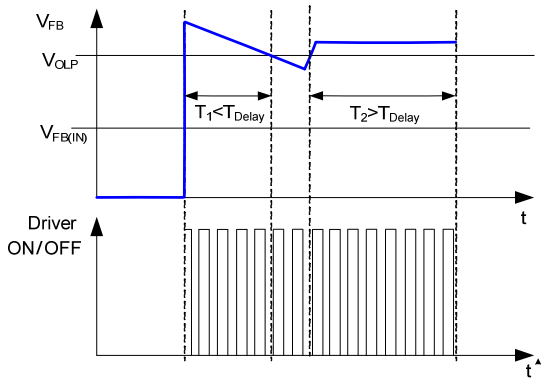



Fig.4 OLP case

**OLP**

OLP will shut down driver when $V_{FB}$> $V_{OLP}$ for continual a blanking time. The OLP event as followed Fig.4.

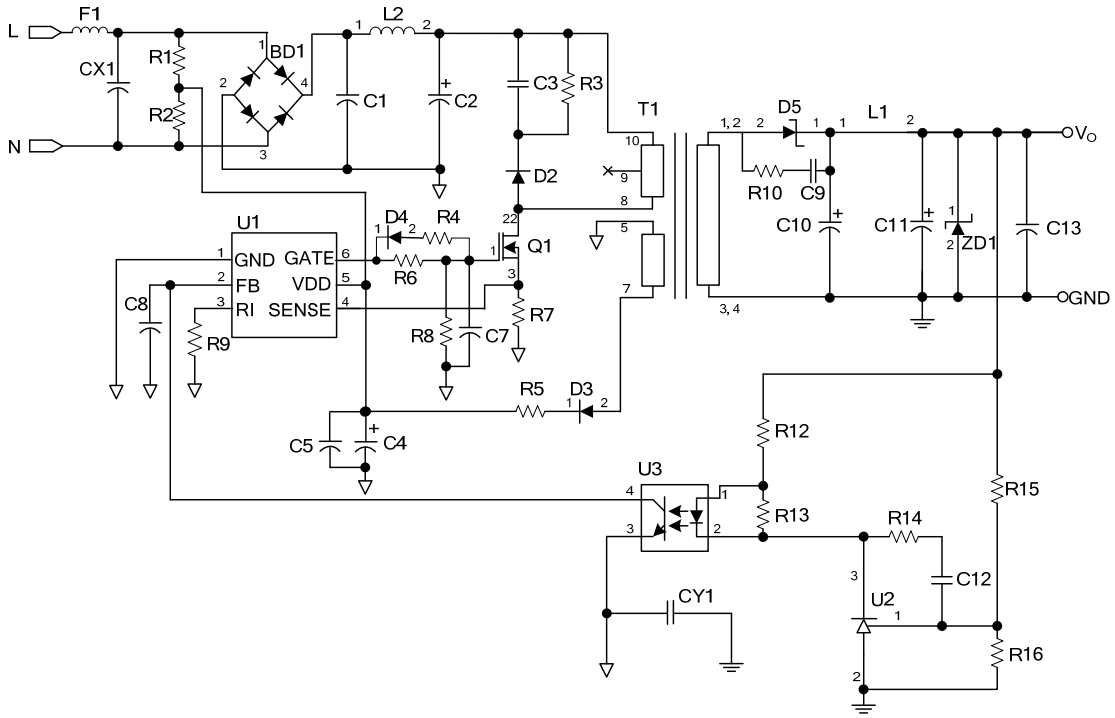
**OTP**

OTP will shut down driver when junction temperature $T_J$>$T_{(THR)}$.

**PCB Layout Note**

Noise from the current sense or the control signal can cause significant pulse width jitter in continuous-conduction mode, and slope compensation helps alleviate these problems. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the **UC3863**, and increasing the power MOS gate resistance is advised.

■ REFRENCE CIRCUIT (12V/1.5A)

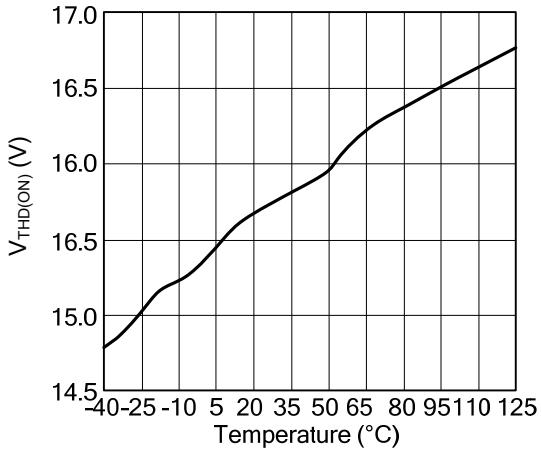



**BOM**

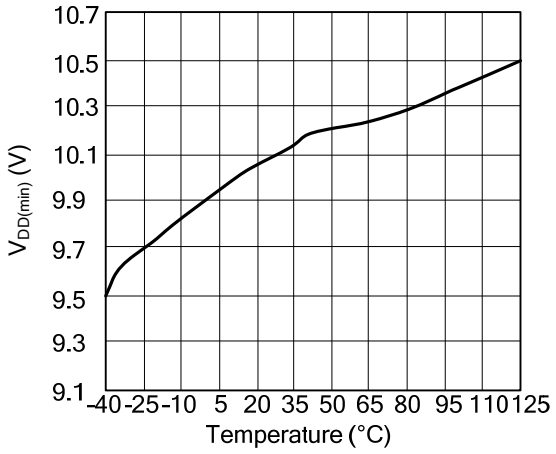
| Reference | Component | Reference | Component |
|---|---|---|---|
| BD1 | 1N4007×4 | L2 | 33μH 6*8mm |
| CX1 (Optional) | NC | Q1 | 4N65K |
| CY1 (Optional) | YC 102P/400V (Y1) | R1,R2 | R 4.7MΩ 1206 |
| C2 | EC 33μF/400V 105°C | R3 | R 200K |
| C1 | EC 6.8μF/400V 105°C | R4 (Optional) | 0Ω |
| C3 | CC 0.001μF/1000V | R5 | R 24.9Ω |
| C4 | EC 10μF/50V | R6 | R 42.21Ω 1206 |
| C5,C13 (Optional) | CC 104P/50V | R7 | R 0.66Ω 1W |
| C7 (Optional) | NC | R8 | R 51kΩ 1206 |
| C8 | CC 103P/25V | R9 | R 100kΩ 0805 |
| C9 | NC | R10 | NC |
| C10 | EC 470u/10V | R12 | R 220Ω 0805 |
| C11 | EC 220u/10V | R13 | R 1KΩ 0805 |
| C12 | CC 103P/50V 0805 | R14 | R 10KΩ 0805 |
| C14 | NC | R15 | R 100kΩ 0805 |
| D2 | Diode FR107 | R16 | R 25.94kΩ 0805 |
| D4 (Optional) | 1N4148 | T1 | EE-219 |
| D5 | MBR10100 | U1 | IC **UC3863** |
| F1 | 2A/250V | U2 | TL431 |
| L1 | NC | U3 | PC817 |

## ■ TYPICAL CHARACTERISTICS

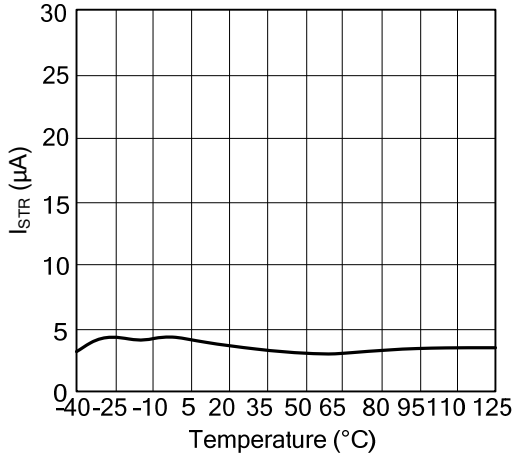
Start-up Threshold Voltage ($V_{THD(ON)}$) vs Temperature



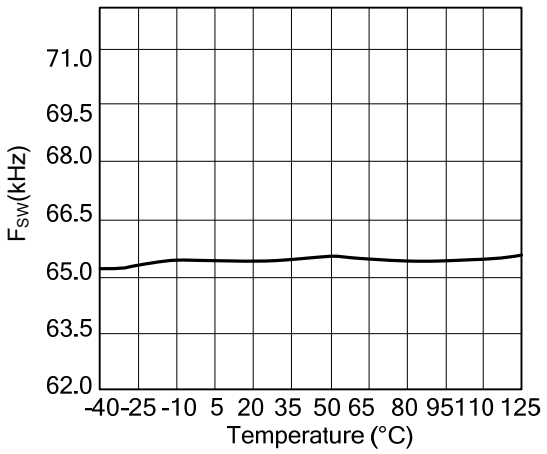

Min. Operating Voltage ($V_{DD\ (min)}$) vs Temperature



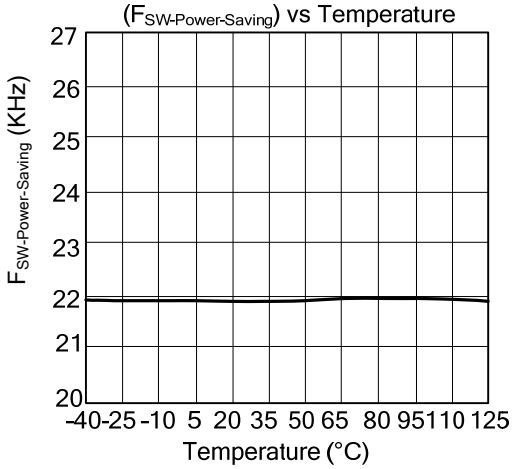

Start-up Crrent ($I_{STR}$) vs Temperature



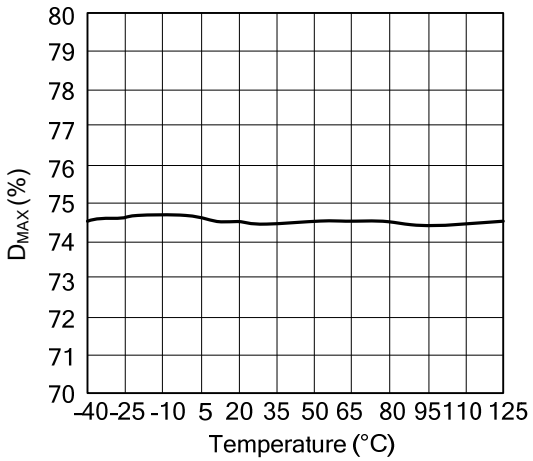

Switch Frequency ($F_{SW}$) vs Temperature



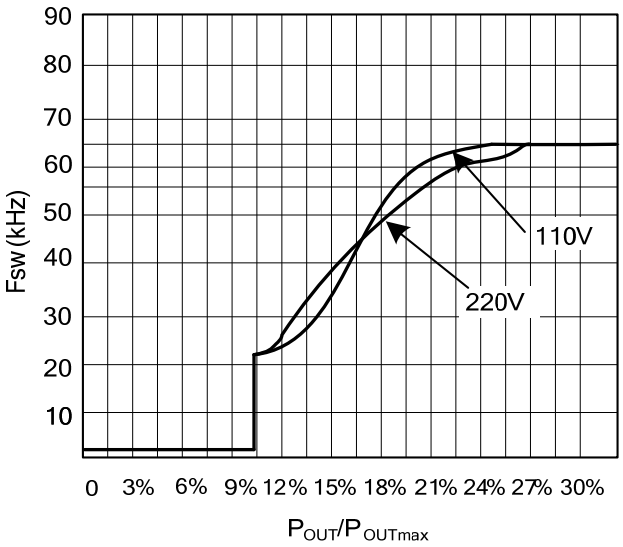

Frequency in Power-Saving mode ($F_{SW\text{-}Power\text{-}Saving}$) vs Temperature




Max. Duty Cycle ($D_{MAX}$) vs Temperature



■ TYPICAL CHARACTERISTICS (Cont.)




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