# Low-Noise, Fixed Output Voltage,300mA/500mA LDO Regulator

## General Description

The RT9167/A is a 300mA/500mA low dropout and low noise micropower regulator suitable for portable applications. The output voltages range from 1.5V to 5V in 100mV increments and 2% accuracy. The RT9167/A is designed for use with very low ESR capacitors. The output remains stable even with 1µF ceramic output capacitor.

The RT9167/A uses an internal P-MOSFET as the pass device, which does not cause extra GND current in heavy load and dropout conditions. The shutdown mode of nearly zero operation current makes the IC suitable for battery-powered devices. Other features include a reference bypass pin to improve low noise performance, current limiting, and over temperature protection.

## Ordering Information

RT9167/A-□□□□

- Package Type
  - B : SOT-23-5
  - BR : SOT-23-5 (R-Type)
  - S : SOP-8
- Lead Plating System
  - P : Pb Free
  - G : Green (Halogen Free and Pb Free)
- Output Voltage
  - 15 : 1.5V
  - 16 : 1.6V
  - :
  - 49 : 4.9V
  - 50 : 5.0V
  - 2H : 2.85V
- 500mA Output Current
- 300mA Output Current

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Features

- **Stable with Low-ESR Output Capacitor**
- **Low Dropout Voltage (350mV @ 300mA)**
- **Low Operation Current –80µA Typical**
- **Shutdown Function**
- **Low Noise Output**
- **Low Temperature Coefficient**
- **Current and Thermal Limiting**
- **Custom Voltage Available**
- **SOT-23-5 and SOP-8 Packages**
- **RoHS Compliant and 100% Lead (Pb)-Free**

## Applications

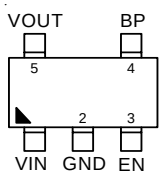
- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- Battery-powered Equipment
- Hand-held Equipment

## Marking Information

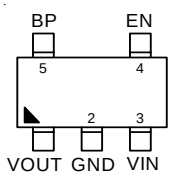
For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

## Pin Configurations

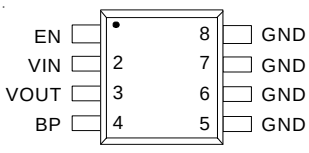
(TOP VIEW)




SOT-23-5

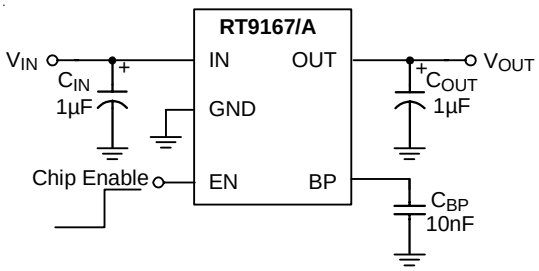



SOT-23-5 (R-Type)




SOP-8

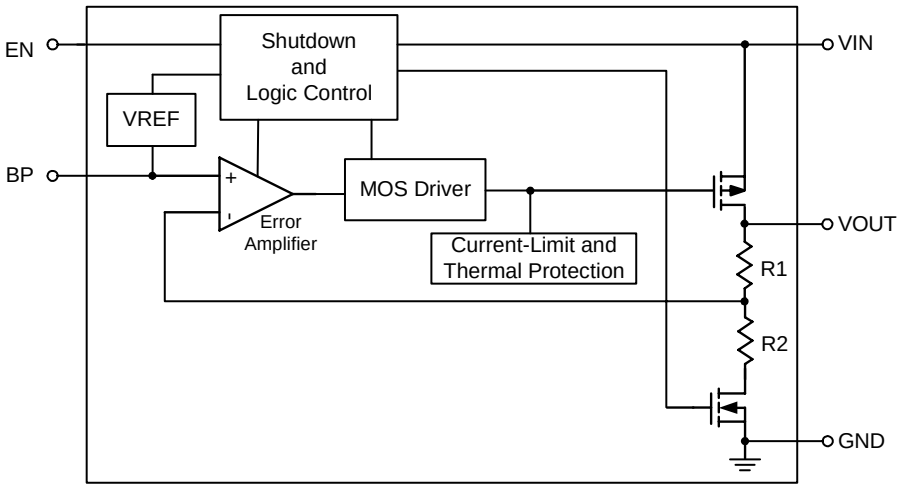
## Typical Application Circuit




## Functional Pin Description

| Pin Name | Pin Function |
|---|---|
| VIN | Power Input Voltage |
| GND | Ground |
| EN | Chip Enable (Active High) |
| BP | Reference Noise Bypass |
| VOUT | Output Voltage |

## Function Block Diagram



## Absolute Maximum Ratings

- Input Voltage ---------- 8V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  - SOT-23-5 ---------- 0.4W
  - SOP-8 ---------- 0.625W
- Package Thermal Resistance (Note1)
  - SOT-23-5, $\theta_{JA}$ ---------- 250°C/W
  - SOT-23-5, $\theta_{JC}$ ---------- 130°C/W
  - SOP-8, $\theta_{JA}$ ---------- 160°C/W
  - SOP-8, $\theta_{JC}$ ---------- 60°C/W
- Operating Junction Temperature Range ---------- –40°C to 125°C
- Storage Temperature Range ---------- –65°C to 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C

## Electrical Characteristics

($V_{IN}$ = 5.0V, $C_{IN}$ = 1μF, $C_{OUT}$ = 1μF, $T_A$ = 25°C, unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input Voltage Range | | $V_{IN}$ | | 2.9 | -- | 7 | V |
| | | | $I_L$ = 50mA | 2.7 | -- | 7 | |
| Output Voltage Accuracy | | $\Delta V_{OUT}$ | $I_L$ = 1mA | -2 | -- | 2 | % |
| Maximum Output Current | RT9167 | $I_{MAX}$ | | 300 | -- | -- | mA |
| | RT9167A | | | 500 | -- | -- | |
| Current Limit | RT9167 | $I_{LIM}$ | $R_{LOAD}$ = 1Ω | 400 | -- | -- | mA |
| | RT9167A | | | 500 | 700 | -- | |
| Quiescent Current | RT9167/A | $I_G$ | No Load | -- | 80 | 150 | μA |
| | RT9167/A | | $I_{OUT}$ = 300mA | -- | 90 | 150 | |
| | RT9167A | | $I_{OUT}$ = 500mA | -- | 90 | 150 | |
| Dropout Voltage (2) ($V_{OUT(Normal)}$ = 3.0V Version) | RT9167/A | $V_{DROP}$ | $I_{OUT}$ = 1mA | -- | 1.1 | 5 | mV |
| | RT9167/A | | $I_{OUT}$ = 50mA | -- | 55 | 100 | |
| | RT9167/A | | $I_{OUT}$ = 300mA | -- | 350 | 450 | |
| | RT9167A | | $I_{OUT}$ = 500mA | -- | 600 | 750 | |
| Line Regulation | | $\Delta V_{LINE}$ | $V_{IN}$= ($V_{OUT}$+0.15) to 7V, $I_{OUT}$ =1mA | -- | -- | 6 | mV/V |
| Load Regulation | RT9167/A | $\Delta V_{LOAD}$ | $I_{OUT}$ = 0mA to 300mA | -- | -- | 30 | mV |
| | RT9167A | | $I_{OUT}$ = 0mA to 500mA | -- | -- | 35 | |
| EN Input High Threshold | | $V_{IH}$ | $V_{IN}$= 3V to 5.5V | 1.6 | -- | -- | V |
| EN Input Low Threshold | | $V_{IL}$ | $V_{IN}$ = 3V to 5.5V | -- | -- | 0.4 | V |
| EN Bias Current | | $I_{SD}$ | | -- | -- | 100 | nA |
| Shutdown Supply Current | | $I_{GSD}$ | $V_{OUT}$ = 0V | -- | 0.01 | 1 | μA |
| Thermal Shutdown Temperature | | $T_{SD}$ | | -- | 155 | -- | °C |

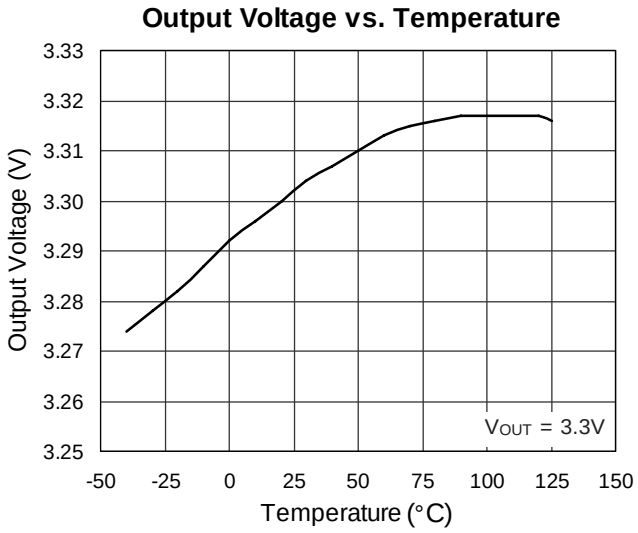
*To be continued*

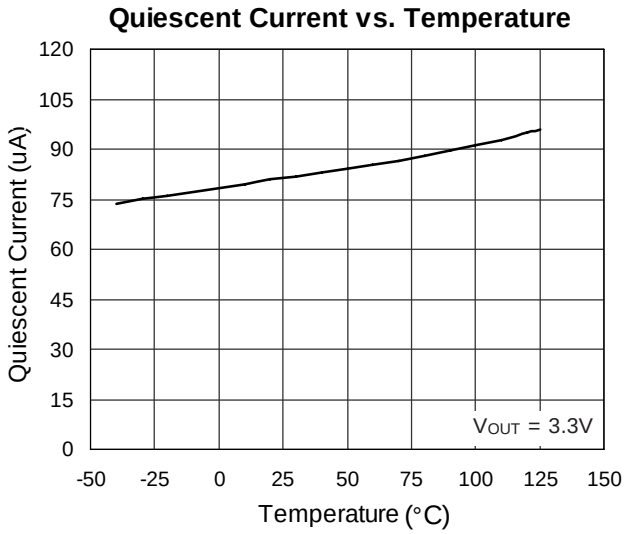
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Noise | $e_{NO}$ | $C_{BP}$ = 10nF, $C_{OUT}$ = 10μF | -- | 350 | -- | $nV\sqrt{Hz}$ |
| Ripple Rejection | PSRR | F = 100Hz, $C_{BP}$ = 10nF, $C_{OUT}$ = 10μF | -- | 58 | -- | dB |

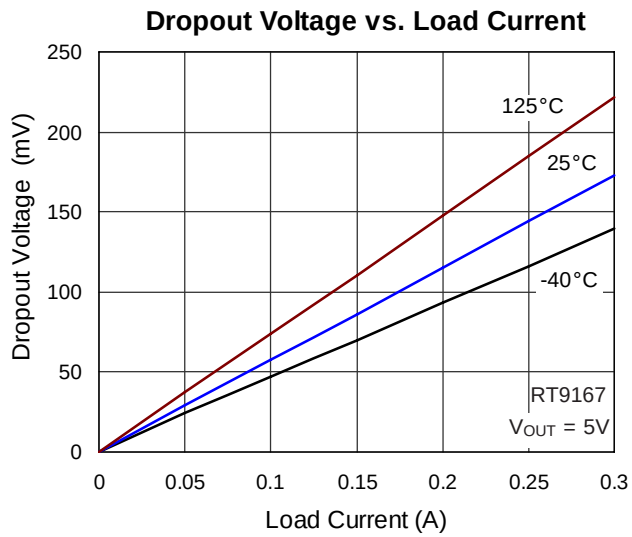
Note 1. $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 1 of SOP-8 and pin4 of SOT-23-5 packages are the case position for $\theta_{JA}$ measurement.

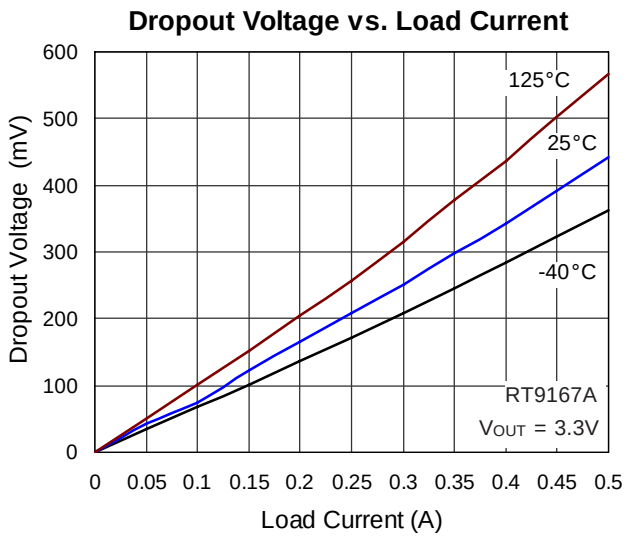
Note 2. The dropout voltage is defined as $V_{IN}$ -$V_{OUT}$, which is measured when $V_{OUT}$ is $V_{OUT(NORMAL)}$ – 100mV.

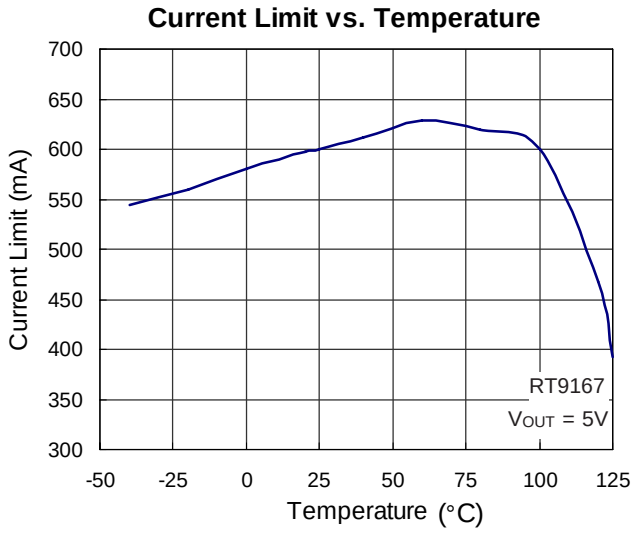
## Typical Operating Characteristics

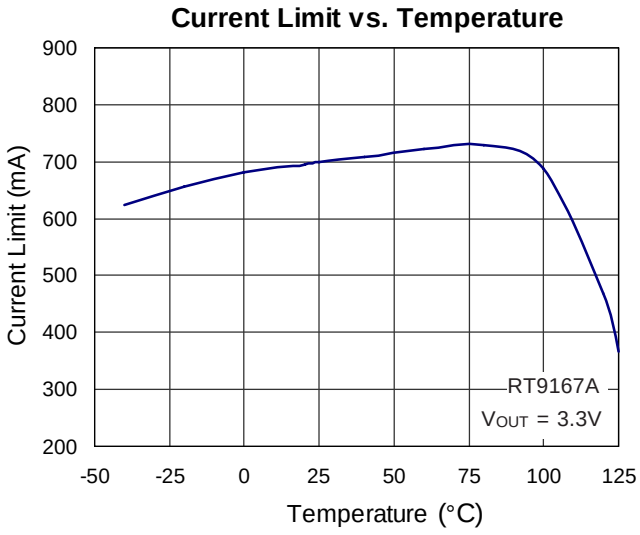


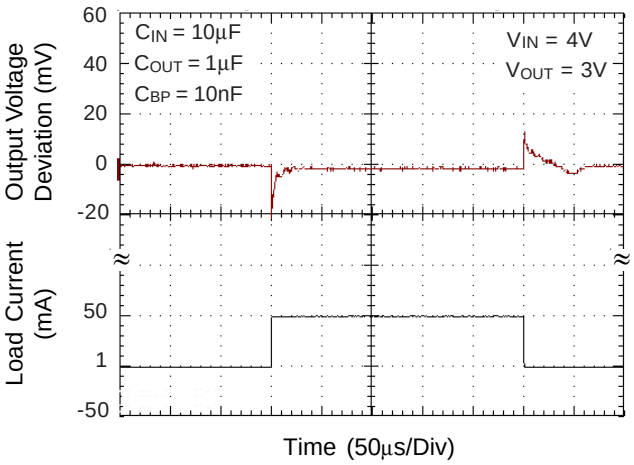



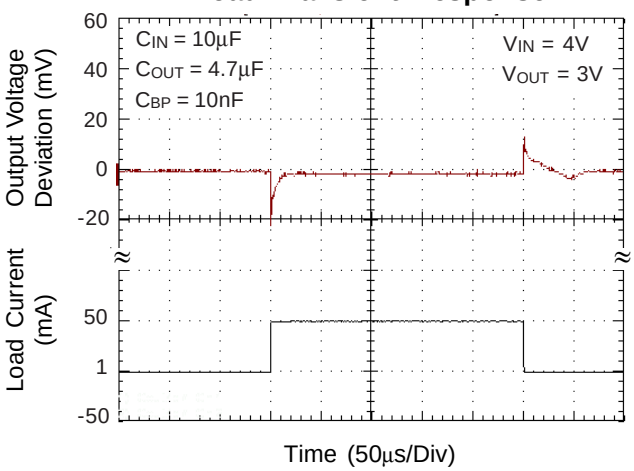



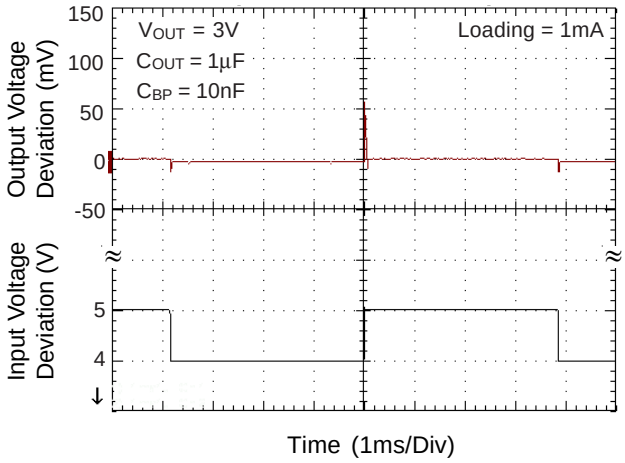
**Load Transient Response**



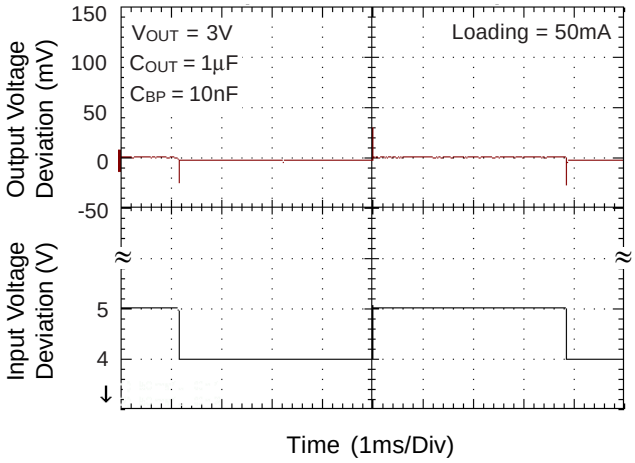

**Load Transient Response**



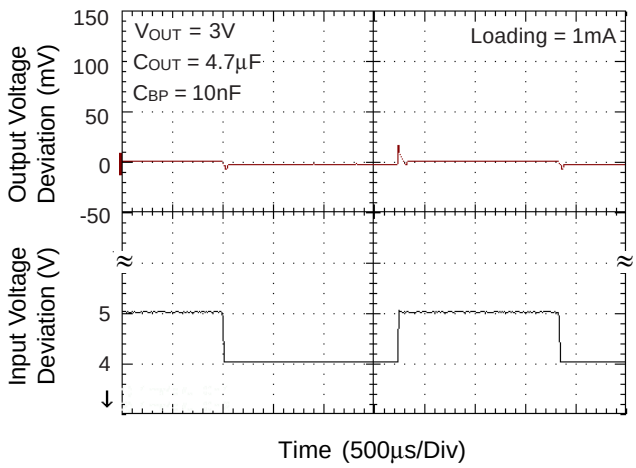

**Line Transient Response**



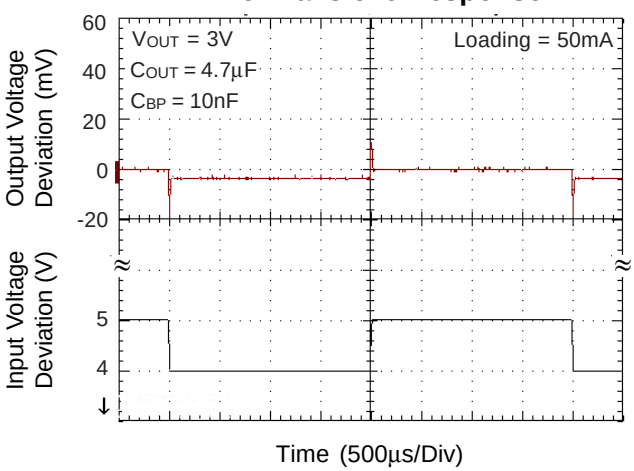

**Line Transient Response**

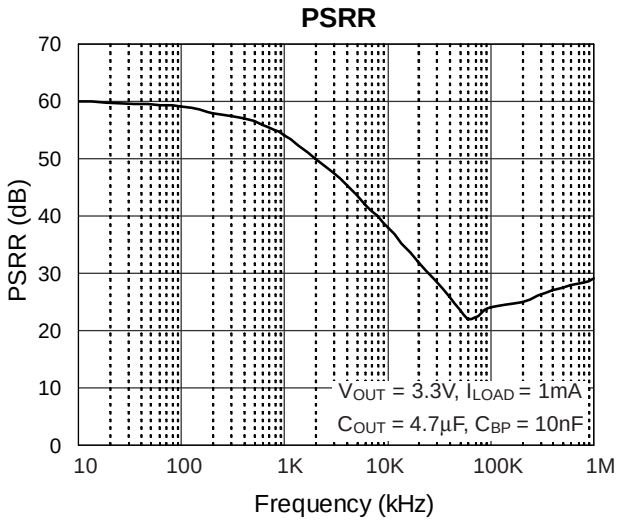



**Line Transient Response**




**Line Transient Response**




PSRR
70
60
50
40
30
20
10
0
PSRR (dB)
10
100
1K
10K
100K
1M
Frequency (kHz)
VOUT = 3.3V, ILOAD = 1mA
COUT = 4.7µF, CBP = 10nF

## Application Information

### Capacitor Selection and Regulator Stability

Like any low-dropout regulator, the external capacitors used with the RT9167/A must be carefully selected for regulator stability and performance.

Using a capacitor whose value is > 1μF on the RT9167/A input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5" from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9167/A is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 5mΩ on the RT9167/A output ensures stability. The RT9167/A still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output voltages and capacitor values. Output capacitor of larger capacitance can reduce noise and improve load-transient response, stability, and PSRR. The output capacitor should be located not more than 0.5" from the $V_{OUT}$ pin of the RT9167/A and returned to a clean analog ground.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. It may be necessary to use 2.2μF or more to ensure stability at temperatures below –10°C in this case. Also, tantalum capacitors, 2.2μF or more may be needed to maintain capacitance and ESR in the stable region for strict application environment.

Tantalum capacitors maybe suffer failure due to surge current when it is connected to a low-impedance source of power (like a battery or very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed to have a surge current rating sufficient for the application by the manufacture.

Use a 10nF bypass capacitor at BP for low output voltage noise. The capacitor, in conjunction with an internal 200kΩ resistor, which connects bypass pin and the band-gap reference, creates an 80Hz low-pass filter for noise reduction. Increasing the capacitance will slightly decrease the output noise, but increase the start-up time. The capacitor connected to the bypass pin for noise reduction must have very low leakage. This capacitor leakage current causes the output voltage to decline by a proportional amount to the current due to the voltage drop on the internal 200kΩ resistor. Figure 2 shows the power on response.

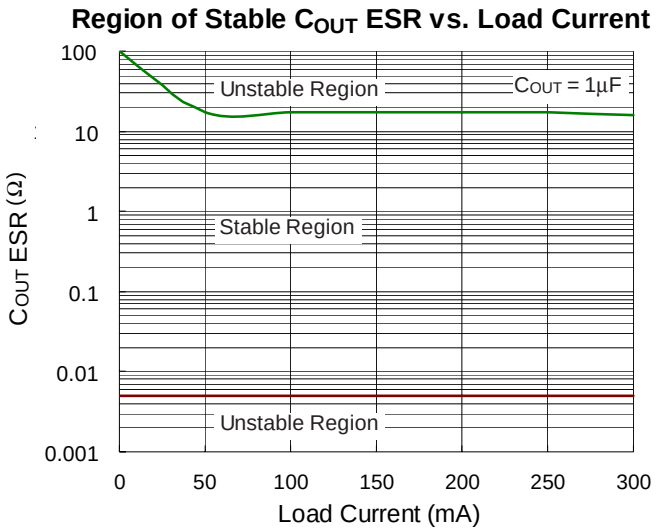



Figure 1

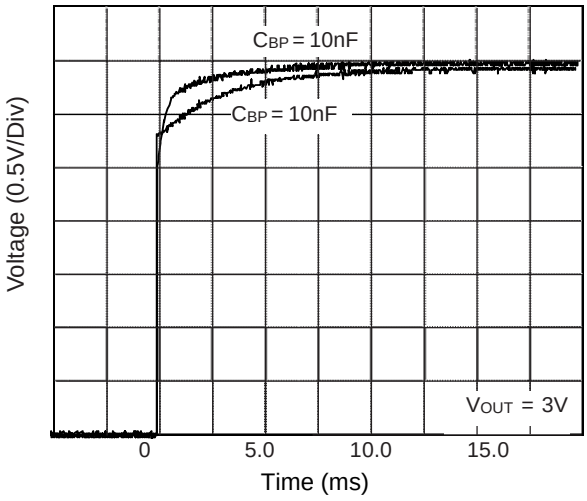



Figure 2

### Load-Transient Considerations

The RT9167/A load-transient response graphs (see Typical Operating Characteristics) show two components of the output response: a DC shift from the output impedance due to the load current change, and the transient response. The DC shift is quite small due to the excellent load regulation of the IC. Typical output voltage transient spike for a step change in the load current from 0mA to 50mA is tens mV, depending on the ESR of the output capacitor. Increasing the output capacitor's value and decreasing the ESR attenuates the overshoot.

### Shutdown Input Operation

The RT9167/A is shutdown by pulling the EN input low, and turned on by driving the input high. If this feature is not to be used, the EN input should be tied to VIN to keep the regulator on at all times (the EN input must **not** be left floating).

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turn-on/turn-off voltage thresholds which guarantee an ON or OFF state (see Electrical Characteristics). The ON/OFF signal may come from either CMOS output, or an open-collector output with pull-up resistor to the RT9167/A input voltage or another logic supply. The high-level voltage may exceed the RT9167/A input voltage, but must remain within the absolute maximum ratings for the EN pin.

### Internal P-Channel Pass Transistor

The RT9167/A features a typical 1.1Ω P-MOSFET pass transistor. It provides several advantages over similar designs using PNP pass transistors, including longer battery life. The P-MOSFET requires no base drive, which reduces quiescent current considerably. PNP-based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base-drive currents under large loads. The RT9167/A does not suffer from these problems and consume only 80μA of quiescent current whether in dropout, light-load, or heavy-load applications.

### Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the RT9167/A uses a P-Channel MOSFET pass transistor, the dropout voltage is a function of drain-to-source on-resistance [$R_{DS(ON)}$] multiplied by the load current.

### Reverse Current Path

The power transistor used in the RT9167/A has an inherent diode connected between the regulator input and output (see Figure 3). If the output is forced above the input by more than a diode-drop, this diode will become forward biased and current will flow from the $V_{OUT}$ terminal to $V_{IN}$. This diode will also be turned on by abruptly stepping the input voltage to a value below the output voltage. To prevent regulator mis-operation, a Schottky diode should be used in any applications where input/output voltage conditions can cause the internal diode to be turned on (see Figure4). As shown, the Schottky diode is connected in parallel with the internal parasitic diode and prevents it from being turned on by limiting the voltage drop across it to about 0.3V. < 100mA to prevent damage to the part.

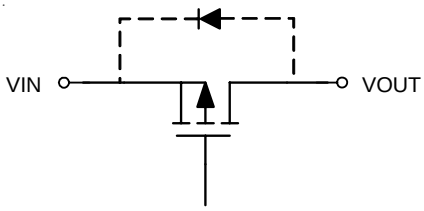



Figure 3

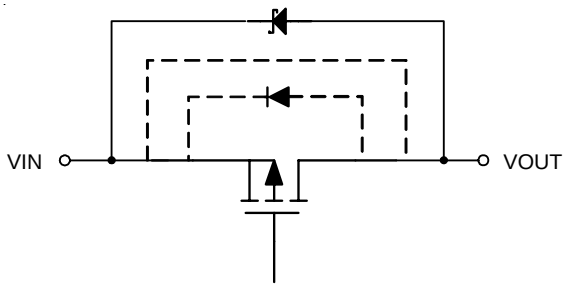



Figure 4

### Operating Region and Power Dissipation

The maximum power dissipation of RT9167/A depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipation across the device is $P = I_{OUT} (V_{IN} – V_{OUT})$. The maximum power dissipation is: $PMAX = (T_J – T_A) / \theta_{JA}$

where $T_J – T_A$ is the temperature difference between the RT9167/A die junction and the surrounding environment, $\theta_{JA}$ is the thermal resistance from the junction to the surrounding environment. The GND pin of the RT9167/A performs the dual function of providing an electrical connection to ground and channeling heat away. Connect the GND pin to ground using a large pad or ground plane.

### Current Limit and Thermal Protection

T9167 includes a current limit which monitors and controls the pass transistor's gate voltage limiting the output current to 350mA Typ. (700mA Typ. for RT9167A). Thermal-overload protection limits total power dissipation in the RT9167/A. When the junction temperature exceeds $T_J = 155°C$, the thermal sensor signals the shutdown logic turning off the pass transistor and allowing the IC to cool. The thermal sensor will turn the pass transistor on again after the IC's junction temperature cools by 10°C, resulting in a pulsed output during continuous thermal-overload conditions. Thermal-overloaded protection is designed to protect the RT9167/A in the event of fault conditions. Do not exceed the absolute maximum junction-temperature rating of $T_J = 150°C$ for continuous operation. The output can be shorted to ground for an indefinite amount of time without damaging the part by cooperation of current limit and thermal protection.

### Thermal Considerations

Thermal protection limits power dissipation in RT9167/A. When the operation junction temperature exceeds 165°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 30°C.

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = ( T_{J(MAX)} – T_A ) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, $T_A$ is the ambient temperature and the $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9167/A, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and $T_A$ is the operated ambient temperature. The junction to ambient thermal resistance $\theta_{JA}$ is layout dependent. For SOT-23-5 package, the thermal resistance $\theta_{JA}$ is 250°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at $T_A = 25°C$ can be calculated by following formula :

$P_{D(MAX)} = (125°C – 25°C) / 250 = 0.4W$ for SOT-23-5 package

$P_{D(MAX)} = (125°C - 25°C) / 160 = 0.625W$ for SOP-8 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance $\theta_{JA}$. For RT9167/A packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

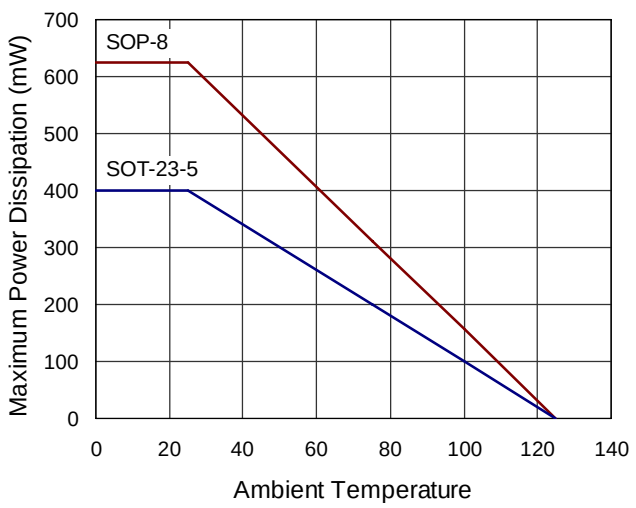



Figure 5. Derating Curves for RT9167/A Packages

The value of junction to case thermal resistance $\theta_{JC}$ is popular for users. This thermal parameter is convenient for users to estimate the internal junction operated temperature of packages while IC operating. It's independent of PCB layout, the surroundings airflow effects and temperature difference between junction to ambient. The operated junction temperature can be calculated by following formula :

$T_J = T_C + P_D \times \theta_{JC}$

Where $T_C$ is the package case temperature measured by thermal sensor, $P_D$ is the power dissipation defined by user' s function and the $\theta_{JC}$ is the junction to case thermal resistance provided by IC manufacturer. Therefore it's easy to estimate the junction temperature by any condition.

For example, how to calculate the junction temperature of RT9167A-28CB SOT-23-5 package. If we use input voltage $V_{IN}$ = 3.3V at an output current $I_O$ = 500mA and the case temperature (pin 4 of SOT-23-5 package) $T_C$ = 70°C measured by thermal couple while operating, then our power dissipation is as follows :

$P_D = (3.3V - 2.8V) \times 500mA + 3.3V \times 90\mu A \cong 250mW$

And the junction temperature $T_J$ could be calculated as following :

$T_J = T_C + P_D \times \theta_{JC}$

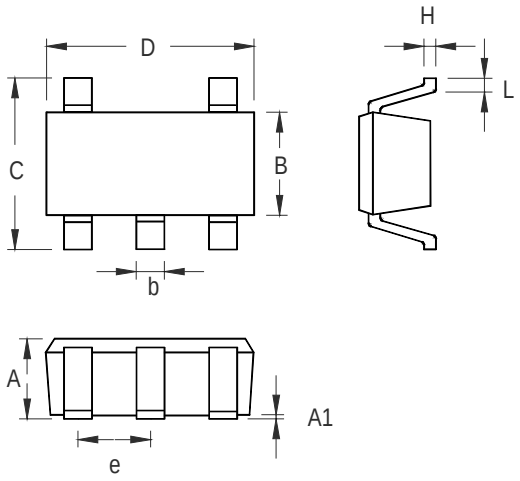
$T_J = 70°C + 0.25W \times 130°C/W$

$= 70°C + 32.5°C$

$= 102.5°C < T_{J(MAX)} = 125°C$

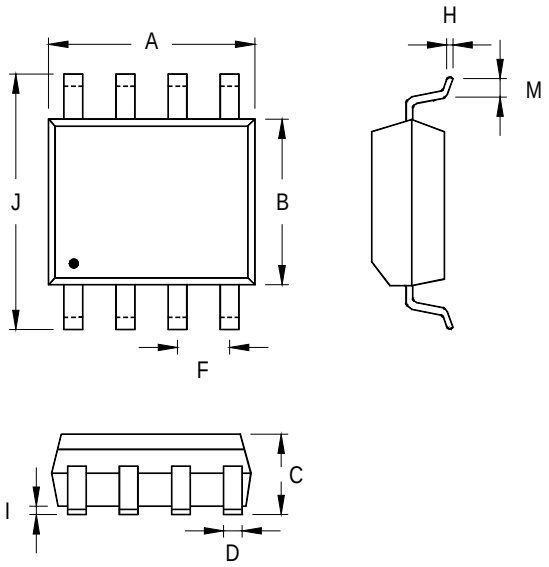
For this operation application, $T_J$ is lower than absolute maximum operation junction temperature 125°C and it's safe to use.

## Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.889 | 1.295 | 0.035 | 0.051 |
| A1 | 0.000 | 0.152 | 0.000 | 0.006 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.356 | 0.559 | 0.014 | 0.022 |
| C | 2.591 | 2.997 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| e | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

**SOT-23-5 Surface Mount Package**




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.170 | 0.254 | 0.007 | 0.010 |
| I | 0.050 | 0.254 | 0.002 | 0.010 |
| J | 5.791 | 6.200 | 0.228 | 0.244 |
| M | 0.400 | 1.270 | 0.016 | 0.050 |

**8-Lead SOP Plastic Package**


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